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Using the CMOS Dual Monostable Multivibrator

Fairchild Semiconductor
Application Note 138
May 1975

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INTRODUCTION

The MM54C221/MM74C221 is a dual CMOS monostable multivibrator. Each one-shot has three inputs (A, B and CLR) and two outputs (Q and $\overline{Q}$). The output pulse width is set by an external RC network.

The A and B inputs trigger an output pulse on a negative or positive input transition respectively. The CLR input when low resets the one-shot. Once triggered the A and B inputs have no further control on the output.

THEORY OF OPERATION

Figure 1 shows that in its stable state, the one-shot clamps C_{EXT} to ground by turning N1 ON and holds the positive comparator input at V_{CC} by turning N2 OFF. The prefix N is used to denote N-channel transistors.

The signal, G, gating N2 OFF also gates the comparator OFF thereby keeping the internal power dissipation to an absolute minimum. The only power dissipation when in the stable state is that generated by the current through R_{EXT}. The bulk of this dissipation is in R_{EXT} since the voltage drop across N1 is very small for normal ranges of R_{EXT}.

To trigger the one-shot the CLR input must be high.

The gating, G, on the comparator is designed such that the comparator output is high when the one-shot is in its stable state. With the CLR input high the clear input to FF is disabled allowing the flip-flop to respond to the A or B input. A negative transition on A or a positive transition on B sets Q to a high state. This in turn gates N1 OFF, and N2 and the comparator ON.

Gating N2 ON establishes a reference of 0.63 V_{CC} on the comparator's positive input. Since the voltage on C_{EXT} can not change instantaneously V1 = 0V at this time. The comparator then will maintain its one level on the output. Gating N1 OFF allows C_{EXT} to start charging through R_{EXT} toward V_{CC} exponentially.

Assuming a perfect comparator (zero offset and infinite gain) when the voltage on C_{EXT}, V1, equals 0.63 V_{CC} the comparator output will go from a high state to a low state resetting Q to a low state. *Figure 2* is a timing diagram summarizing this sequence of events.

This diagram is idealized by assuming zero rise and fall times and zero propagation delay but it shows the basic operation of the one-shot. Also shown is the effect of taking the CLR input low. Whenever CLR goes low FF is reset independent of all other inputs. *Figure 2* also shows that once triggered, the output is independent of any transitions on B (or A) until the cycle is complete.

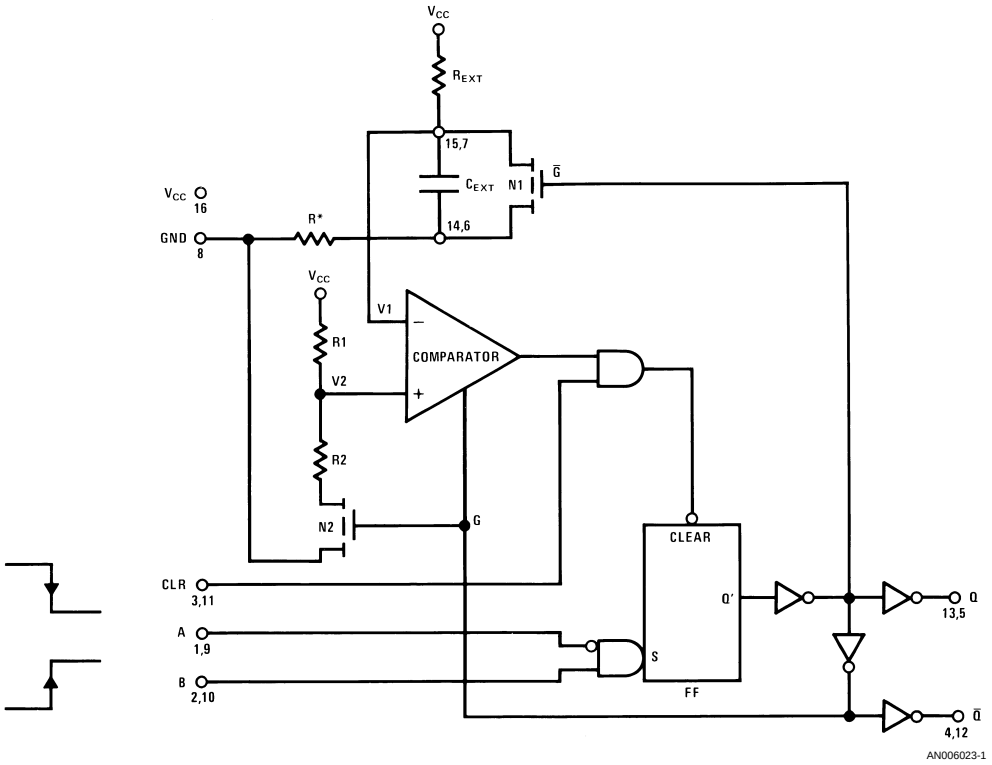


FIGURE 1. Monostable Multivibrator Logic Diagram

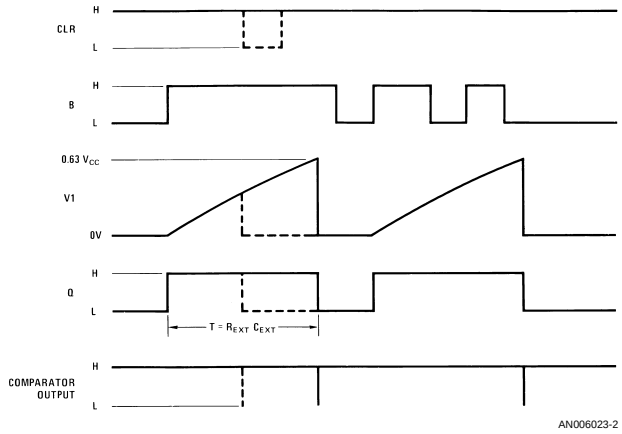


FIGURE 2. One-Shot Timing Diagram

The output pulse width is determined by the following equation:

$$V1 = V_{CC} (1 - e^{-T/R^{EXT}C^{EXT}}) = 0.63\ V_{CC} \quad (1)$$

Solving for t gives:

$$T = R_{EXT}\ C_{EXT}\ \text{In}\ (1/0.37) = R_{EXT}\ C_{EXT} \quad (2)$$

A word of caution should be given in regards to the ground connection of the external capacitor (C_{EXT}). It should always be connected as shown in *Figure 1* to pin 14 or 6 and never to pin 8. This is important because of the parasitic resistor R*. Because of the large discharge current through R*, if the

capacitor is connected to pin 8, a four layer diode action can result causing the circuit to latch and possible damage itself.

ACCURACY

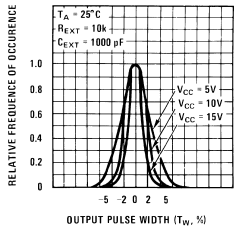
There are many factors which influence the accuracy of the one-shot. The most important are:

1. Comparator input offset
2. Comparator gain
3. Comparator time delay
4. Voltage divider R1, R2
5. Delays in logic elements
6. ON impedance of N1 and N2
7. Leakage of N1
8. Leakage of C_{EXT}
9. Magnitude of R_{EXT} and C_{EXT}

The characteristics of C_{EXT} and R_{EXT} are, of course, not determined by the characteristics of the one-shot. In order to establish the accuracy of the one-shot, devices were tested using an external resistance of 10 kΩ and various capacitors. A resistance of 10 kΩ was chosen because the leakage and ON impedance of transistor N1 have a minimal effect on accuracy with this value of resistance.

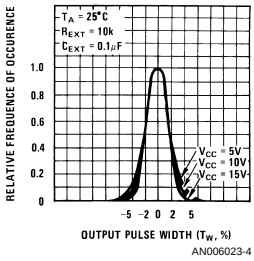
Two values of C_{EXT} were chosen, 1000 pF and 0.1 µF. These values give pulse widths of 10 µs and 1000 µs with R_{EXT} = 10 kΩ.

Figure 3 and *Figure 4* show the resulting distributions of pulse widths at 25˚C for various power supply voltages. Because propagation delays, at the same power supply voltage, are the same independent of pulse width, the shorter the pulse width the more the accuracy is affected by propagation delay. *Figure 3* and *Figure 4* clearly show this effect. As pointed out in Application Note AN-90, 54C/74C Family Characteristics, propagation delay is a function of V_{CC}. *Figure 3,* (Pulse Width = 10 µs) shows much greater variation with V_{CC} than *Figure 4* (Pulse Width = 1000 µs). This same information is shown in *Figure 5* and *Figure 6* in a different format. In these figures the percent deviation from the average pulse width at 10V V_{CC} is shown vs V_{CC}. In addition to the average value the 10% and 90% points are shown. These percentage points refer to the statistical distribution of pulse width error. As an example, at V_{CC} = 10V for 10 µs pulse width, 90% of the devices have errors of less than +1.7% and 10% have errors less than −2.1%. In other words, 80% have errors between +1.7% and −2.1%.



0% point pulse width:
At V_{CC} = 5V, T_W = 10.6 µs
At V_{CC} = 10V, T_W = 10 µs
At V_{CC} = 15V, T_W = 9.8 µs
Percentage of units within 4%:
At V_{CC} = 5V, 90% of units
At V_{CC} = 10V, 95% of units
At V_{CC} = 15V, 98% of units

FIGURE 3. Typical Pulse Width Distribution for 10 µs Pulse



0% pulse width:
At V_{CC} = 5V, T_W = 1020 µs
At V_{CC} = 10V, T_W = 1000 µs
At V_{CC} = 15V, T_W = 982 µs
Percentage of units within 4%:
At V_{CC} = 5V, 95% of units
At V_{CC} = 10V, 97% of units
At V_{CC} = 15V, 98% of units

FIGURE 4. Typical Pulse Width Distribution for 1000 µs Pulse

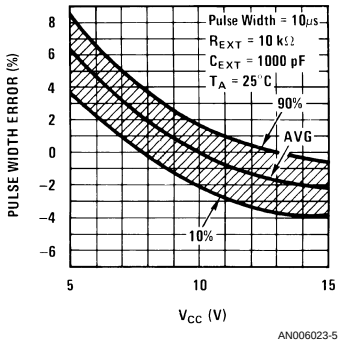


FIGURE 5. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 10 µs)

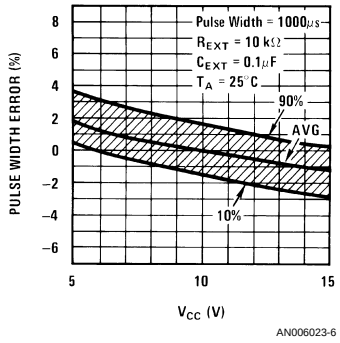


FIGURE 6. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 1000 µs)

The minimum error can be obtained by operating at the maximum V_{CC}. A price must be paid for this and this price is, of course, increased power dissipation.

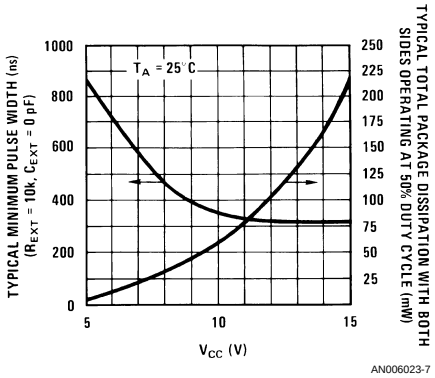


FIGURE 7. Typical Minimum Pulse Width and Power Dissipation vs V_{CC}

Figure 7 shows typical power dissipation vs V_{CC} operating both sides of the one-shot at 50% duty cycle. Also shown in the same figure is typical minimum pulse width vs V_{CC}. The minimum pulse width is a strong function of internal propagation delays. *It is obvious from these two curves that in creasing V_{CC} beyond 10V will not appreciably improve inaccuracy due to propagation delay but will greatly increase power dissipation.*

Accuracy is also a function of temperature. To determine the magnitude of its effects the one-shot was tested at temperature with the external resistance and capacitance maintained at 25˚C. The resulting variation is shown in *Figure 8* and *Figure 9*.

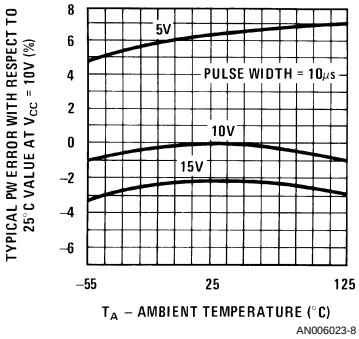


FIGURE 8. Typical Pulse Width Error vs Temperature (PW = 10 µs)

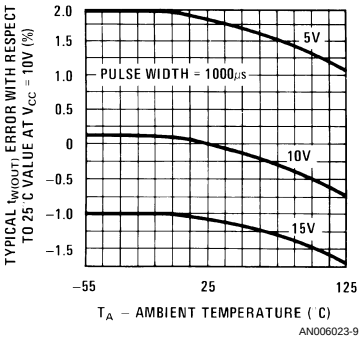


FIGURE 9. Typical Pulse Width Error vs Temperature (PW = 1000 µs)

Up to this point the external timing resistor, R_{EXT}, has been held fixed at 10 kΩ. In actual applications other values may be necessary to achieve the desired pulse width. The question then arises as to what effect this will have on accuracy.

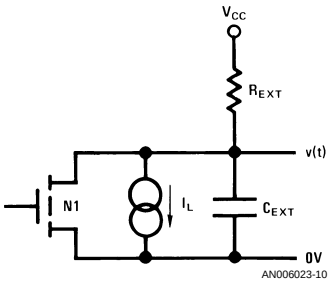


FIGURE 10.

As R_{EXT} becomes larger and larger the leakage current on transistor N1 becomes an ever increasing problem. The equivalent circuit for this leakage is shown in *Figure 10*.

v(t) is given by:

$$v(t) = (V_{CC} - I_L R_{EXT}) (1 - e^{-t^L/R^{EXT} C^{EXT}})$$

As before, when v(t) = 0.63 V_{CC}, the output will reset. Solving for t_L gives:

$$t_L = R_{EXT} C_{EXT} \ell n \left(\frac{V_{CC} - I_L R_{EXT}}{0.37 V_{CC} - I_L R_{EXT}} \right) \quad (3)$$

Using T as defined in Equation 2 the pulse width error is:

$$\text{PW Error} = \frac{t_L - T}{T} \times 100\%$$

Substituting Equations 2 and 3 gives:

$$\text{PW Error} = \frac{R_{EXT} C_{EXT} \ell n \left(\frac{V_{CC} - I_L R_{EXT}}{0.37 V_{CC} - I_L R_{EXT}} \right) - R_{EXT} C_{EXT} \ell n(1/0.37)}{R_{EXT} C_{EXT} \ell n (1/0.37)}$$

PW Error is plotted in *Figure 11* for V_{CC} = 5, 10 and 15V. As expected, decreasing V_{CC} causes PW Error to increase with fixed I_L. Note that the leakage current, although here assumed to flow through N1, is general and could also be interpreted as leakage through C_{EXT}. See MM54C221/MM74C221 data sheet for leakage limits.

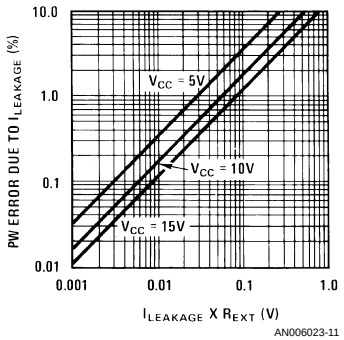


FIGURE 11. Percentage Pulse Width Error Due to Leakage

To demonstrate the usefulness of *Figure 11* an example will be most helpful. Let us assume that N1 has a leakage of 250 x 10^{-9}A, C_{EXT} has leakage of 150 x 10^{-9}A, output pulse width = 0.1 sec and V_{CC} = 5V. What R_{EXT} C_{EXT} should be used to guarantee an error due to leakage of less than 5%.

From *Figure 11* we see that to meet these conditions R_{EXT} I_L < 0.14V.

Then:

R_{EXT} < 0.14/(250 + 150) x 10^{-9}

< 350 kΩ

Choosing standard component values of 250 kΩ and 0.004 µF would satisfy the above conditions.

We have just defined the limitation on the maximum size of R_{EXT}. There is a corresponding limit on the minimum size that R_{EXT} can assume. This is brought about because of the finite ON impedance of N1. As R_{EXT} is made smaller and smaller the amount of voltage across N1 becomes significant. The voltage across N1 is:

$$V_{NI} = V_{CC} r_{ON}/(R_{EXT} + r_{ON}) \quad (4)$$

The output pulse width is defined by:

$v(t_O) = (V_{CC} - V_{N1}) (1 - -t^{O/R^{EXT}} C^{EXT})$

$+ V_{N1} = 0.63 V_{CC}$

Solving for t_O gives:

$$t_O = R_{EXT}\, C_{EXT}\, \ell n \left(\frac{V_{CC} - V_{N1}}{0.37\, V_{CC}} \right)$$

Pulse Width Error is then:

$$\text{PW Error} = \frac{t_O - T}{T} \times 100\%$$

Substituting Equations 2 and 4 gives:

$$= \frac{R_{EXT}\, C_{EXT}\, \ell n \left(\frac{V_{CC} - V_{N1}}{0.37\, V_{CC}} \right) - R_{EXT}\, C_{EXT}\, \ell n\,(1/0.37)}{R_{EXT}\, C_{EXT}\, \ell n\,(1/0.37)}$$

This function is plotted in *Figure 12* for r_{ON} of 50Ω, 25Ω, and 16.7Ω. These are the typical values of r_{ON} for a V_{CC} of 5V, 10V and 15V respectively.

As an example, assume that the pulse width error due to r_{ON} must be less than 0.5% operating at V_{CC} = 5V. The typical value of r_{ON} for V_{CC} = 5V is 50Ω. Referring to the 50Ω curve in *Figure 12*, R_{EXT} must be greater than 10 kΩ to maintain this accuracy. At V_{CC} = 10V, R_{EXT} must be greater than 5 kΩ as can be seen from the 25Ω curve in *Figure 12*.

Although clearly shown in the MM54C221/MM74C221 data sheet, it is worthwhile, for the sake of clarity, to point out that the parasitic capacitance between pins 7(15) and 6(14) is typically 15 pF. This capacitor is in parallel with C_{EXT} and must be taken into account when accuracy is critical.

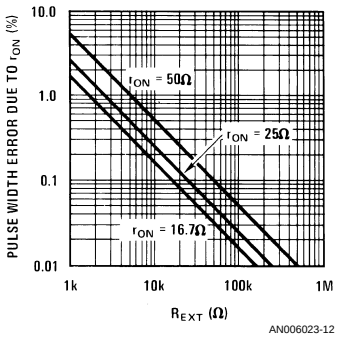
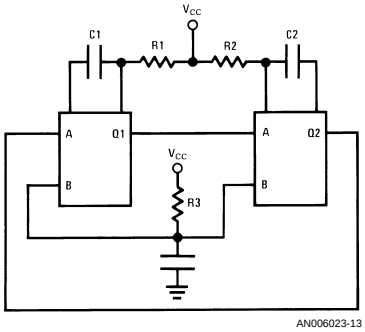


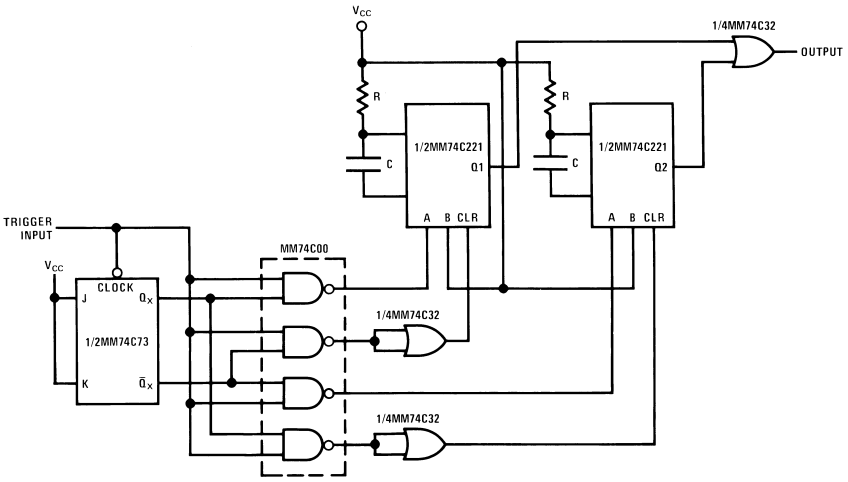
FIGURE 12. Percentage Pulse Width Error Due to Finite r_{ON} of Transistor N1 vs R_{EXT}

TYPICAL APPLICATIONS

Basic One-Shot Oscillator

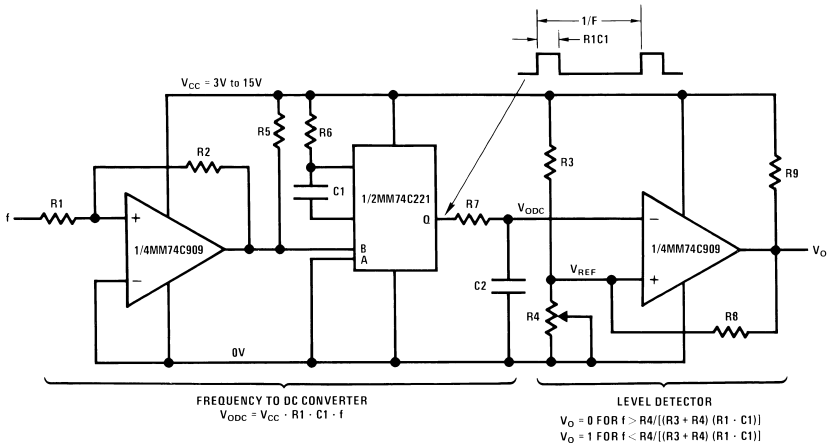


Retriggerable One-Shot



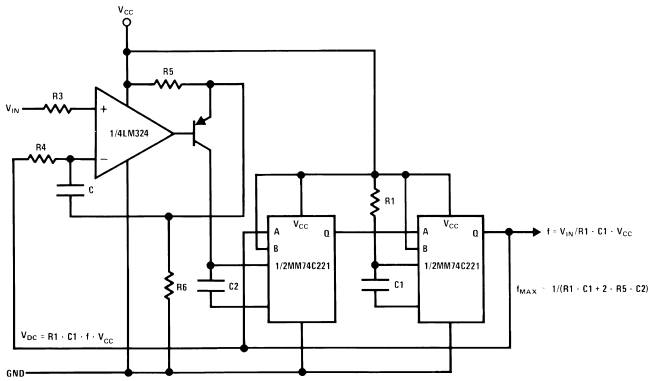
AN006023-14

Frequency Magnitude Comparator



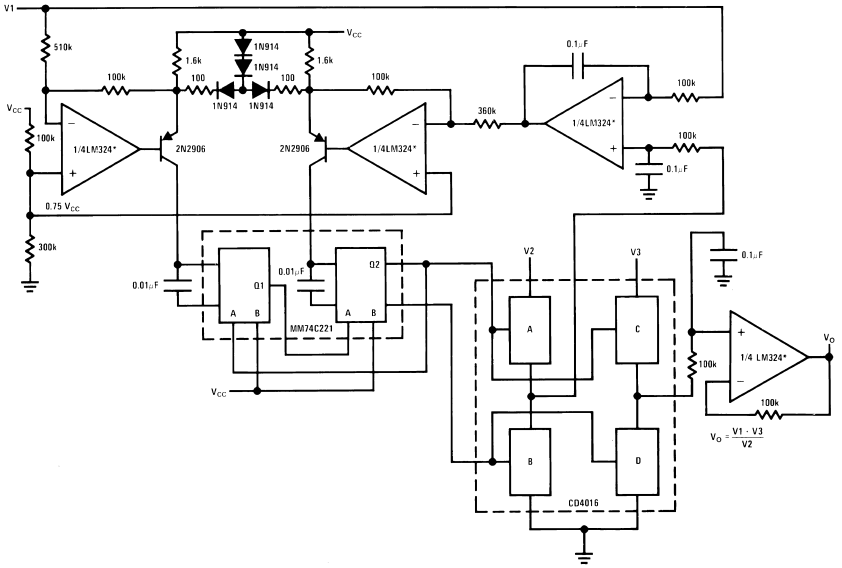
AN006023-15

Linear VCO



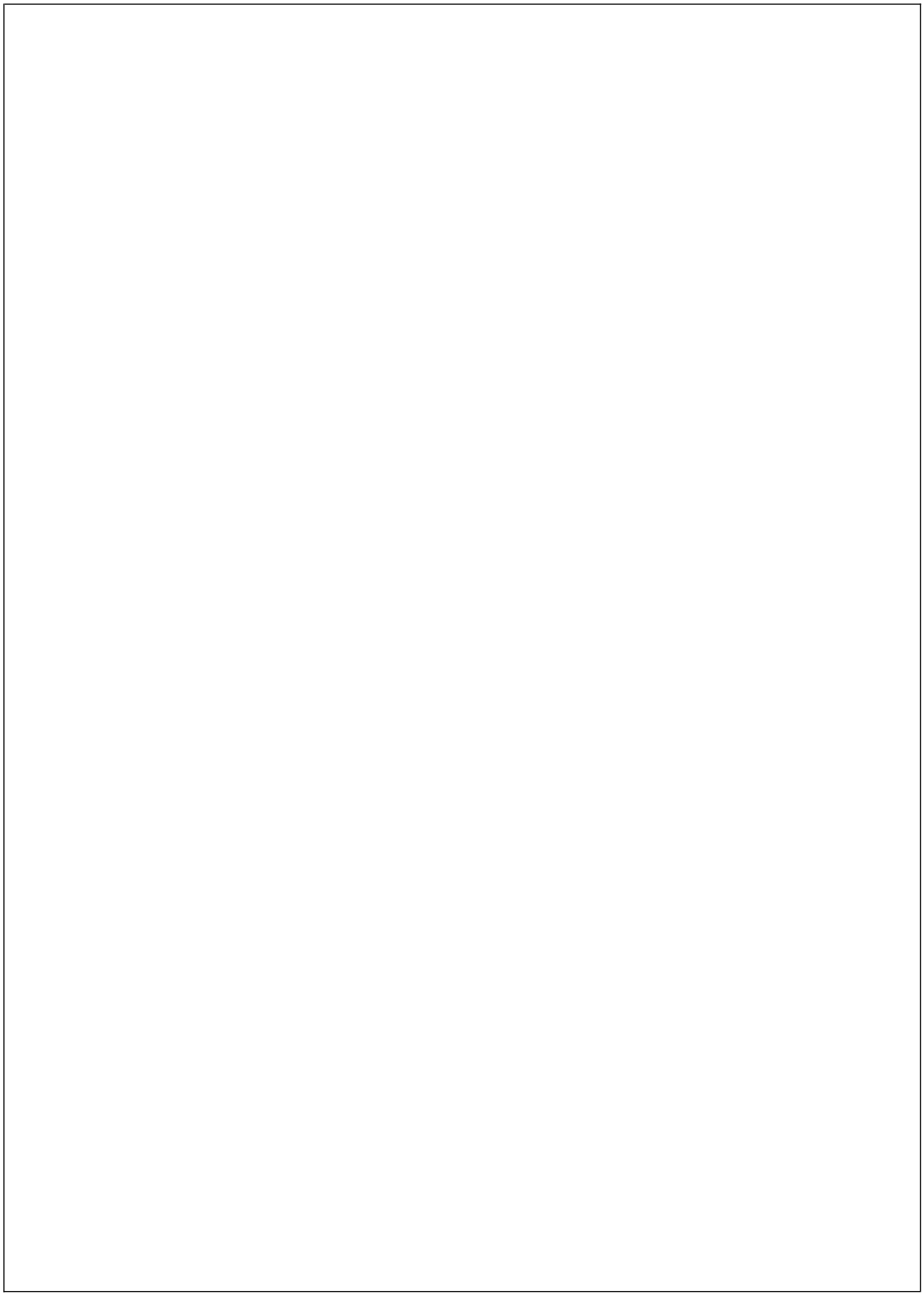
AN006023-16

Analog Multiplier/Divider



AN006023-17

*ON LM324 $V^+ = V_{CC}$
$V^- = GND$



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