Design Review: Power Stage Design for a 200W Off-Line Power Supply

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ABSTRACT

This paper describes the design of the power train of a two switch forward power supply with a continuous PFC front end based on the FAN4800. Design choices for such a power supply are reviewed. Practical topics including power device selection, magnetic design, layout and EMI are discussed with the aim of helping practicing engineers to accelerate and improve their designs.

1 Introduction

New AC power supply designs in the range 200W - 500W increasingly require power factor correction (PFC) which reduces the energy wasted in the power utility supply lines and increases the maximum power which can be drawn from a power outlet.

This article describes the design and construction of a 200W power supply intended for use in an LCD TV, so a lot of attention has been paid to achieve high efficiency, standby power below 1W, small form factor, especially a height of 25mm, simple cooling without a fan and last but not least, low cost. These features are indispensable for the intended application.

2 Circuit Description and Design

The specifications for this design are:

- AC Input Voltage: 85 – 265V_{RMS}
- Power-Factor: > 0.95
- Total Output Power: 200W
- Three DC Outputs: 5V/0.3A, 12V/5A, 24V/6A

The power supply consists of two units.

The first power supply incorporates a PFC circuit, built around the FAN4800 PFC/PWM combo controller and generates the 24V/6A and the 12V/6A outputs. This device contains an average current-mode PFC controller and a PWM controller able to work in both voltage and current mode. In the presented application, the PWM works in current mode and controls a two switch forward converter. This converter generates a regulated 24V

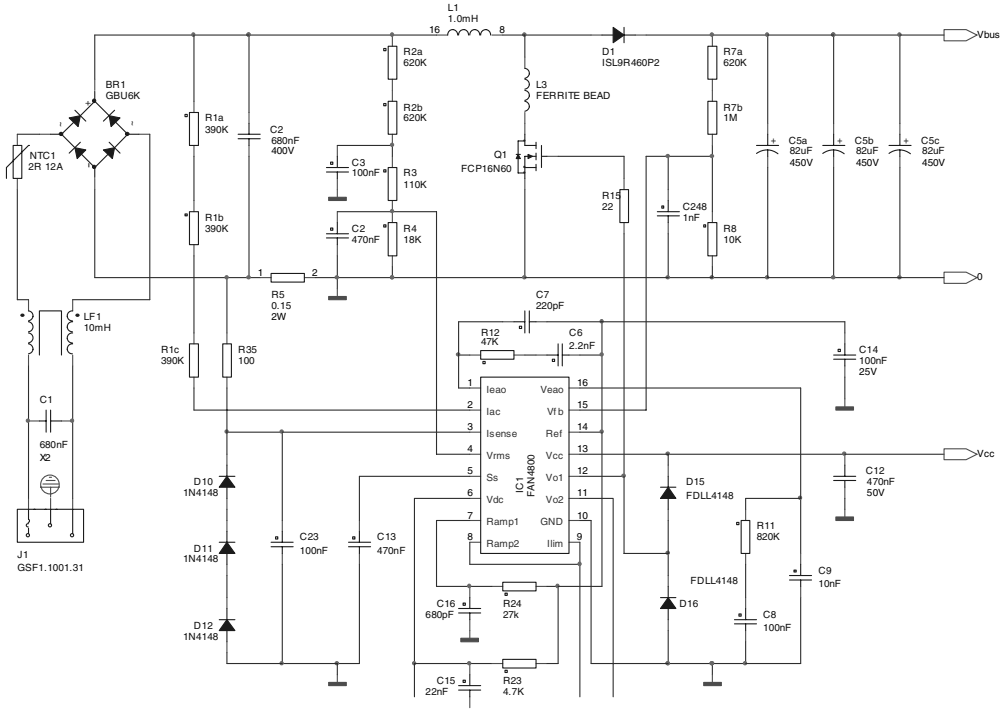

Figure 1: Schematic of the PFC. (In this schematic part references have been chosen to comply with AN-6032)

output. The 12V output is generated with a buck converter controlled by an MC34063A PWM controller. This additional block improves regulation of the 12V output and reduces cross-regulation problems, which is always a problem with a multiple output forward converter when loads vary over a wide range. The additional converter cost is not very high if one keeps in mind the more complex and larger coupled inductor for a dual output forward converter.
The second power supply is a flyback converter based on the Fairchild Power Switch (FPS) FSD210B that generates both the 5V output and the supply voltage for the FAN4800. This power supply is the one that is active in standby mode and its no load power consumption is below 500mW. Therefore, it is possible to meet the 1W limit for standby consumption even with a small load in an active power save mode.
For simplicity, the design calculations and schematics will be given for each block individually. The complete schematic and layout can be found in the appendix.

3 Power Factor Correction

This section reviews the selection of the power devices used in the PFC circuit. The dimensioning of the low power parts that set up the operating point of the multiplier and the gain and frequency compensation of the error amplifiers is reviewed in [1].

3.1 Rectifier

Since the main power supply is designed to deliver an output power of 200W, the total input power, Pin, assuming a efficiency of 90% for the PFC and an efficiency of 90% for the forward converter, including output stage will be:

$$P_{In} = \frac{200W}{0.9 \cdot 0.9} = \underline{247W}$$

With the minimal input voltage of $85V_{RMS}$ one gets an maximum input current of:

$$I_{In,RMS} = \frac{247W}{85V} = \underline{2.9A}$$

The common mode choke of the EMI filter has to cope with this current and must at the same time have a high inductance of more than 15mH. There are a few chokes on the market, that combine high current, high inductance and low profile, namely from EPCOS and TDK. The actual value and type of the choke has to be determined with EMI testing and, depending on the operating conditions, might differ from the filter that is proposed in this paper.
The negative temperature coefficient thermistor (NTC) in series with the input limits the inrush current, but is not really necessary for the operation of the power supply.

The rectifier could be selected according to $I_{In,RMS}$, but noting that diodes with higher current ratings normally have a lower voltage drop at a given current, it is favorable to use a rectifier bridge with a slightly higher current rating. For the actual design, a 6A/800V bridge GBU6K has been chosen.
The rectifier loss can be estimated in the well known manner approximating the diode forward characteristic by a constant forward voltage plus a series resistance. The forward voltage V_F and the series resistance R_S have to be estimated from the datasheet as 0.8V and 0.03Ω respectively for the GBU6K. The loss equation then becomes:

$$\begin{aligned} P_{Loss,BR1} &= 4 \cdot (I_{AVG,D} \cdot V_{F,D} + I_{RMS,D}^2 \cdot R_{S,D}) \\ &= 4 \cdot (I_{In,RMS} \cdot 0.45 \cdot 0.8V + \left(\frac{I_{In,RMS}}{\sqrt{2}}\right)^2 \cdot 0.03\Omega) \\ &= \underline{4.7W} \end{aligned}$$

If one assumes an absolute maximum junction temperature TJ of 150°C and a maximum ambient temperature TA of 50°C then the maximum thermal resistance (case to ambient) of the heatsink for BR1 should be

$$\begin{aligned} R_{\Theta,BR1} &= \frac{T_{J,max} - T_{A,max}}{P_{Loss,BR1}} \\ &= \frac{150°C - 50°C}{4.7W} - \frac{0.75°C}{W} \\ &\approx \underline{21°C/W} \end{aligned}$$

3.2 Inductor L_1

In the presented design the amplitude of the ripple current through L_1 was chosen to be 20% of the input current. With this choice, the inductance can be calculated according to the following equation [2]:

$$\begin{aligned} L_1 &= \frac{\left(V_{Out} - \sqrt{2} \cdot V_{In,min}\right) \cdot V_{In,min}^2}{V_{Out} \cdot f_S \cdot dI \cdot P_{In}} \\ &= \frac{(400V - 85V \cdot \sqrt{2}) \cdot 85V^2}{400V \cdot 100kHz \cdot 20\% \cdot 247W} \\ &= \underline{1.08mH} \end{aligned}$$

giving an inductance of almost exactly 1mH. The peak current of L_1 is

$$\begin{aligned} I_{Peak,L1} &= I_{In,RMS} \cdot \sqrt{2} + I_{Ripple}/2 \\ &= I_{In,RMS} \cdot \sqrt{2} + 0.2 \cdot I_{In,RMS} \cdot \sqrt{2}/2 \\ &= I_{In,RMS} \cdot \sqrt{2} \cdot 1.1 \\ &= \underline{4.5A} \end{aligned}$$

while the RMS current is equal to the RMS input current. With this current and a current density of 5A/mm^2 the necessary copper area is about 0.58mm^2. Since the high frequency current is only 20% of the input current, skin- and proximity effect are not very distinct. Three or four thinner wires in parallel, having in sum the required area, are sufficient. In the actual design three wires of 0.5mm diameter have been used, leading to a current density slightly below 5A/mm^2.

The core size of L_1 is chosen with the help of the so-called core area product A_P, which is the product of the effective magnetic cross section and the winding area (of the bobbin). This product can easily shown to be

$$A_P = A_e \cdot A_w = \frac{L \cdot I_{Peak} \cdot A_{Cu}}{B_{Peak} \cdot f_{Cu}}$$

where A_{Cu} is the copper area, B_{Peak} is the saturation flux density ($\leq$0.35T for most ferrites) and f_{Cu} the copper fill factor, that is about 0.5 for a simple inductor and about 0.4 for a transformer with several windings. With these data the necessary A_P for L_1 is

$$A_P = 14914\text{mm}^4$$

Based on the observance that for most cores the magnetic cross section and the winding area are very similar, one looks for a core with

$$A_e = \sqrt{A_P}$$

So for our application, a suitable core should have an A_e of about 122mm^2. While it is not difficult to find cores with this magnetic cross section, the height of the inductor is limited to 25mm by the application. Therefore, after some careful searching of core and bobbin datasheets, an EER3542 core was chosen, with an A_e of 107mm^2 and an A_W of 154mm^2, giving an A_P of about 16500mm^4

An approximate length s of the gap in the center leg is given by:

$$s \approx 0.4 \cdot \pi \cdot A_e \cdot \left(\frac{1}{A_L} - \frac{1}{A_{L,0}} \right)$$

where $A_{L,0}$ is the A_L of the ungapped core (given in the core's datasheet) and the A_L of the gapped core is 1mH/124^2 = 65nH. If the latter two values are in nH and A_e is given in mm^2, the gap length s is in mm. In this particular case the gap length is about 2 mm.

3.3 Q_1 and D_1

Since the maximum rated input voltage is 265V_{RMS}, maximum drain voltage of 500V for Q_1 seems to be sufficient. It is nevertheless recommended to use a 600V rated MOSFET, since experience shows that a 600V MOSFET is able to withstand the surge test according to IEC 61000-4-5 without damage, while a 500V type needs additional surge voltage limiters. The same is valid for boost diode D_1. This is due to the fact that the electrolytic cap C5 is able to absorb a lot of energy, protecting a 600V device but not a 500V device.

The peak currents of Q_1 and D_1 are identical to that through L_1 i.e. 4.5A, while the RMS current of Q_1 is given by:

$$\begin{aligned} I_{RMS,Q1} &= I_{In,RMS} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{In,Min}}{3 \cdot V_{Out}}} \\ &= 2.9\text{A} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 85\text{V}}{3 \cdot \pi \cdot 400\text{V}}} \\ &= \underline{2.5\text{A}} \end{aligned}$$

and that of D_1 is:

$$\begin{aligned} I_{RMS,D1} &= I_{In,RMS} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{In,Min}}{3 \cdot V_{Out}}} \\ &= 2.9\text{A} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot 85\text{V}}{3 \cdot \pi \cdot 400\text{V}}} \\ &= \underline{1.46\text{A}} \end{aligned} \quad .$$

Especially for the MOSFET, low losses and not the peak current is the important factor for selecting a certain device. After some calculations the SUPERFET^{TM} FCP16N60 with a maximum R_{DSon} of about 0.45Ω @ 100°C has been chosen. The total losses of Q_1 have to be divided into conduction and switching losses. The conduction losses are:

$$\begin{aligned} P_{Loss,Q1}^{Cond} &= I_{RMS,Q1}^2 \cdot R_{DSON_{max},Q1} \\ &= \underline{2.8\text{W}} \end{aligned}$$

Switching losses are further divided into losses due to the discharge of the Drain-Source capacitance (plus parasitic capacitances e.g. of the L_1 and PCB), losses due to the overlap of voltage and current during the switching process and losses due to reverse recovery of D_1. All three terms are not known exactly but have to be estimated with the following expressions:

$$\begin{aligned} P_{Loss,Q1}^{Cap} &\approx 0.5 \cdot \left(C_{OSS,eff} + C_{ext}\right) \cdot V_{Out}^2 \cdot f_S \\ &= 0.5 \cdot 260\text{pF} \cdot 400\text{V}^2 \cdot 100\text{kHz} \\ &= \underline{2.1\text{W}} \end{aligned}$$

$$\begin{aligned} P_{Loss,Q1}^{Cross} &\approx 0.9 \cdot I_{In,RMS} \cdot V_{Out} \cdot \frac{t_r + t_f}{2} f_S \\ &= 0.9 \cdot 2.9\text{A} \cdot 400\text{V} \cdot \frac{130 + 90}{2}\text{ns} \cdot \frac{2.9}{16} \cdot 100\text{kHz} \\ &= \underline{2.1\text{W}} \end{aligned}$$

$$\begin{aligned} P_{Loss,Q1}^{rr} &\approx Q_{rr,D1} \cdot V_{Out} \cdot f_S \\ &= 50\text{nc} \cdot 400\text{V} \cdot 100\text{kHz} \\ &= \underline{2\text{W}} \end{aligned}$$

$C_{OSS,eff}$ of the FCP16N60 is 110pF, while the parasitic capacitances C_{ext} have been estimated to be 150pF. Since the data sheet gives the rise- and fall-times at a drain current of 16A, one has to scale these values to the actual current i.e. multiply with 2.9A/16A.
Finally, the total loss of Q1 is:

$$P_{Loss,Q1} \approx \underline{9W}$$

The maximum thermal resistance of a heatsink for Q_1 therefore is about 10ºC/W.
Conduction losses of D_1 are calculated in a similar manner as those of BR_1:

$$P_{Loss,D1}^{Cond} \approx I_{AVG,D1} \cdot V_{F,D1} + I_{RMS,D1}^2 \cdot R_{S,D1}$$
$$= \frac{P_{Out}}{\eta \cdot V_{Out}} \cdot V_{F,D1} + I_{RMS,D1}^2 \cdot R_{S,D1}$$
$$= 0.56A \cdot 1.3V + 1.47A^2 \cdot 0.08\Omega$$
$$= \underline{0.9W}$$

Switching losses of D_1 are identical to the reverse recovery losses already calculated in case of the MOSFET. The total loss of the diode will be

$$P_{Loss,D1} \approx \underline{2.9W}$$

A suitable heatsink for this diode should have a thermal resistance of no more than 25ºC/W.

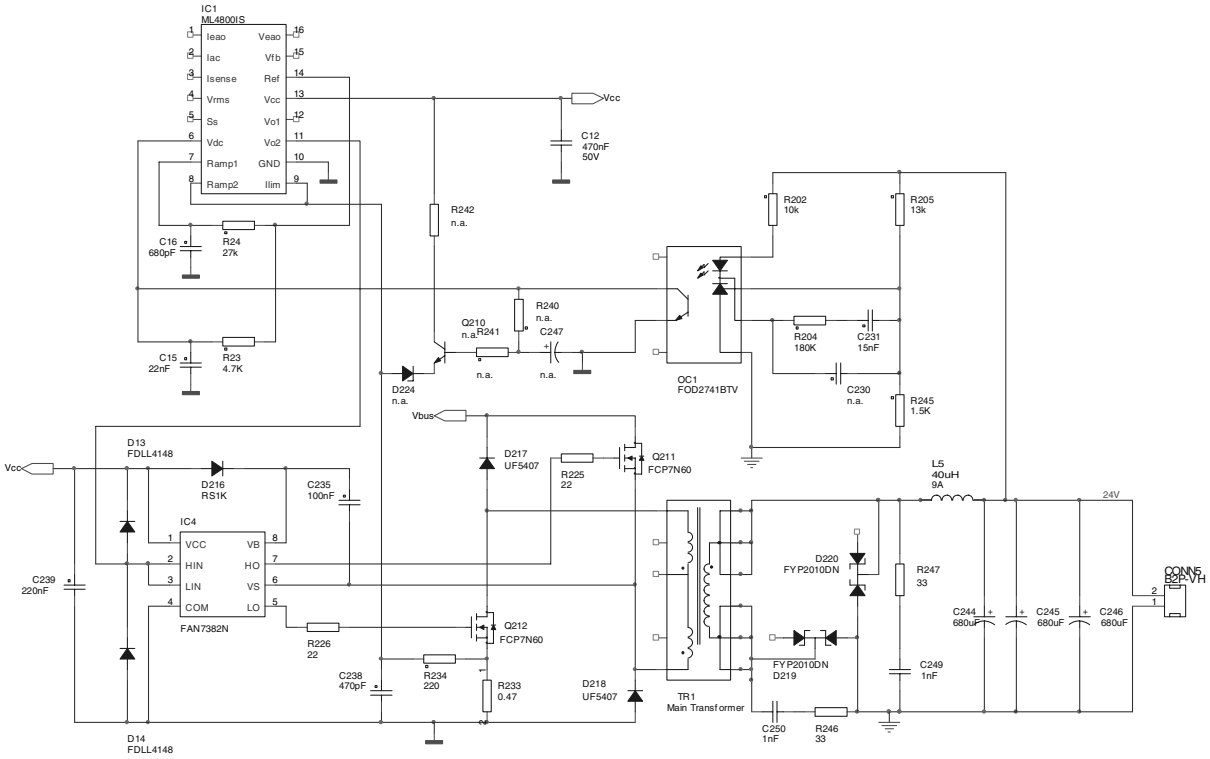

Figure 2: Schematic of the Forward Converter

4 Two Switch Forward Converter

In this application, the PWM section of the FAN4800 operates in current mode and controls a two switch forward converter. This topology is basically identical to the well known single transistor forward converter. But it has the advantage that each of the two transistors only needs a maximum drain voltage equal to the DC output voltage of the PFC. The standard forward converter in comparison needs double that value, requiring a rated drain voltage of 800 – 900V. Moreover, in the two switch version, the transformer construction is simpler and cheaper since it does not need a reset winding.

There are of course disadvantages to be considered: the proposed topology needs two transistors instead of one and the gate signal of one of them is floating at a high voltage. If one has a closer look, these issues are not that big as the on resistance of Power MOSFET is proportional to the drain voltage to the power of 2 to 2.5. That means that two transistors with half the drain voltage *and* half the on resistance – in order to get same conduction loss – use in sum less silicon.

So the cost of either solution is similar.

As the gate driver FAN7382 is used, the second drawback disappears as well. This device contains one low-side and one high-side gate driver which are completely independent. That is important since in the two switch forward both transistors are turned off and on at the same time. When both are on, the energy is transferred to the secondary, when both are off, the transformer is de-magnetized via reset diodes D217 and D218.

The main design equations for the two switch and the single switch forward are identical and therefore Fairchild Application Note AN-4137 and its associated spreadsheet [2] can be used for calculation after a few changes have been considered.

Since the converter DC voltage is generated by a PFC pre-regulator, the line voltages entered into the spreadsheet have to be chosen appropriately in order to get the right DC link voltage. In this application $284V_{RMS}$ are used for both the minimum and maximum line voltage. The line frequency does not influence the calculation.

Next, a huge DC link capacitor (e.g. 1000uF) should be entered pro forma, since, due to the PFC, the ripple voltage across the real DC link capacitor is quite small.

The maximum duty cycle has to be strictly below 0.5 to allow transformer de-magnetization. In order to leave some margin a value of 0.45 for the maximum duty cycle has been chosen.

Since the sheet was developed for a single transistor forward, the np/nr (Excel: Np/Nr) ratio and the maximum nominal MOSFET voltage can be ignored.

The choice of the current ripple factor K_{RF} for the output filter inductor L_5 is normally an iterative process. On the one hand, one would like to make this factor as small as possible to reduce the RMS and peak values of the primary and secondary side currents. On the other hand, L_5 shall not be too large. As a consequence, start with a certain ripple factor and then check whether the resulting configuration of L_5 is acceptable. In the present design a value of 0.21 has been used for K_{RF}, a value that results in an inductance of 40µH for L_5. The calculated windings will fill an EER2828 core completely. With the mentioned choice of K_{RF} the RMS and peak values of the current through Q205 and Q206 are:

$$I_{Peak,Sw} = \underline{1.6A}$$

$$I_{RMS,Sw} = \underline{0.9A}$$

As already mentioned a maximum drain voltage slightly bigger than 400V would be sufficient, effectively leading to the use of 500V rated MOSFET. Again, the use of 600V MOSFET is recommended instead of a surge voltage limiter at the input and the SUPERFET™ FCP7N60 having the following data

$$R_{DSON,max} = 1.1\Omega \quad at \quad 100°C$$

$$C_{OSS,eff} = 60pF$$

$$t_{r,max} = 120ns \quad at \quad 7A$$

$$t_{f,max} = 75ns \quad at \quad 7A$$

was chosen. The loss calculation can be easily done similar to the one for Q1.

$$P_{Loss,Sw}^{Cond} = I_{RMS,Sw1}^2 \cdot R_{DSON_{max},Sw}$$

$$= 0.9A^2 \cdot 1.1\Omega$$

$$= \underline{0.9W}$$

For forward converter with reset winding

FAIRCHILD SEMICONDUCTOR™

Blue cell	is the input parameters
Red cell	is the output parameters

1. Define specifications of the SMPS

Minimum Line voltage (V_line.min)	284	V.rms
Maximum Line voltage (V_line.max)	284	V.rms
Line frequency (fL)	50	Hz

	Vo		Io		Po		KL
1st output for feedback	24	V	8.5	A	203	W	100
2nd output	0	V	0	A	0	W	0
3rd output	0	V	0	A	0	W	0
4th output	0	V	0	A	0	W	0
Maximum output power (Po) =	202.8	W					
Estimated efficiency (Eff)	90	%					
Maximum input power (Pin) =	225.3	W					

2. Determine DC link capacitor and the DC voltage range

DC link capacitor	1000	uF
DC link voltage ripple =	4	V
Minimum DC link voltage =	397	V
Maximum DC link voltage =	402	V

3. Determine the maximum duty ratio (Dmax)

Maximum duty ratio	0.45		
Turns ratio (Np/Nr)	1	>	0.82
Maximum nominal MOSFET voltage =	803	V	

Figure 3: Excerpt of the Excel sheet belonging to AN-4134

$$P_{Loss,Q205}^{Cap} \approx 0.5 \cdot \left(C_{OSS,eff} + C_{ext}\right) \cdot V_{Out}^2 \cdot f_S$$
$$= 0.5 \cdot 120pF \cdot 400V^2 \cdot 100kHz$$
$$= \underline{1.2W}$$

$$P_{Loss,Q205}^{Cross} \approx I_{Peak,Q205} \cdot V_{Out} \cdot \frac{t_r + t_f}{2} f_S$$
$$= 1.6A \cdot 400V \cdot \frac{120+75}{2} ns \cdot \frac{1.6}{7} \cdot 100kHz$$
$$= \underline{1.4W}$$

$$P_{Loss,Q205}^{Tot} \approx \underline{3.7W}$$

This gives an upper limit for the losses. In practice, the resonance of the magnetizing inductance and the node output capacitance will reduce the value of the voltage below 400V.

The loss of Q206 is of course identical. A heatsink with a maximum thermal resistance of 20ºC/W should be used for each MOSFET.

The value of the current sense resistor R233 is chosen such, that a maximum peak current of more than 1.6A is possible. With a value of 0.56Ω, this condition is fulfilled but there is no margin left. For that reason, a value of 0.47Ω has been chosen, which results in a maximum peak current of 2.1A.

As inductor L_5, the transformer, secondary rectification and filtering can be calculated with the Excel sheet.

With the help of the formula for the A_P of the transformer given in the worksheet, an EER2834 core has been chosen for the transformer, winding data can be found in the appendix.

The calculated reverse voltage of the rectifier diodes is 57V and it is recommended to use ones with a specified maximum voltage of at least 100V. To reduce both conduction and switching losses, it is favorable to use Schottky diodes. The RMS current load is given in the spreadsheet and can be used to determine suitable diodes; the actual selection is two FYP2010DN diodes.

The average current of the rectifier diodes D219 and D220 is given by:

$$I_{Avg,rect} = I_{Out} \cdot (1 - D_{max})$$
$$= 8.5A \cdot 0.55$$
$$= \underline{4.7A}$$

and the losses are determined in a similar manner as has been done for BR1 and D1.

$$P_{Loss,rect} \approx I_{Avg,rect} \cdot V_{F,Rect} + I_{RMS,rect}^2 \cdot R_{S,Rect}$$
$$= 4.7A \cdot 0.25V + 5.7A^2 \cdot 0.04\Omega$$
$$= \underline{2.5W}$$

Again, a heatsink of not more than 20ºC/W should be used for each diode.

Due to the fast switching of the Schottky diodes, parasitic oscillations are excited that must be damped by the RC networks R246/C250 and R247/C249. While there are a lot of formulae in the literature how to determine the values of these networks, experience shows the calculated values are only a starting point for experimental optimization.

It is possible in principle to use the two diodes contained in one FYP2010, but in that case the loss per package is doubled and cooling is complicated. Another reason to use two diodes instead of one is, that the PCB is prepared for the assembly of a self driven synchronous rectifier (not shown) that needs two single diodes.

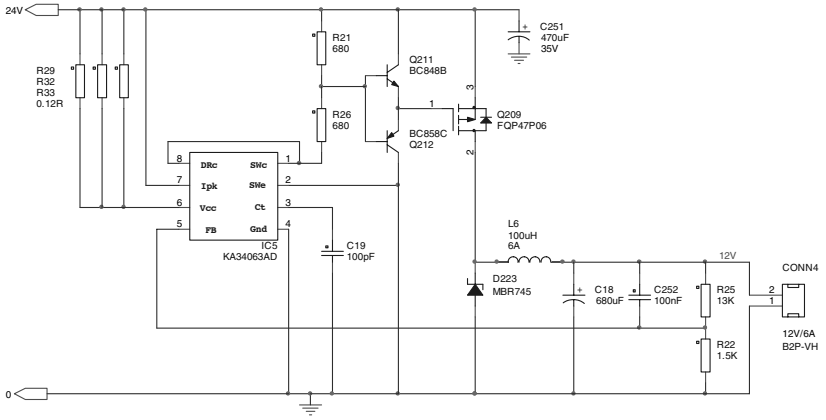

Figure 4: Schematic of the Buck Converter 24V -> 12V

5 DC/DC Converter

The Buck converter shown in Fig. 3 operates in continuous mode and is controlled by the simple but effective PWM controller MC34063 operating at 100 kHz. Due to the open collector output a driver consisting of Q211/212 is used to drive a p-channel MOSFET. Peak current through Q209, D223 and L6 is 6.3A. Losses can easily be determined as already shown. Just the result is given here:

$$P_{Loss,Q209} = \underline{3.1W}$$

$$I_{Loss,D223} = \underline{2.4W}$$

Both devices need heatsinks having a thermal resistance of less than 25ºC/W.

6 Standby power supply

The flyback type power supply driven by the FSD210B generates not only the 5V output voltage but the supply for FAN4800 and FAN7382 as well. By means of OC2 the main power supply is completely switched off during standby and only this power supply still operates.

Principally there is nothing special about this power supply and it can be easily designed with the help of AN-4137 and the related spreadsheet or with the SMPS Design Tool [3] (http://www.fairchildsemi.com/designcenter/acdc/SMPSDT16_Install.zip). The actual design is for an output voltage of 5V and a current of 0.3A, but with the mentioned tool it is not an issue to change the design to a different output voltage and a power up to about 6W. Due to the use of the FOD2711BTV an output voltage down to 3.3V is no problem as well.

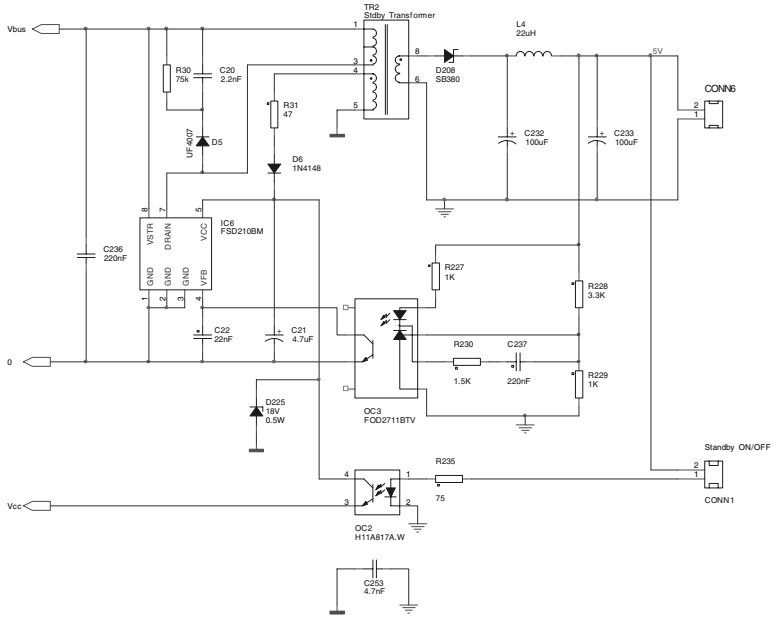

Figure 5: Schematic of Standby power supply

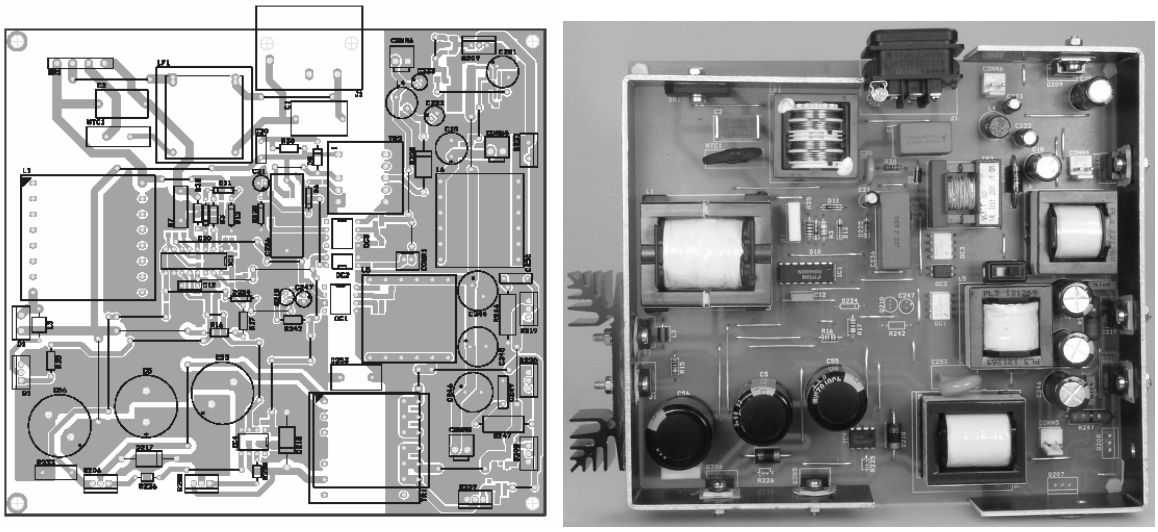

Figure 6: Layout and photo of finished board. Dimensions are 170mm x 156mm x 25mm (L x W x H)

7 PCB Layout and Mechanical Construction

In the literature [4] one will find layout rules for power electronics layout rules saying that the enclosed area of loops with high di/dt and the copper area of nodes with high dv/dt must be as small as possible. Both rules are intended to minimize EMI. Further, the source pin of Q1, the ground connection of R233, right hand side of R5 and ground pin of FAN4800 should be connected in form of a star in order to minimize the negative effect of common impedance coupling.

In practice there are the problems that the PCB will be larger for higher output powers and the power semiconductors have to be attached to big heatsinks. As a result, it is often not possible to make the loops as small as they should be, while combining the current density rules the copper area of traces and a real star would spoil the complete PCB. Therefore a PCB of a high power power supply sometimes is a compromise, especially in the case of a single sided PCB. The latter has been chosen for cost reasons.

If one takes a close look at the actual PCB, one will recognize that some of the less critical signals are not necessarily routed to the shortest path. This enables the large ground plane that emulates the star like connection. Moreover, using the minimum possible spacing between ground plane and hot signals (for reliability reasons this is about 2mm for the given voltage level), minimizes loops.

Again for cost reasons, a simple heatsink consisting of a sheet of aluminum with 2mm thickness, bent into the form of a 'U' has been used on primary and secondary side. Only Q1, which dissipates more power, needs an additional heatsink.

8 Test Results

A detailed test report is available for this board. Here three of the test results are shown.

8.1 Standby Power vs Input Voltage

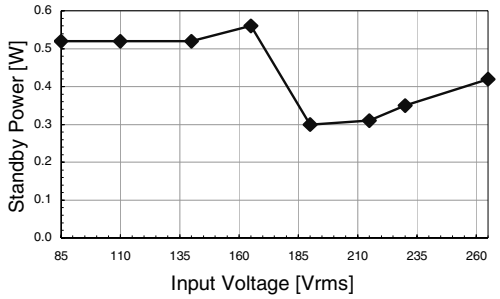

Figure 7: Standby Power versus input voltage

8.2 Full Load Efficiency vs Input Voltage

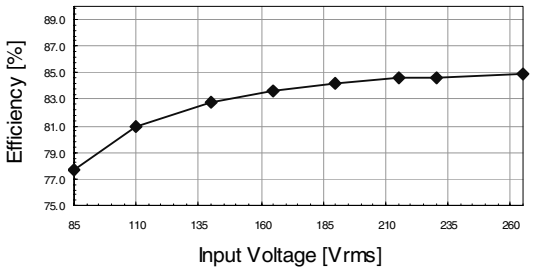

Figure 8: Efficiency versus input voltage

The efficiency is well above the projected 81% above $110V_{RMS}$. At smaller voltages, figures could be improved with a lower resistance EMI filter and by removing NTC1.

8.3 Power Switch and Diode Waveforms

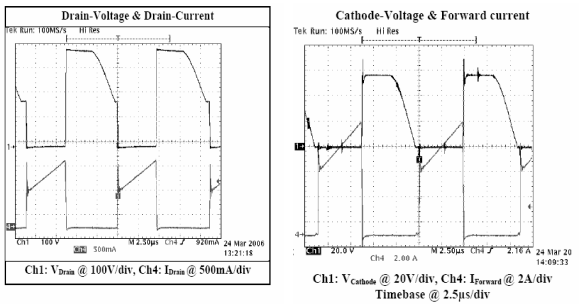

Figure 9: MOSFET and Diode waveforms

The left hand side of shows the drain current (red) and voltage (black) of Q212. From the current it is obvious the PSU works in CCM. The drain voltage is well clamped to the DC supply voltage when the MOSFET is turned off. After de-magnetization of the transformer the voltage starts to drop. The slope is determined by the resonance of the transformers magnetizing inductance and C_{DS} of the MOSFETs. By chance the drain voltage is close to minimum when the MOSFET is switched on, but this may differ from board to board due to the high tolerance (+/- 30%) of the magnetizing inductance.
The diode waveforms on the right hand side clearly show the parasitic oscillations when the diode turns off.

Dr. Michael Weirich

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APPENDIX

Figure A-1 Complete Schematic Diagram

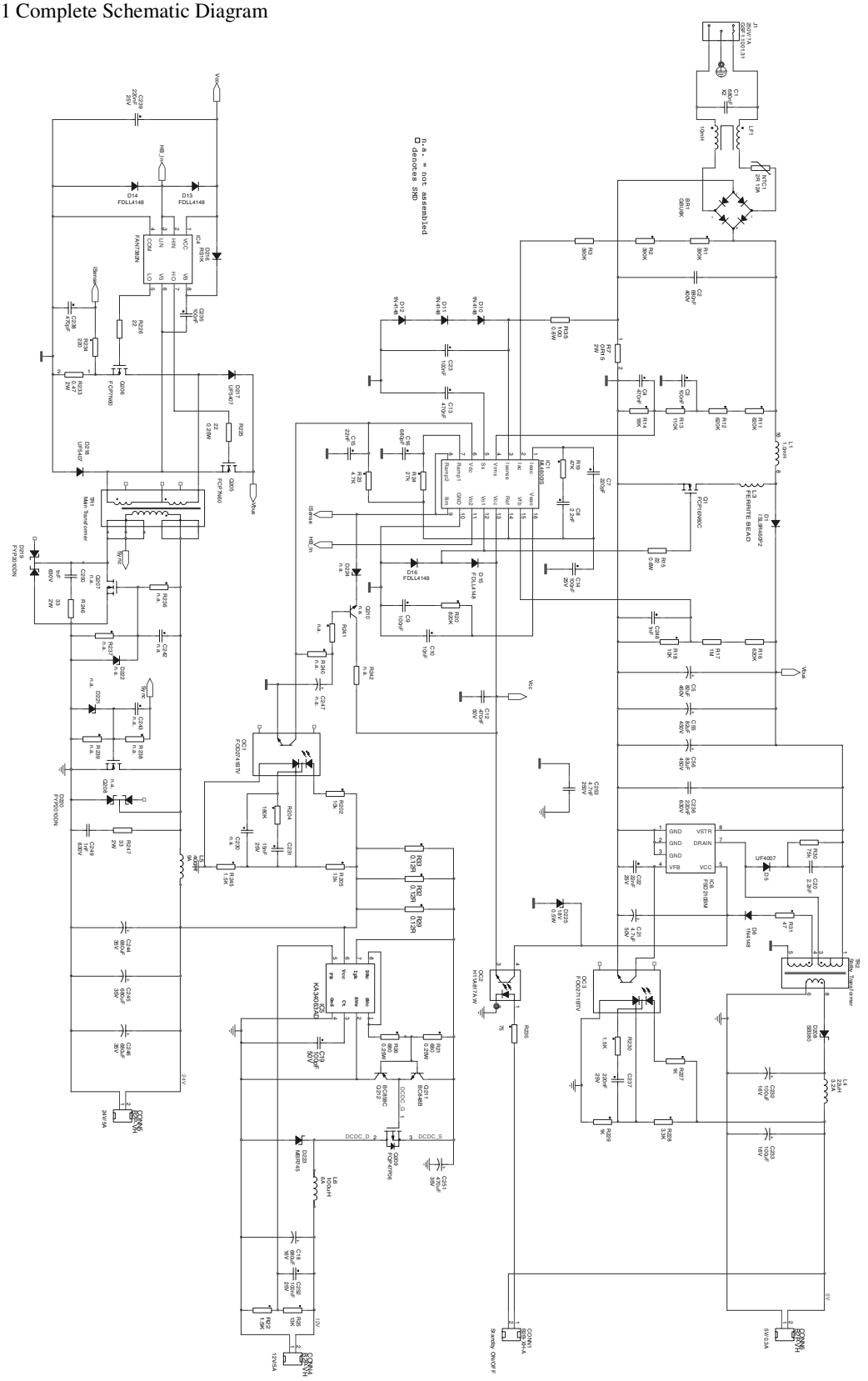


Table A-1: Bill of Materials

Item	Qty	Reference	Specification	Manufacturer/Type
1	1	BR1	GBU6K	Fairchild Semiconductor
2	1	CONN1	B2B-XH-A	JST XH Series
3	3	CONN4,CONN5,CONN6	B2P-VH	JST VH Series
4	1	C1	680nF \ 275V	EPCOS B32922 Series
5	1	C2	220nF \ 400V	EPCOS B32562 Series
6	1	C3	100nF \ 50V	AVX MLC X7R
7	1	C4	470nF \ 16V	AVX MLC X7R
8	3	C5,C55,C56	82uF \ 450V	Rubycon USG Series
9	1	C7	220pF \ 25V	AVX MLC X7R
10	1	C8	2.2nF \ 25V	AVX MLC X7R
11	5	C9,C14,C23,C235,C252	100nF \ 25V	AVX MLC X7R
12	1	C10	10nF \ 25V	AVX MLC X7R
13	1	C12	470nF \ 50V	KEMET CK06
14	1	C13	470nF \ 16V	AVX MLC X7R
15	2	C15,C22	22nF \ 25V	AVX MLC X7R
16	1	C16	680pF \ 25V	AVX MLC X7R
17	1	C18	680uF \ 16V	Nichicon PW Series
18	1	C19	100pF \ 50V	AVX MLC X7R
19	1	C20	2.2nF \ 1000V	Murata DE
20	1	C21	4.7uF \ 50V	SAMWHA SD
21	1	C230	n.a.	AVX MLC X7R
22	1	C231	15nF \ 25V	AVX MLC X7R
23	1	C232	100uF \ 16V	Nichicon PW Series
24	1	C233	100uF \ 16V	SAMWHA SD
25	1	C236	220nF \ 630V	Arcotronics R60 Series
26	2	C237,C239	220nF \ 16V	AVX MLC X7R
27	1	C238	470pF \ 25V	AVX MLC X7R
28	2	C242,C243	n.a.	AVX MLC X7R
29	3	C244,C245,C246	680uF \ 35V	Nichicon PW Series
30	1	C247	n.a.	SAMWHA SD
31	1	C248	1nF \ 25V	AVX MLC X7R
32	2	C249,C250	1nF \ 630V	Arcotronics R76 Series
33	1	C251	470uF \ 35V	Rubycon ZL Series
34	1	C253	4.7nF \ 250V	Murata DE Series
35	1	D1	ISL9R460P2	Fairchild Semiconductor
36	1	D5	UF4007	Fairchild Semiconductor
37	4	D6,D10,D11,D12	1N4148	Fairchild Semiconductor
38	4	D13,D14,D15,D16	FDLL4148	Fairchild Semiconductor
39	1	D208	SB380	Fairchild Semiconductor
40	1	D216	RS1K	Fairchild Semiconductor
41	2	D217,D218	UF5407	Fairchild Semiconductor
42	2	D219,D220	FYP2010DN	Fairchild Semiconductor
43	2	D221,D222	n.a.	
44	1	D223	MBR745	Fairchild Semiconductor
45	1	D224	n.a.	
46	1	D225	18V \ 0.5W	Fairchild Semiconductor
47	1	IC1	ML4800IS	Fairchild Semiconductor
48	1	IC4	FAN7382N	Fairchild Semiconductor
49	1	IC5	KA34063AD	Fairchild Semiconductor

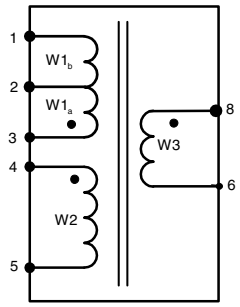
50	1	IC6	FSD210BM	Fairchild Semiconductor
51	1	J1	GSF1.1001.31	Schurter
52	1	LF1	2 x 10mH	EPCOS B82733 Series
53	1	L1	1.0mH	See Specification
54	1	L3	FERRITE BEAD	
55	1	L4	22uH	Coilcraft RFB0810
56	1	L5	40uH	See Specification
57	1	L6	100uH	See Specification
58	1	NTC1	2R	EPCOS
59	1	OC1	FOD2741BTV	Fairchild Semiconductor
60	1	OC2	H11A817A.W	Fairchild Semiconductor
61	1	OC3	FOD2711BTV	Fairchild Semiconductor
62	1	Q1	FCP16N60	Fairchild Semiconductor
63	2	Q205,Q206	FCP7N60	Fairchild Semiconductor
64	3	Q207,Q208,Q210	n.a.	
65	1	Q209	FQP47P06	Fairchild Semiconductor
66	1	Q211	BC848B	Fairchild Semiconductor
67	1	Q212	BC858C	Fairchild Semiconductor
68	2	R1,R2	390K \ 0.125W	Any
69	1	R3	390K \ 0.6W	Any
70	1	R7	0R15 \ 2W	Any
71	2	R11,R12	620K \ 0.125W	Any
72	1	R13	110K \ 0.125W	Any
73	1	R14	18K \ 0.125W	Any
74	1	R15	22 \ 0.6W	Any
75	1	R16	620K \ 0.6W	Any
76	1	R17	1M \ 0.6W	Any
77	2	R18,R202	10k \ 0.125W	Any
78	1	R19	47K \ 0.125W	Any
79	1	R20	820K \ 0.125W	Any
80	2	R21,R26	680 \ 0.25W	Any
81	3	R22,R230,R245	1.5K \ 0.125W	Any
82	1	R23	4.7K \ 0.125W	Any
83	1	R24	27k \ 0.125W	Any
84	2	R25,R205	13k \ 0.125W	Any
85	3	R29,R32,R33	0.12R \ 1W	Any
86	1	R30	75k \ 0.6W	Any
87	1	R31	47 \ 0.125W	Any
88	1	R35	100 \ 0.6W	Any
89	1	R204	180K \ 0.125W	Any
90	2	R225,R226	22 \ 0.25W	Any
91	2	R227,R229	1K \ 0.125W	Any
92	1	R228	3.3K \ 0.125W	Any
93	1	R233	0.47 \ 2W	Any
94	1	R234	220 \ 0.125W	Any
95	1	R235	75 \ 0.125W	Any
96	6	R236,R237,R238,R239,R240,	n.a. \ 0.125W	Any
97	1	R242	n.a. \ 0.6W	Any
98	2	R246,R247	33 \ 2W	Any
99	1	TR1	Main Transformer	See Specification
100	1	TR2	Stdby Transformer	See Specification

1 Table A-2: Specifications for wound components

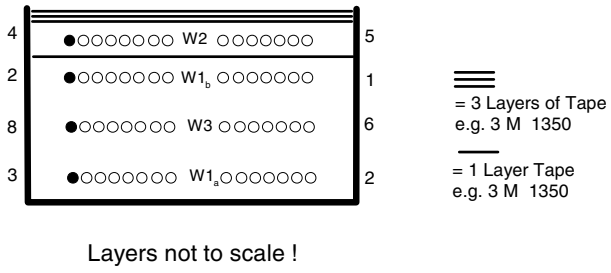
1.1 Standby Transformer Specification

1.1.1 Winding Details

Name	Pins (Start →End)	# of Layers	Strands x Wire ø	Turns	Construction	Material
W1a	3 →2	2	1 x 0.15 mm	91	spaced winding	CuLL
W3	8 →6	1	1 x 0.5 mm	8	spaced winding	Triple insulated
W1b	2 →1	2	1 x 0.15 mm	91	spaced winding	CuLL
W2	4 →5	1	1 x 0.15 mm	24	spaced winding	CuLL



Schematic



Construction

1.1.2 Electrical Characteristics

Parameter	Pins	Specification	Conditions
Primary Inductance	1 → 3	5.85 mH +/- 5%	10kHz, 100mV, all secondaries open
Leakage inductance	1 → 3	290 uH maximum	10kHz, 100mV, all secondaries short

1.1.3 Core and Bobbin

Core:	EF 20
Material:	FI325 (Vogt) or equivalent
Bobbin:	EF20 / 10 Pin / Horizontal / Increased creepage
Gap in center leg:	approx. 0.2 mm for A_L of 177 nH/Turns^2

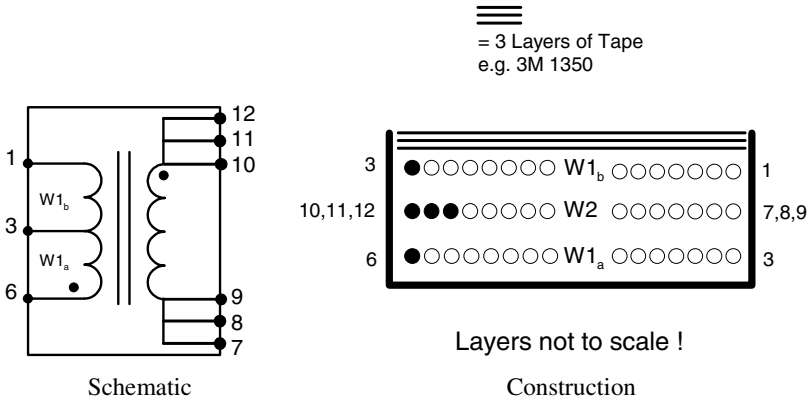
1.1.4 Safety

High voltage test: 3000V_{rms} for 1 minute between primary (pins 1 to 5) and secondary (pins 6 to 8)

1.2 Main Transformer Specification

1.2.1 Winding Details

Name	Pins (Start →End)	Layers	Strands x Wire ø	Turns	Construction	Material
W1a	6 →3	1	1 x 0.5 mm	39	perfect solenoid	CuLL
W3	10,11,12 →7 ,8,9	2	3 x 0.7 mm	11	perfect solenoid	Triple insulated
W1b	3 →1	1	1 x 0.5 mm	38	perfect solenoid	CuLL



Schematic Construction

1.2.2 Electrical Characteristics

Parameter	Pins	Specification	Conditions
Primary Inductance	1 → 6	13 mH +/- 30%	10kHz, 100mV, all secondaries open
Leakage Inductance	1 → 3	500 uH maximum	10kHz, 100mV, all secondaries short

1.2.3 Core and Bobbin

Core: EER2834
Material: PC40 (TDK) or equivalent
Bobbin: EER2834 / 12 Pin / Horizontal e.g. Pin Shine P-2809
Gap in center leg: 0 mm

1.2.4 Safety

High voltage test: 3000V_{rms} for 1 minute between primary (pins 1 to 6) and secondary (pins 7 to 12)

1.3 PFC Choke

1.3.1 Winding Details

Name	Pins (Start →End)	Layers	Strands x Wire ø	Turns	Construction	Material
W1	8 →16	6	3 x 0.5 mm	124	perfect solenoid	CuLL

1.3.2 Electrical Characteristics

Parameter	Pins	Specification	Conditions
Inductance	8 → 16	1000 uH +/- 5%	10kHz, 100mV

1.3.3 Core and Bobbin

Core: EER3542
Material: PC40 (TDK) or equivalent
Bobbin: EER3542 / 16 Pin / Horizontal e.g. Pin Shine P-3508
Gap in center leg: aprox. 2.0 mm for an A_L of 65 nH/Turns^2

1.4 Choke 40uH / 9A (L5)

1.4.1 Winding Details

Name	Pins (Start →End)	Layers	Strands x Wire ø	Turns	Construction	Material
W1	1,2,3,4,5 →8,9,10,11,12	6	5 x 0.71 mm	15	perfect solenoid	CuL

1.4.2 Electrical Characteristics

Parameter	Pins	Specification	Conditions
Inductance	1 → 5	40 uH +/- 5%	10kHz, 100mV

1.4.3 Core and Bobbin

Core: EER2828
Material: PC40 (TDK) or equivalent
Bobbin: EER2828 / 12 Pin / Horizontal e.g. Pin Shine P-2816
Gap in center leg: approx. 0.4 mm for an A_L of 230 nH/Turns^2

1.5 Choke 100uH / 6A (L6)

1.5.1 Winding Details

Name	Pins (Start →End)	Layers	Strands x Wire ø	Turns	Construction	Material
W1	1,2,3,4,5 →8,9,10,11,12		5 x 0.56mm	25	perfect solenoid	CuL

1.5.2 Electrical Characteristics

Parameter	Pins	Specification	Conditions
Inductance	1 → 5	100 uH +/- 5%	10kHz, 100mV

1.5.3 Core and Bobbin

Core: EER2828
Material: PC40 (TDK) or equivalent
Bobbin: EER2828 / 12 Pin / Horizontal e.g. Pin Shine P-2816
Gap in center leg: aprox. 0.45 mm for an A_L of 205nH/Turns^2