7 SURFACE MOUNTING OF COMPONENTS

7.1 Surface Mount Device Lead Forming Leads **shall [D1D2D3]** be formed in such a manner that the lead-to-body seal is not damaged or degraded (see Figures 7-1 and 7-2). When lead forming is required during the assembly process leads **shall [D1D2D3]** be formed such that there is an available minimum lead length for contact to the solder land as shown in Table 7-1.

The leads of surface mounted components **shall [D1D2D3]** be formed to their final configuration prior to soldering.

Note: Where severe loading conditions exist such as Coefficient of Thermal Expansion (CTE) mismatches or severe operational environments, extra consideration should be given to the minimum available contact length.

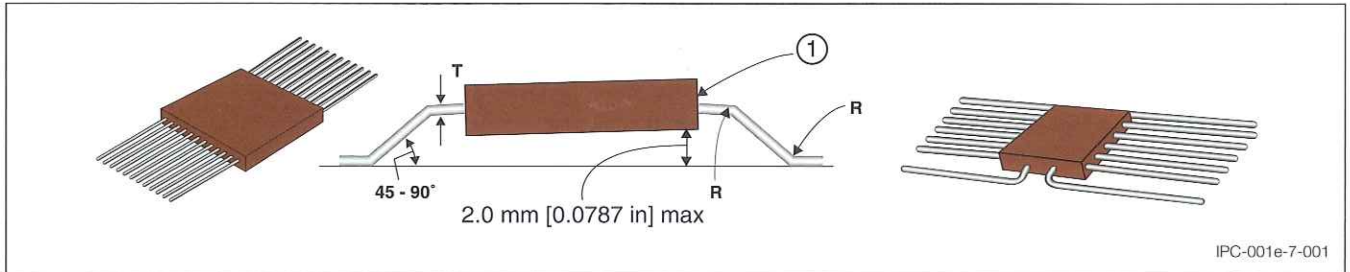

Figure 7-1 Surface Mount Device Lead Forming
1. No bend into the seal

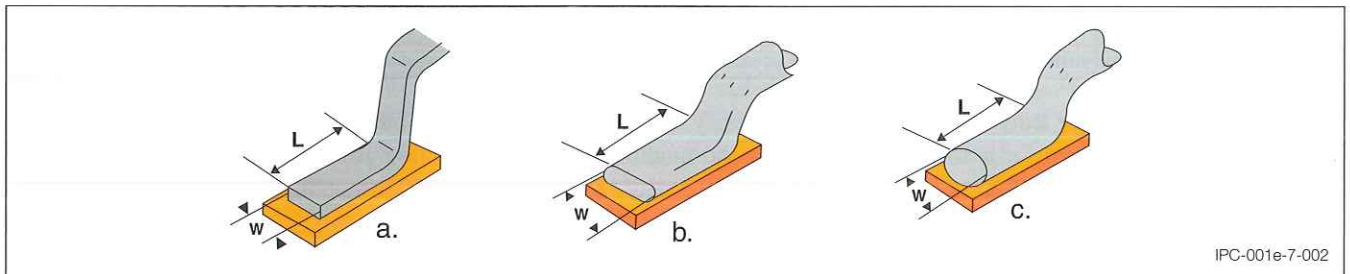

Figure 7-2 Surface Mount Device Lead Forming

Table 7-1 SMT Lead Forming Minimum Lead Length

a. One lead width for flat leads.
b. Two lead widths for coined leads.
c. Two lead diameters for round leads.

7.1.1 Lead Deformation Limits Whether leads are formed manually or by machine or die, parts or components **shall not [D1D2D3]** be mounted if the part or component lead has nicks or deformation exceeding 10% of the diameter, width, or thickness of the lead except as allowed for flattened leads (see 7.1.4). Exposed basis metal is acceptable if deformation does not exceed 10% of the diameter, width, or thickness of the lead.

Lead deformation (unintentional bending) may be allowed provided:

a. There **shall [D1D2D3]** be no evidence of a short or potential short existing.

b. The lead-to-body seal or weld **shall not [D1D2D3]** be damaged by the deformation.

c. The minimum electrical clearance **shall not [D1D2D3]** be violated.

d. The top of the lead should not extend beyond the top of the component body, except for preformed stress loops.

e. If present on ends, toe curl should not exceed two times the thickness of the lead.

7.1.2 Flat Pack Parallelism Leads on opposite sides of surface mounted flatpacks should be formed such that the nonparallelism between the base surface of the component and the surface of the printed board (i.e., component cant) is minimal. Component tilt is permissible; however, the final configuration should not exceed the clearance limit of 2.0 mm [0.0787 in] (see Figure 7-1).