

# FSF-AD8200A 8-Channel, 185MSPS JESD204B ADC FMC

# **Quick Start Guide**

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# **Revision History**

Revision	Author	Release Date	Description of Change
0.1	EJD	2013.12.18	First Draft
0.2	EJD	2013.12.19	Updated for Vivado <sup>®</sup> 2013.2
1.0	ST	2014.01.21	Updated. Released.

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# Glossary

Term	Definition
CLI	Command Line Interface. A simple text-based interface that allows a user to read and write register values, enabling hardware target operation and experimentation.
FMC	FPGA Mezzanine Card (VITA 57.1). A small board that plugs into an FMC connector, such as on the VC707 evaluation board. These daughter boards usually add functions that are too specialized to be included on a general purpose evaluation board. Often they are input/output boards. Examples include input boards for video sampling and compression, or output boards for motor control.
JESD204B	A high-speed data transfer standard primarily targeted at data converters. The analog- to-digital chips on the FSF-AD8200A FMC transfer their digitized data to the FPGA using the JESD204B physical layer and protocol. Xilinx provides a JESD204B IP core targeted at their programmable devices. The FSF-AD8200A demonstration bitfile contains an instantiation of the Xilinx JESD204B IP core.
ILA	Integrated Logic Analyzer. An ILA is inserted into a Xilinx FPGA design using the Vivado design tool from Xilinx. During debug or experimentation, the ILA can then be triggered to capture data. This data can then be shown graphically or exported for post-processing on a PC. ILA is similar to Xilinx's previous Chipscope™ offering.
Tera Term PRO	Tera Term PRO is a good quality, free, terminal emulator program. It is the example terminal emulator referred to in both this guide as well as the VC707 documentation.
Vivado®	Xilinx tool enabling FPGA design, programming, and debug.
VC707	A Virtex-7 <sup>®</sup> Development Kit sold by Xilinx <sup>®</sup> , containing a Virtex-7 FPGA and other hardware; containing two FMC connectors (FMC1 and FMC2).

# 1. INTRODUCTION

#### 1.1 Document Purpose

This document provides step-by-step instructions enabling customers to evaluate and experiment with the FSF-AD8200A FMC when mated with a VC707 Development Kit. By following this guide, the user will be able to evaluate and experiment with the FSF-AD8200A culminating in the capture of analog signals. Following capture, the user may decide to export the digitized waveform for post-processing in the signal processing tool of their choice.

This document and the demonstration code provided by Fidus assumes the following:

- a) The Host platform is a VC707
- b) The Host PC is a Windows system
- c) Xilinx Vivado 2013.2 is installed correctly and will be used on the Host PC
- d) Tera Term PRO is installed correctly and will be used on the Host PC
- e) The end user has copied the FSF-AD8200A Project Directory to the Host PC. For the purposes of the demonstration, a directory called "work" was created. An empty Xilinx project was then placed under the "work" directory. This empty Xilinx project directory is provided by Fidus. No source or other files are provided, the directory simply allows a Hardware Session to be opened, which allows the user to download the FPGA bitfile and use the ILA cores to extract and view graphed results. The source files for FPGA software and hardware are not provided.

# 2. STEP-BY-STEP GUIDE

#### 2.1 Connect FSF-AD8200A FMC to VC707 carrier card

- 1. Ensure that the VC707 PCB is powered-down, and that you have exited Vivado and Tera Term.
- 2. Ensure that the JTAG cable and the Serial-over-USB cables are connected between the VC707 and the Host PC. For more information refer to Xilinx's VC707 manuals.
- 3. Plug the FSF-AD8200A card onto the VC707's J37 HPC2 connector. The bitfile will not work if the FMC is plugged into the wrong FMC connector. Ensure the card is fully mated. Since the FSF-AD8200A will hang off the edge of the VC707, you may want to relieve stress on the FMC connector by supporting the weight of the FMC card (beyond the scope of this document).
- 4. Inspect your setup. If all looks correct. Turn the VC707 power switch ON.

#### 2.2 Configure the host PC to create a virtual COM port, running over USB.

Refer to Xilinx's documentation for specific instructions on establishing a virtual COM port to connect to the VC707. For this guide, we assume that all necessary drives are already installed, and that COM5 is configured as the virtual COM port. Note: This document uses COM5 as an example, but the actual COM number will be assigned by the Host PC, and will likely not be COM5.

### 2.3 Launch Tera Term Pro



#### 2.4 Configure Tera Term PRO "New Connection"

After launch, Tera Term will ask for new connection details. Select the "SERIAL" radio button and using the "Port:" pulldown menu, find, and then select, the entry that mentions "Silicon Labs USB to UART bridge". This will be your virtual COM port. In this example, the virtual COM port was established as COM5. Click "OK".

Í	🚇 Tera Term - [o	lisconnected] VT	0.8	S		-		- 0	23	
1	File Edit Setu	Tera Term: New c	onnection				×			
		© TCP/IP	Host:	myhost.exa	imple.com		-		Î	
	1			☑ History ● Telnet ● SSH	TCP port SSH version:					
		Serial	Port:	O Other	Protocol: (		-			
			OK	COM3: Intel COM4: USB	munications Port (R) Active Manag Serial Port (COM con Labs CP210×	ement Teo 4)	107.	88 8	à ô	
L		-				<b>N</b>				

#### 2.5 Configure Tera Term PRO Serial Port

On the top menu, click on the SETUP menu item, this will open a pulldown menu, select "SERIAL PORT..." This menu allows you to configure your serial port interface.

File Edit	Setup Control Window H	elp
	Terminal Window Font Keyboard	
	Serial port	
	Proxy	
	SSH	
	SSH Authentication	
	SSH Forwarding	
	SSH KeyGenerator	
	TCP/IP	
	General	
	Additional settings	+
U	Save setup Restore setup	S: SIIICON LADS CP2TUX USE to UART BRIDGE (CUMS)
24 BPP	Load key map	3 KB Not a fil

Configure the Serial Port to be 8-N-1, with a baud rate of 115200. In the "Flow control" pulldown, select Xon/Xoff. Set the transmit delay to be zero for lines and characters.

Port:	COM5 -	ОК
Baud rate:	115200 👻	
Data:	8 bit 🔹	Cancel
Parity:	none 🔻	
Stop:	1 bit 🔹	Help
Flow control:	Xon/Xoff	\$
Transmit dela	y	

Click "OK". Your terminal is now properly configured.

#### 2.6 Launch Vivado 2013.2

Launch Vivado 2013.2 by clicking on its desktop icon (or from Windows "Start" menu).

Recycle Bin	Cygwin64 Terminal	Vivades 2015.2
<b>?</b>	6	

### 2.7 Ignore the warning that 2013.2 has been superseded.

This warning is a normal message simply advising you that more recent versions of Vivado are now available. Ignore the warning by clicking on "CLOSE".

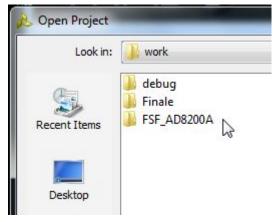
VIVADC	2013.2				
	💫 XilinxNotify - Available Updates			×	
	Ge Product Updates	Installed Version	Available Version	Show Message	
	Vivado Design Suite 2013.3 available for download	2013.2	2013.3	<b>V</b>	
	Item Details * IP enhancements: sharing clocking reset reso	purces for IP, access to GT	debug ports, detailed	change log.	-
	<u>UltraFast Design Methodology</u> : This release em as well as HDL and XDC templates for correct	t-by-construction designs.			
onsole	Partial Reconfiguration enables greater usage o also result in lower power consumption and en Kintex-7, Virtex-7 and Zynq.				-
	Internet	Settings More Info	Download	Close	

### 2.8 Open the Empty Project

In the FILE menu, click on OPEN PROJECT.

File	Tools Window Help	_	1
æ	New Project	_	
•	Open Project		
	Open Recent Project	•	
	Open Example Project	•	2013.2
	Open Checkpoint		
	Open Recent Checkpoint	×	
	Open Hardware Session		L
	New IP Location		Getting Star
	Open Recent IP Locations	Þ	
	Exit		Cr Cr
			Nev of s

Assuming you installed the FSF\_AD8200A Empty Project directory in your C:\work directory, go to that directory and click on it.

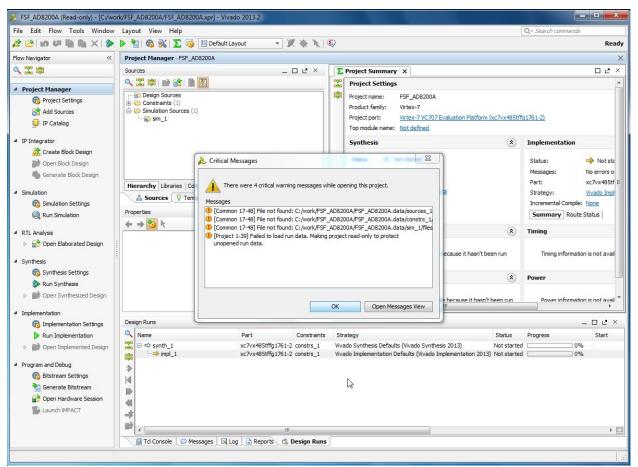


Then click on the FSF\_AD8200A.xpr file to load this empty project into Vivado 2013.2.

Look in	FSF_AD8	200A	
Ca.	J. Xil		
Recent Items	scustomer_release		
Recent runs	FSF_AD8200A.cache FSF_AD8200A.hw		
Desktop	SF_AD82	2007	
- controp			
1			
My Documents			
	File name:	FSF_AD8200A.xpr	
	Files of type:		

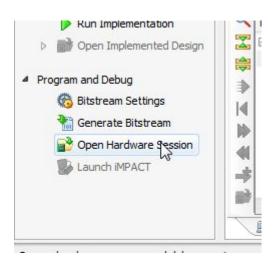
#### 2.9 Ignore warnings from Empty Project in Vivado

Warnings may appear. Click on "OK" to ignore them.



#### 2.10 Open a Hardware Session

Look in the bottom left corner of the Vivado screen and click on "Open Hardware Session".



#### 2.11 Select a Target

The hardware session will open, now the user must connect it to a target. If this is your first run, click on "Open a new hardware target". Otherwise, click on "open recent target".

KF_AD8200A (Read-only) - [C:/wor	rk/FSF_AD8200A/FSF_AD8200A.xpr] - Vivado 2013.2
File Edit Flow Tools Window	Layout View Help
🯄 😂 i in 🕫 🐚 🐘 X i 🗞	🕨 📸   🍪 💥   ∑ 🚳 😬 Default Layout 🔹 🗶 🔌 🔭   🧐
Flow Navigator «	Hardware Session - unconnected
🔍 🛣 🖨	(i) No hardware target is open. Open recent target Open a new hardware target
<ul> <li>Project Manager         <ul> <li>Project Settings</li> <li>Project Settings</li> <li>Add Sources</li> <li>IP Catalog</li> </ul> </li> <li>IP Integrator         <ul> <li>IP Integrator</li> <li>Create Block Design</li> <li>Open Block Design</li> <li>Generate Block Design</li> </ul> </li> </ul>	Hardware   Image: Comparison of the second

The actual target name will appear similar to "localhost:60001..224A". Think of it as the software driver which talks to the FPGA.

🚴 FSF_AD8200A (Read-only) - [C:/wo	ork/FSF_AD8200A/FSF_AD8200A.xpr] - Vivado 2013.2			
File Edit Flow Tools Window	Layout View Help			
🯄 🔁 🗠 🕫 🐚 🐘 🗙 🔇 🗞	🕨 🚵   🍪 💥   ∑ 🇔 🔛 Default Layout 🛛 👻 💥 🔌 🍾   🎨			
Flow Navigator «	Hardware Session - unconnected			
Q 🔀 🚔	() No hardware target is open. Open recent target Open a new hardware target			
<ul> <li>Project Manager         <ul> <li>Project Settings</li> <li>Add Sources</li> <li>IP Catalog</li> </ul> </li> <li>IP Integrator         <ul> <li>Create Block Design</li> <li>Open Block Design</li> </ul> </li> </ul>	Hardware			

Once the hardware target is open, you will see the particular Xilinx Virtex<sup>®</sup> device on the VC707 board. It is called "xilinx\_tcf/..." Usually it first is reported as "Closed". If you used it recently, it may be reported as "Open".

File Edit Flow Tools Wind	ow Layout View Help 🖻 🕨 🚵   🍪 💥   ∑ 🧔 😐 De	efault Layout 🔹 🗶
-low Navigator	Kardware Session - localhost/xilin	nx_tcf/Digilent/210203339224A
2 🖀	(i) No hardware target is open. Q	pen closed target Open recent t
Project Manager     Roject Settings	Hardware <hr/> <hr/> <h< td=""><td>_ D &amp; ×</td></h<>	_ D & ×
Add Sources	Name	Status
	□· Iocalhost (1)	Connected 3339224A (0) Closer
<ul> <li>IP Integrator</li> <li>Create Block Design</li> <li>Open Block Design</li> <li>Generate Block Design</li> </ul>		13

Right click on the word in the Status column ("Closed" or "Open"), to open the menu, and select "Open Target".

💫 FSF_AD8200A (Read-only) - [C:/wo	rk/FSF_AD8200A/FSF_AD8200A.xpr] - Vivado	o 2013.2	
File Edit Flow Tools Window	Layout View Help		
🯄 🖄 🕼 🕫 🗎 🖬 🗙 💊	🕨 🐮   🍪 💥   ∑ 🎼 📴 Default Lay	rout	• 🗶 🔌 🖹 💿
Flow Navigator «	Hardware Session - localhost/xilinx_tcf/Dig	gilent/2102033	39224A
	(i) No hardware target is open. Open close	d target Ope	en recent target Open a new hardware target
Project Manager     Proiect Settings	Hardware	_ 🗆	12 ×
Project Hallager     Roject Settings     Strand Add Sources	Name	Status	
IP Catalog	⊡ localhost (1)	Connect	ed
	ill ⊘ xilinx_tcf/Digilent/210203339224/	A (U) 🖬 🚳	Hardware Target Properties Ctrl+E
<ul> <li>IP Integrator</li> <li>Create Block Design</li> <li>Open Block Design</li> <li>Generate Block Design</li> </ul>		ø	Set as Current Target Refresh Target Close Target
Generate block Design			Open Target
<ul> <li>Simulation</li> </ul>			Export to Spreadsheet
🔞 Simulation Settings	Hardware Target Properties	_ 0	e ×

This will declare the target driver xilinx\_tcf/...224A to be "Open". It will also report that one FPGA is present: XC7VX485T\_0. If the FPGA was recently used, it may still be reported as "Programmed", otherwise it will state "Unprogrammed".

#### 2.12 Program FPGA

Right-click under the Status column (on "Programmed" or "Unprogrammed") to bring up the menu and select "Program Device...".

💫 FSF_AD8200A (Read-only) - [C:/w	ork/FSF_AD8200A/FSF_AD8200A.xpr	] - Vivado 2013.2	
File Edit Flow Tools Window	v Layout View Help		
🯄 🖻   10 🕫 🗎 🖿 🗙   👂	• 🕨 🐮   🍪 🐝   🔽 🍯 😑	efault Layout 🛛 🔻 💓 🗞 🕅	
Flow Navigator 🛛 🔍	Hardware Session - localhost/xili	nx_tcf/Digilent/210203339224A	
🭳 🛣 🚔	() There are no debug cores. Pro	gram device Refresh device	
4. Duringt Manager	Hardware	_ 🗆 🖒 ×	
<ul> <li>Project Manager</li> <li></li></ul>	< Z ⇔ E > > ■		
Add Sources	Name	Status	
IP Catalog	□· localhost (1) □· Ø xilinx_tcf/Digilent/2102	Connected 03339224A (1) Open	
▲ IP Integrator	XC7VX485T_0 (0) (a		I+E
Create Block Design		Assign Programming File	
Dpen Block Design		Program Device	
🌑 Generate Block Design		@ Refresh Device	
<ul> <li>Simulation</li> </ul>		Export to Spreadsheet	
Simulation Settings			

A dialog will open asking what bitstream file to send to the target device.

Select b	itstream file for de	vice XC7VX485T_0		
Parameters				
Bitstream file:	1			
			Specify B	itstream Fi
	Program	Cancel		

Click on the "..." button, and navigate the directories to select "FSF\_AD8200A/customer\_release/datafiles/download.bit". Click "OK".

#### FSF-AD8200A Quick Start Guide

Look in:	) datafiles		-	🦻 🚳 🗐 🖡	🗙 💁 💷 -	
Recent Items	download	d.bit	Recent Directories			•
	File name:	download	l bit			OK

The previously selected path and file returns to the prior dialog. Click "PROGRAM".

	tstream file for device XC7VX485T_0.
Parameters Bitstream file:	mer_release/datafiles/download.bit 🕥 💮

The programming of the FPGA begins. A status bar will indicate percent complete as the download.bit file configures the FPGA. The total download time can vary, but generally, it takes about 30 seconds.

Hardware Session - localhost/xilinx_tcf/Digilent/	210203339224A	
There are no debug cores. Program device F	<u>Refresh device</u>	
Hardware	2 ×	
< 🔀 🖨 🛃 🕨 🕨 🔳		
Name	Status	
	Connected	
xilinx_tcf/Digilent/210203339224A (1) XC7VX485T_0 (0) (active)	Open Programmed	
	Contract Annual Million and	
Hardware Device Properties		
🖕 🛶 🛐 🔈 Program Device		×
XC7VX485 Programming the device	_	Cancel
	_	 Cancel

#### 2.13 Observe Command Interface Start

If you switch to the terminal program during programming, you will observe that after programming the initial Command> prompt is displayed by the command interface.

Command Interpreter program commencing	
FPGA Hardware Version # 0x0000000A Build Date: unknown Build Time: unknown Build Tag: NONE FSF-AD8200A Finale Command Interpreter Version # 0x00ED0101 Build Date: 2013/Dec/10 Build Time: 1:42 pm EST Build Tag: NONE	
Miscellaneous Information: SILENT_MODE : 0 USE_XON_XOFF : 1 USE_WORD_ADDRESSES_FOR_JESD : 0 read_data_values_checked : 0 accumulated_mismatches : 0	
For help in Finale DEBUG Command interpreter type "help" (no quotes). Command>	-

#### 2.14 Confirm that Vivado recognizes the ILA cores

Once programmed, Vivado will report that it 'sees' two ILA cores within the FPGA: hw\_ila\_1 and hw\_ila\_2. Both report as IDLE, meaning neither has been triggered.

and the second se				– 🗆 🖻 ×
🗙 😂 🖪 N				
lame		Status		
🛛 📕 localhost (1)		Connected		
	/Digilent/2102033392			
E 🔊 XC7VX4	485T_0 (2) (active)	Programmed		
iw_i		◯ Idle		
lardware Device Pro	perties			_ 🗆 🖻 ×
+ + 🔁 🗟				
XC7VX485T_0				
Name:	XC7VX485T_0			
Part:	XC7VX485T			
ID code:	33687093			
IR length:	6			E
📝 Is programmabl	e			
Programming file:	C:/work/FSF_AD	8200A/customer_relea	ase/datafiles/downloa	d.bit
Probes file:				
User chain count:	4			
General Propertie	es			

#### 2.15 (Optional Step) Attempt to Capture Data with ILA Cores

For completeness, this optional step is intended to demonstrate the error message the user will receive if the user tries to capture data before loading the probes file. Feel free to proceed directly to section 2.17 if so desired.

While hovering over the "Idle" word under the Status column (for either ila\_0 or ila\_1), right-click to bring up the menu. Click on "Run Trigger".

Hardware Session - localhost/xilinx_tcf/Digiler	nt/2102033	39224A
Hardware		_ 🗆 🕑 ×
🔍 🔀 🖨 🛃 🕨 🕪 🔳		
Name	Status	
🖃 🚪 localhost (1)	Connect	ted
📄 📓 🤌 xilinx_tcf/Digilent/210203339224A (	1) Open	
🖻 🚸 XC7VX485T_0 (2) (active)	Program	med
<mark>i2 hw_i</mark> la_1 <sup>i</sup> …a∰ hw_ila_2		ILA Core Properties Ctrl+E
		Run Trigger
ILA Core Properties		Stop Trigger
	DD	Run Trigger Immediate
← → ○○		Export to Spreadsheet

# 2.16 No ILA Probes Detected Error Message

This error message indicates that there are no probes defined. This indicates that Vivado has not yet been told how to interpret the data coming from the ILA cores.

Run Trigger	x
No ILA probes detected. You may need to refresh th	ne device before executing command: Run Trigger
Don't show this dialog again	
	OK Cancel

#### 2.17 Define a Probes File

Fix this problem by telling Vivado what probes are available. Under the box where the programming file is defined, a second box is available to define the probes file.

Hardware			_ 🗆 🕑	2
🤍 🔀 🖨 🖪 🕨	▶ 🔳			
Name		Status		
🗄 🚦 localhost (1)		Connected		
	/Digilent/210203339224A (1)	Open		
	485T_0 (2) (active)	Programmed		
bw_i ≣ hw_i ∎ hw_i		◯ Idle 6		
	IG_2			
ial uwale Device Pro	perdes		- 0 2	
← → 🚱 🕅				
← → 🚱 🦻	XC7VX485T_0			
XC7VX485T_0 Name: Part:				
★ → ∑   XC7VX485T_0 Name:	XC7VX485T_0			
XC7VX485T_0 Name: Part:	XC7VX485T_0 XC7VX485T			
<pre>xC7VX485T_0 Name: Part: ID code:</pre>	XC7VX485T_0 XC7VX485T 33687093 6			
XC7VX485T_0 Name: Part: ID code: IR length:	XC7VX485T_0 XC7VX485T 33687093 6	ustomer_release/datafi		
XC7VX485T_0 XC7VX485T_0 Name: Part: ID code: IR length: Is programmab	XC7VX485T_0 XC7VX485T 33687093 6	ustomer_release/datafi		

Click on the "..." button next to the Probes File box, and navigate up and over to select the "debug\_nets.ltx" file in the customer\_release/datafiles directory.

lardware Device Pro	perties	
+ → 🗞 🕅		
XC7VX485T_0		
Name:	XC7VX485T_0	<u>×</u>
Part:	XC7VX485T	
ID code:	33687093	
IR length:	6	E
🗸 Is programmabl	e	
Programming file:	C:/work/FSF_AD8200A/customer_release/datafiles/download.bit	
Probes file:	C:/work/FSF_AD8200A/customer_release/datafiles/debug_nets.ltx	
User chain count:	4	

#### 2.18 Refresh the Device

The user must now REFRESH the device to tell Vivado that a probes file has been defined. Hover over the word "Programmed" next to the device listing (XC7VX485T...). Right-click and select "Refresh Device".

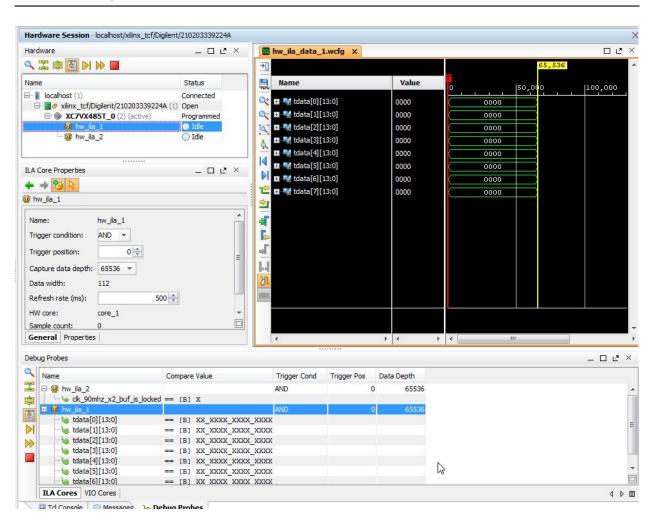
ardware				_ 🗆 🖻	×		
、 🛛 🖨 🖪 🕨 🖉	▶ 🔳						
Name							
- localhost (1) ⊡ ∭ ∕ xilinx_tcf/Dig	ilent/210203339224A (1)	Connec Open	ted				
E 🗞 XC7VX48		Progra		Underson Desides Descention	Ctrl+E		
				Assign Programming File	CUITE		
				Program Device			
Hardware Device Properties				Run Trigger			
XC7VX485T_0			DD	Stop Trigger Run Trigger Immediate			
Name: XC7VX485T 0			ø	Refresh Device			
Part:	 XC7VX485T			Export to Spreadsheet			
ID code:	33687093		-				
IR length:	6						
✓ Is programmable					111		
Programming file:	C:/work/FSF_AD8200A/customer			ase/datafiles/download.bit 💿 💮			
Probes file:	C:/work/FSF_AD8200A/c	ustomer	_rele	ase/datafiles/debug_nets.ltx 🕥 📖	1.00		
User chain count:	4			-			

Immediately after the refresh, the various Debug Probes will be visible in the bottom window. Vivado and ILA are now ready to capture data.

#### 2.19 (Optional Step) Capture Static Data using ILA Core

For completeness, this optional step demonstrates the results of capturing data without first running INIT (configuring the registers on the FSF-AD8200A). If desired, this step may be skipped and the user can proceed directly to section 2.21.

Now that ILA has been set-up, clicking trigger will capture 8 channels of data instead of resulting in an error. The captured data is shown in the waveform display. 64K samples are recorded for each of the 8 channels. In the example below, the data is completely static, this is because the FSF-AD8200A has not yet been configured for operation.



## FSF-AD8200A Quick Start Guide

# 2.20 Observing the Clock is not Initialized

Triggering on hw\_ila\_2 reveals a problem- the JESD204B IP core clock is not locked. This result highlights that the FPGA is not receiving a clock reference from the FSF-AD8200A.

Hardware	_ 🗆 🖻 ×	hw ila data 1.wc	fg 🗙 🔚 hw_ila_data_2	.wcfg X	_ L
< 🔀 🖨 🛃 🕨 🕨 🔳		₹0			65,53
Name	Status	Name Name	Value		50,000
	Connected Open Programmed Idle	Qt         U <sub>i</sub> ck_90mhz_           Qt         N           Qt         N           Qt         N           Qt         N	x2_buf_is_locked 0		
ILA Core Properties		<ul> <li>▼</li> <li>↓</li> <li>↓</li></ul>			
Name:     hw_ila_2       Trigger condition:     AND ▼       Trigger position:     0 ♀       Capture data depth:     65536 ▼	E	<b>*</b> •			
Data width:         1           Refresh rate (ms):         500 ≜√           HW core:         core_2           Sample count:         0	- -	<u>21</u>			
General Properties					

#### 2.21 Using the command interface to Initialize the System

Within the terminal session, type "init" to initialize the FSF-AD8200A card.

Once <enter> is pressed, a long sequence of commands will be sent from the FPGA to both the FSF-AD8200A card and to the JESD204B receiver IP core within the FPGA. This list of commands is available within an appendix in the FSF-AD8200A User Manual.

#### FSF-AD8200A Quick Start Guide

		- Tera Term V introl Windo				_	
rite to	Device	LMKØ4828	(i0), a	t waddr=	ØxØ126,	wdata=	0×F0
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0127,	wdata=	Øx15
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0128,	wdata=	0×0E
rite to	Device	LMKØ4828	(i0), a	t waddr=	Øx0129,	wdata=	Øx55
rite to		LMKØ4828	(i0), a	t waddr=	Ux012B,	wdata=	0×00
rite to			(10), a	t waddr=	0x012C,	wdata=	Øx22
rite to		LMK04828	(10), a	t waddr=	OXOLZU,	wdata=	0.00
rite to rite to	Device	LMKØ4828 LMKØ4828	(10), a	t waddr=	OXULZE,	Wdata=	Oxf0 Oxf
rite to			(10), a	t waddr= t waddr=	0x012F,	wuata-	0X12
rite to		LMK04828	(10)	t waddr=	0,0131	wdata=	0,00
rite to		LMK04828	(10)	it waddr=	0,0133	wdata=	0200
rite to		LMKØ4828	(10)	t waddr=	Øv0134	udata=	Øx22
rite to		LMKØ4828	(10).	t waddr=	ØxØ135	wdata=	0×00
rite to	Device	LMK04828	(i0).	t waddr=	Øx0136	wdata=	Ø×FØ
rite to	Device	LMKØ4828	(i0).	t waddr=	Øx0137.	wdata=	Øx15
rite to	Device	LMKØ4828	(i0). a	t waddr=	Øx0138.	wdata=	0×00
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0139,	wdata=	0×03
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x013A.	wdata=	0×07
rite to	Device	LMKØ4828	(i0), a	it waddr=	0x013B,	wdata=	0×E0
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x013C,	wdata=	0x00
rite to	Device	LMKØ4828	(iØ), a	it waddr=	0x013D,	wdata=	0×08
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x013E,	wdata=	0×03
rite to	Device	LMKØ4828	(i0), a	it waddr=	0x013F,	wdata=	0×00
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0140,	wdata=	0×01
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0141,	wdata=	0×00
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0142,	wdata=	0×00
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0143,	wdata=	0×10
rite to		LMKØ4828	(i0), a	t waddr=	0x0144,	wdata=	0×00
rite to		LMKØ4828	(i0), a	t waddr=	Ux0145,	wdata=	Øx7F
rite to		LMKØ4828	(i0), a	t waddr=	Ux0146,	wdata=	0×0F
rite to		LMKØ4828		t waddr=	Ux0147,	wdata=	0×06
rite to		LMKØ4828		t waddr=			
rite to		LMK04828	(10), a	t waddr=	0x0149,	wdata=	0×02
rite to		LMK04828	(10), a	t waddr=	0x014H,	wdata=	
rite to	Device	LMKØ4828 LMKØ4828	(10), a	t waddr=	0X014B,	wdata=	0X10
rite to rite to		LMKØ4828	(10), 3	t waddr= t waddr=	0x01.40,	wdata=	
rite to		LNK04828		it waddr=			
rite to		LMK04828		it waddr=			
rite to		LMK04828	(in)	t waddr=	0x0150	wdata=	Øx1B
rite to		LMK04828	(10)	it waddr=	Øx0151	wdata=	Øx02
rite to		LMK04828		t waddr=			
rite to		LMK04828		t waddr=	0×0153	wdata=	0×00
rite to		LMK04828	(i0).	t waddr=	0x0154	wdata=	0×02
rite to		LMKØ4828	(i0).	t waddr=	0x0155	wdata=	0×00
rite to		LMKØ4828	(i0), a	t waddr=	0x0156,	wdata=	0×02
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0157,	wdata=	0×00
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x0158,	wdata=	Øx96
rite to	Device	LMKØ4828	(i0), a	it waddr=	0x0159,	wdata=	0×00
rite to	Device	LMKØ4828	(i0), a	t waddr=	0x015A,	wdata=	Ø×19
rite to	Device	LMKØ4828	(i0), a	it waddr=	0×015B,	wdata=	Ø×DF
rite to	Deutice	LMKØ4828	(10)	t unddm=	D-DIEC	udata-	

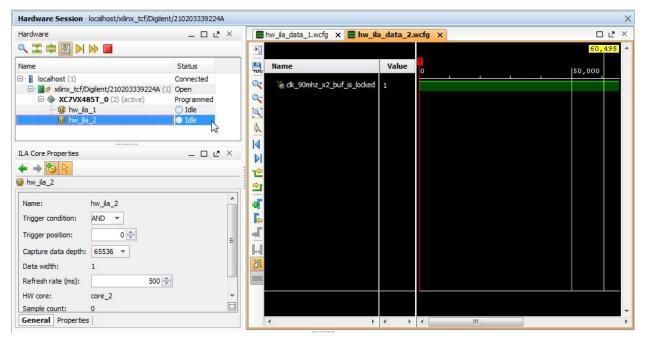
Wait for initialization to complete— it takes about 5 seconds. There are several pauses of 400ms to meet the timing requirements of the ADCs (beyond the scope of this document).

11 100 to people hpillip_1 (11), at waali opoid, waata oxoo	
Write to Device AD1443D_4 (i4), at waddr= 0x0811, wdata= 0x40	
Write to Device AD1443D_4 (i4), at waddr= 0x0812, wdata= 0x0A	
Write to Device AD1443D_4 (i4), at waddr= 0x081E, wdata= 0x08	
Write to Device AD1443D_4 (i4), at waddr= 0x086B, wdata= 0x02	
Write to Device AD1443D_4 (i4), at waddr= 0x086C, wdata= 0x02	
Write to Device AD1443D_4 (i4), at waddr= 0x0872, wdata= 0x04	e Etre Santa Santo Wolfer Miller
Write to Device JESD204B (i7), waddr= 0x04, actual_waddr= 0xB0000004, wda	ata= 0x00000001
Write to Device JESD204B (i7), waddr= 0x0C, actual_waddr= 0xB000000C, wda	
Write to Device JESD204B (i7), waddr= 0x00, actual_waddr= 0xB0000000, wda	
Write to Device JESD204B (i7), waddr= 0x00, actual_waddr= 0xB0000000, wda	ata= 0x00000712
Info: Done Initialization	lession - service peterpeters and service
Command>	

#### 2.22 (Optional Step) Confirming the Clocks are Operating after Initialization

For completeness, this optional step directs the user to confirm that a clock is now being received from the FSF-AD8200A card following initialization. If so desired, this validation step may be skipped; go directly to section 2.23.

In Vivado, trigger on hw\_ila\_2, the waveform now shows that the clock is locked, and initialization must have completed.



#### 2.23 Capturing Non-Static Data with the ILA cores

The system is now fully configured and is ready to use hw\_ila\_1 to capture and display signals from the JESD204B receiver. To drive all 8 analog inputs, an RF generator outputs a sine wave, which is then split into 8 feeds. These 8 feeds are then connected to the 8 analog inputs on the FSF-AD8200A. In Vivado, however over the "IDLE" word in the Status column next to hw\_ila\_1, and right-click, select "TRIGGER". After a few seconds the display is updated and waveforms are displayed.

Note, within ILA, the format of the waveforms can be defined by the user. For the following display, the format was set to ANALOG, and the waveform height was set to 30 pixels for each trace.

Name	Value	<u>.</u>					
		0		S 1		50,000	
	2864	and a state	and the state of t	and and the suffice suffice	an aite	on officiate	
🖽 📲 tdata[1][13:0]	2893	ուստ հոդեր Դեն հոդեր	entre attre attre	ane ane activitation	and a	onthe laster	an ha
🖬 📲 tdata[2][13:0]	2875	and and a state	ano ano an hu.	an an an	and a	te auto	in and
🗄 📲 tdata[3][13:0]	28a9		alle alle alle	ann ann te ailte ait	ane aite	ontre on Le sate	19 
∎ 📲 tdata[4][13:0]	287f	aller aller alle alle	ann ann ann aithe aithe ait	an an naite aite	an a	n ann	un Calu
🛨 📲 tdata[5][13:0]	2895	ան, ան,	արը օրը։ օրը Հուս շինչ	are are warde are	ann an	n nin a	.alle
🗄 📲 tdata[6][13:0]	2883	alle alle			ne	un andra	ane Inc
🖽 📲 tdata[7][13:0]	28ca	and and	ante ante ante antes antel ant	ane alle at	ane and the	ur ann a	aur be.
1							
k							

This is a full collection of 64K samples from each of 8 channels. By zooming in, one can clearly see the sine waves.

hw_ila_data_2.wcfg ×	🛢 hw_ila_data	CEL VA	다. ~
Name	Value	18,586	
•••• •• 	20aa		19,000 19,
🔍 🗉 📲 tdata[1][13:0]	2084		
🛓 ⊞ 📲 tdata[2][13:0]	2067	$\Delta \Delta \Delta$	$ \land \land \prime $
Image: The second s	2042		$\Delta \Delta \ell$
📴 📲 tdata[4][13:0]	2023		AA(
➡	1fdd		
🖌 🖬 📲 tdata[6][13:0]	20b6		
🍋 🖬 🔩 tdata[7][13:0]	206a		
↔]			
<u>kn</u>			
•	► <	F (	

The display can be updated with new samples by clicking the TRIGGER button in Vivado or right clicking on the hw\_ila\_1 status and then selecting "TRIGGER" from the menu.

Note that the digitized data being used by the ANALOG display can be saved within a file on the Host PC using the following TCL command:

write\_hw\_ila\_data filename.zip [upload\_ila hw\_ila\_1]

This 'recorded' data can then be post processed on the Host PC. Post processing shows perfect or near perfect alignment of all 8 sampled signals— a huge advantage of JESD204B Subclass 1!