CO401GW1A-BD

CANopen-Gateway-Modul

frenzel + berg electronic

General Description

The CO401GW1-BD is a low cost CANopen module for gateway applications. The chip enables serial connections to a standard CANopen network. The module uses the single chip controller CO401GW1. So this data sheet is an appendix of the CO401GW1 data sheet.


Features

- Single Chip CANopen Controller
- According to CiA Draft Standards DS301 Version 4.0 and DS401 Version 2
- Gateway Interface using UART with programmable Baudrate
- CAN-Baudrate up to 1MBit
- Output drivers with 4mA
- Watchdog output
- Temperature ranges up to –40 to 85 °C
- Package 60 pin module
- Dimensions (41mm x 31mm x 18mm)

Applications

- Connection of microcontroller applications to CANopen networks
- CANopen slave controller for existing applications

CANopen Features

- 2 Transmit- and 2 Receive PDOs
- Variable PDO identifier
- All CANopen specific PDO transmission types supported:
  synchronous, asynchronous, event driven, cyclic, acyclic and remote frame dependent.
- Event timer and inhibit timer features for all transmit PDOs.
- Storing and restoring of object dictionary to non-volatile memory
- Node guarding, Life guarding, Heartbeat
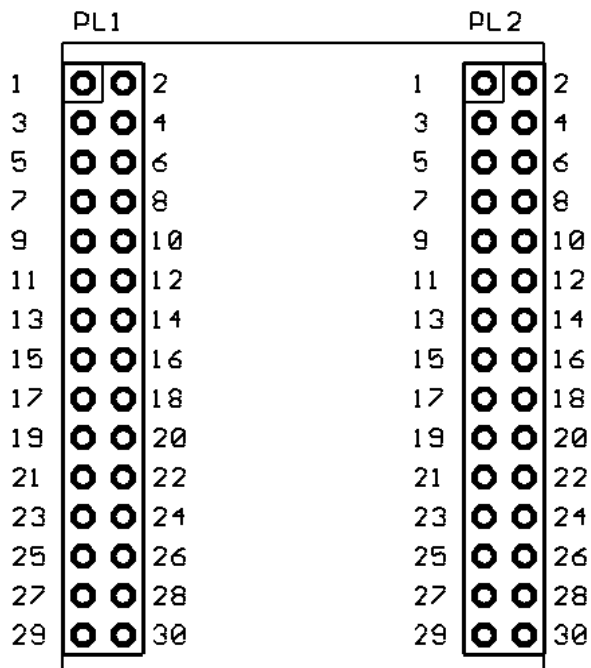- Emergency messages
- Minimum boot up
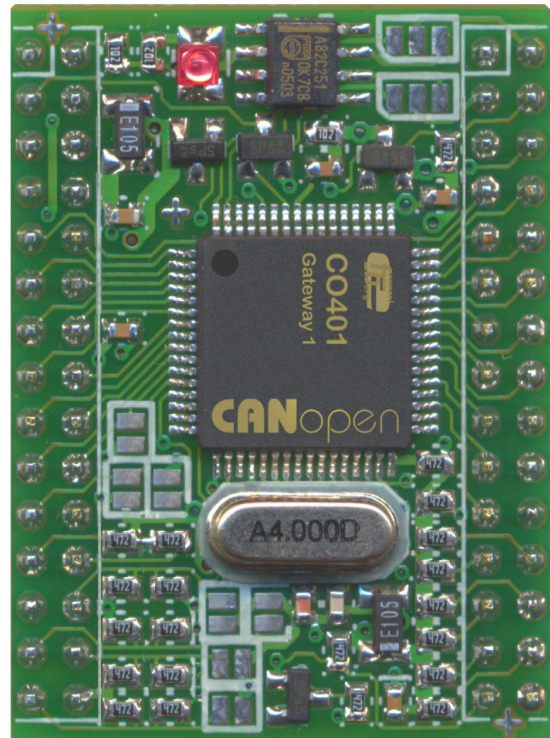
Ordering Information

**CO401-Gateway-BD
(programmed, licence included)**

Part	Temp. Range	Package
CO401GW1A-BD	0 to 70 °C	60 Pin module
CO401GW1AE-BD	-40 to 85 °C	60 Pin module

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Pin Assignment

PL1   PL2

Top view (component side)

Pin Listing CO401GW1-BD

PL1

Pin No.	Pin Name	Function
1	VSS	Ground
2	LED	4 mA limited output (anode) for a status LED
3	WD#	Watch dog out
4	SSC0	Reserved for Synchronous Serial Interface Control (for future applications)
5 to 7	RSBD0 .. RSBD2	CANopen baud rate selection bits
8	SCLK	Reserved for Synchronous Serial Interface Clock (for future applications)
9	RSTXD	Serial interface transmitter output line
10 to 17	IN7 .. IN0	Digital Input channels
18, 19	RES0, RES1	Reserved for future use

PL1

Pin No.	Pin Name	Function
20	AVCC	Supply for A/D-Converter
21	AVREF	Reference Voltage for A/D-Converter
22	AVSS	Ground for A/D-Converter
23 to 25	BD2 .. BD0	Baud rate selection inputs
26	CFG2 / WD	Configuration input Bit2 Watchdog output
27	SERNO	Reserved for external Serial Number IC DS2401P (for future applications)
28	CFG1 / E	Configuration input Bit0 CANopen error LED output
29	CFG0 / R	Configuration input Bit0 CANopen run LED output
30	VCC	Power supply

PL2

Pin No.	Pin Name	Function
1	VCC	Power supply
2	CANH	CAN high line
3	CANL	CAN low line
4	RSRXD	Serial interface receiver input line
5	RESET#	Reset in / out
6 to 11	SSC1 .. SSC6	Reserved for Synchronous Serial Interface Control (for future applications)
12	EMY1#	Emergency Input 1 Active low
13	EMY0#	Emergency Input 0 Active low
14 to 21	OUT7 .. OUT0	Digital output channels
22 to 28	ID6 .. ID0	CANopen Identifier selection input bits
29	BOOT#	Firmware Update Input
30	VSS	Ground

Handling the Device

Preventing latch up

The CO401GW1-BD is a CMOS device and may suffer latch up under the following conditions:
1) A voltage higher than VCC or lower than VSS is applied to any pin.
2) Absolute maximum ratings are exceeded
3) AVCC power is provided before VCC supply

Handling unused input Pins

Do not leave unused input pins open. This might cause malfunction of the device.

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Power Supply Pins

Make sure that all ground and power supply pins are connected to the same potential. Do not leave any ground or power pins open. Connect at least two ceramic capacitors of 100 nF and a tantalum capacitor of 1 uF between VCC and VSS as close as possible to the device.

Power Supply for A/D converter

The power supply for the A/D converter must not be turned on before the power supply VCC.
If the A/D converter is not used, connect the pins as follows: AVCC = VCC, AVSS = AVREF = VSS.

Note! Make sure, that Jumper J5, J6 and J7 are open in this case!

Pull up/down resistors

The CO401GW1-BD does not support internal pull up/down resistors at the INx/OUTx pins. Use external components where needed.


Pin Description

BOOT#: Firmware Update

A low level during reset at this pin, and an ID0 and ID1 at low level, activate the firmware update mode. In this case the pins RSTXD and RSRXD will be used for updating the firmware by an asynchronous communication.

Pin Name	Pin No.	Normal operation	Firmware update
BOOT#	PL2 / 29	High	low
ID0	PL2 / 28	X	low
ID1	PL2 / 27	X	low
RSTXD	PL1 / 9	TXD (TTL)	TXD (TTL)
RSRXD	PL2 / 4	RXD (TTL)	RXD (TTL)

The update may be done with a COM-Port from a PC/Notebook and an in circuit update tool for the Fujitsu MB90F497 micro controller. TXD and RXD are the transmitter and receiver pins of the asynchronous serial interface.
The pins TXD and RXD work with 5V TTL-level. So if you need a connection to a PC COM-Port, you have to add a RS232 driver circuit like it is shown by the followed figure.

RS232 Driver Circuit

Cable with D-SUB 9 connector to a PC COM port
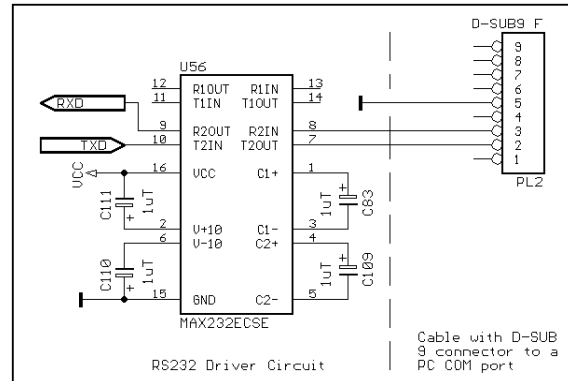
CFG0 .. CFG2: Configuration input pins
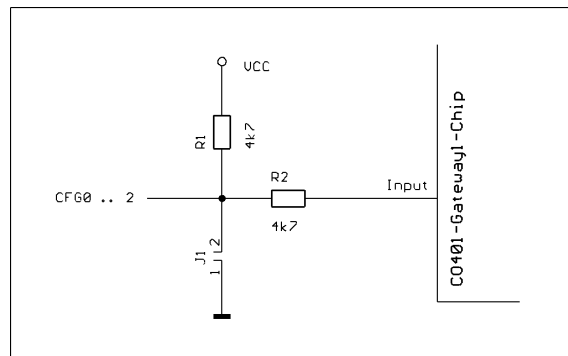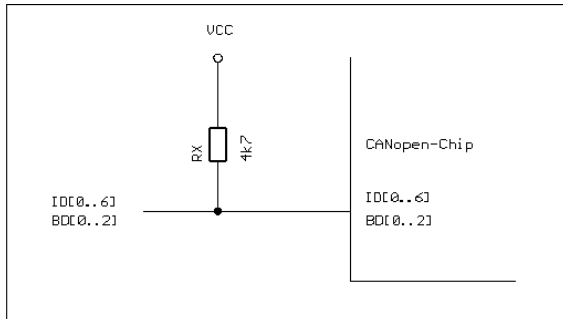

The CFG1, CFG2 configuration inputs are reserved for future use.
Note: These pins have also jumper on board. To preventing malfunctions and short circuits check the jumper settings before using this pins.

For future use: Set device configuration to preferred operation mode using CFG0 to CFG2. If you leave any configuration input unconnected make sure, that the correct configuration is set via the on board jumpers. Refer to chapter 'Device Configuration' for details and functionality.

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ID0 .. ID6, BD0 .. BD2: Identifier and baud rate input pins

Refer to chapter 'Device Configuration' for details and functionality.

CANH, CANL (CANTx, CANRx) CAN Interface

The CAN Bus with its associated protocol allows communication between a number of stations which are connected to this bus with high efficiency. (Transfer speed up to 1 MBaud)

The on board CAN transceiver (82C251) can be used or not, depending on the setting of Jumper J8 and J9.

Without using the CAN transceiver:
In case without using the on board CAN transceiver, a user specific (opto isolated) CAN driver circuit may be realized on the application board. Therefore the Jumpers J8 and J9 have to be set to position 1-2.

In this condition the CANH pin is connected to signal CANRX and CANL to CANTX (TTL level).

With using the CAN transceiver:
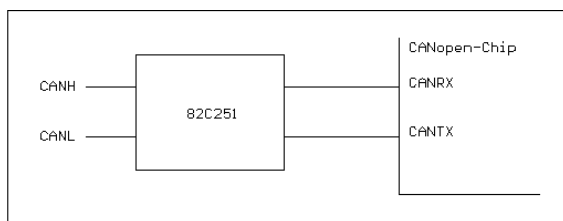
By using the on board CAN transceiver it is possible to connect the board directly to a two wire CAN bus associated to ISO11898. Therefore the Jumpers J8 and J9 have to be set to position 2-3.

Note: It is not allowed to set the Jumper J8 or J9 in position 1-2-3 same times. This might cause permanent damage to the device.
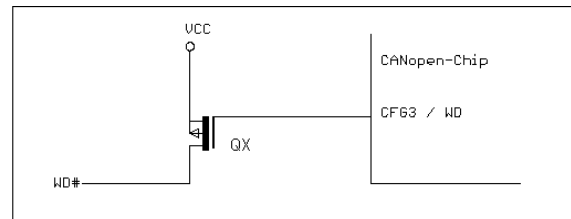
RESET#: Reset input/output pin

The on board reset chip does the power up reset. It pulls the RESET# line low. So it is possible to reset external components during power up using this signal.
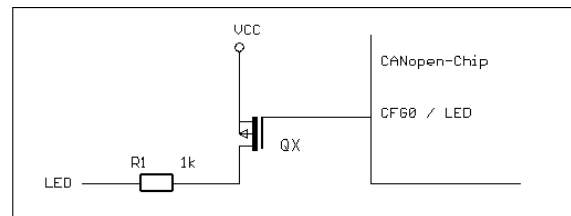
The reset pin may also be used as reset input. For a correct device reset by external components, provide a low level longer than 50 ms to the input RESET#.

Note: Do never drive a high level to the RESET# pin. This may cause permanent damage to the device. Use a push button or an open drain driver for this condition.

WD: Watch dog output pin

LED: Status LED output pin

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The following sections describe the device configuration with meaning:
1: ViH   logic high level
0: ViL   logic low level

CAN Identifier

The CAN Identifier will be set with Pins ID0 to ID6. ID7 is reserved for future use. This configuration pins use internal inverter. The ID is set as follows:

ID6	ID5	ID4	ID3	ID2	ID1	ID0	CAN-Identifier
1	1	1	1	1	1	1	Programmable ID
1	1	1	1	1	1	0	1 = 0x01
1	1	1	1	1	0	1	2 = 0x02
1	1	1	1	1	0	0	3 = 0x03
1	1	1	1	0	1	1	4 = 0x04
			….				….
1	0	0	0	0	0	0	63 = 0x3F
0	1	1	1	1	1	1	64 = 0x40
0	1	1	1	1	1	0	65 = 0x41
			….				
0	0	0	0	0	1	0	125 = 0x7C
0	0	0	0	0	0	1	126 = 0x7E
0	0	0	0	0	0	0	127 = 0x7F

All Identifiers from 1 to 127 are valid settings.

CAN baud rate

The baud rate configuration will be done with configuration inputs BD0 to BD2

BD2	BD1	BD0	CAN-Baud Rate / Bus length
1	1	1	1 Mbit/sec 25 m *1)
1	1	0	800 kbit/sec 50 m *1)
1	0	1	500 kbit/sec 100 m *2)
1	0	0	250 kbit/sec 250 m *2)
0	1	1	125 kbit/sec 500 m *3)
0	1	0	50 kbit/sec 1000 m *3)
0	0	1	20 kbit/sec 2500 m *3)
0	0	0	10 kbit/sec 5000 m *3)

*1)   Calculation without optocouplers.
      For optocouplers bus length is reduced for about 4m per 10 nsec propagation delay of employed optocoupler type
*2)   Calculation with 40 nsec optocoupler propagation delay
*3)   Calculation with 100 nsec optocoupler propagation delay

The calculation of the bus length is based on a line propagation delay of 5 nsec/m.

Serial baud rate

The serial baud rate configuration for the serial gateway interface will be done with configuration inputs RSBD0 to RSBD2

RS BD2	RS BD1	RS BD0	Serial Interface Baud Rate	
			nominal	Exact
1	1	1	9600	9615
1	1	0	4800	4807
1	0	1	2400	2404
1	0	0	Reserved	-
0	1	1	76900	76923
0	1	0	38400	38461
0	0	1	19200	19230
0	0	0	Reserved	-

Device Configuration Pins

With the device configuration input bits the CANopen Gateway Chip can be adapted to several application requirements.
CFG0 is used to enable/disable the digital input lines by default.
CFG1, CFG2 are reserved for future use.

	CFG		Setting
2	1	0	
X	X	1	Digital inputs enabled
X	X	0	Digital inputs disabled

In order to keep compatibility to future versions of the CO401GW1 controller it is recommended to place pull up resistors of approx. 10k to the reserved configuration input pins.

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Absolute Maximum Ratings

Stresses greater than those listed parameters may cause permanent damage to the device. Functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended times may affect reliability.
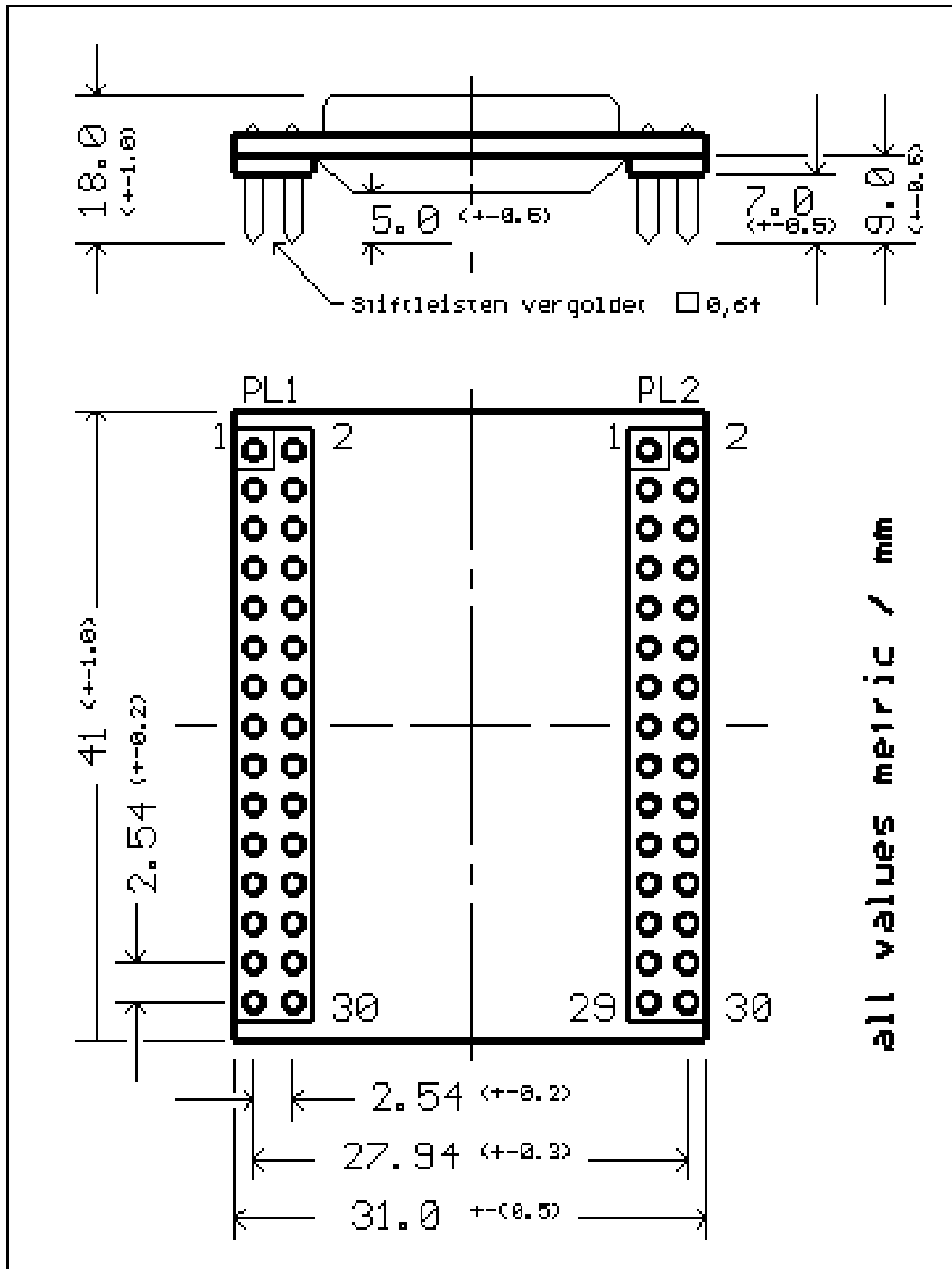
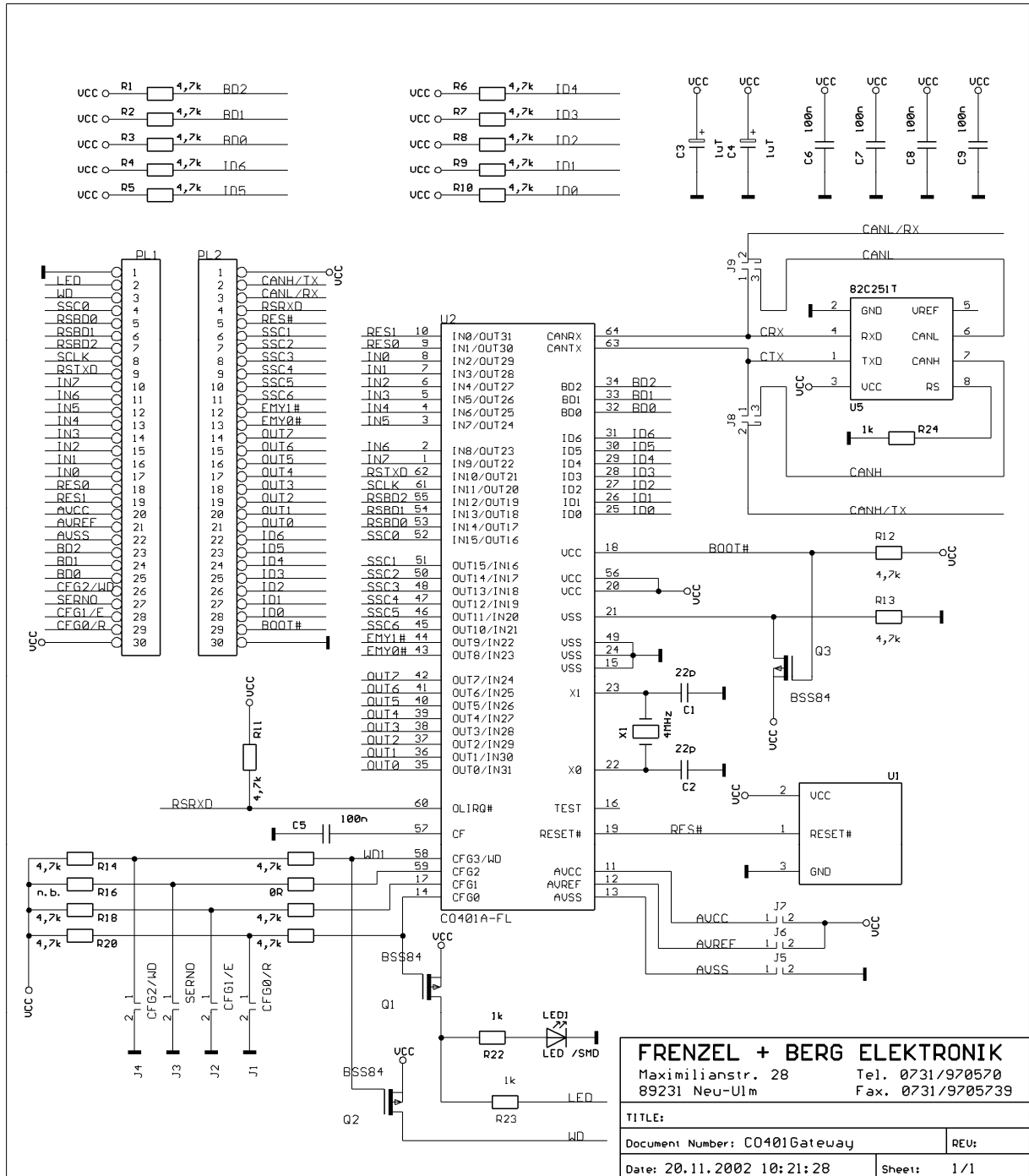| Parameter	Symbol	Rated Value		Units	Remarks
		Min.	Max.		
Power supply voltage	VCC	VSS – 0.3	VSS + 6.0	V	
Analog power supply voltage	AVCC	VSS – 0.3	VCC	V	
Analog reference voltage	AVREF	VSS – 0.3	VCC	V	
Input voltage	Vi	VSS – 0.3	VSS + 6.0	V	Vi < VCC + 0.3V
Output voltage	Vo	VSS – 0.3	VSS + 6.0	V	Vo < VCC + 0.3V
L level maximum output current	I_{OLMAX}		15	mA	Time < 20 msec
L level maximum output current	I_{OL}		4	mA	
H level maximum output current	I_{OHMAX}		15	mA	Time < 20 msec
H level maximum output current	I_{OH}		4	mA	
Maximum Power dissipation	P_{MAX}		800	mW	
Operating temperature	T_A	0	+70	ºC	CO401GW1-BD
	T_A	-40	+85	ºC	CO401GW1E-BD
Storing temperature	T_A	-55	+150	ºC	

Recommended Operation Conditions and Characteristics

Functional operation should be restricted to recommended operation conditions.

Parameter	Symbol	Rated Value			Units	Remarks
		Min.	Typ.	Max.		
Power supply voltage	VCC	4.5	5.0	5.5	V	
Analog power supply voltage	AVCC			VCC	V	
Analog reference voltage	AVREF			VCC	V	
Power supply current	I_{CC}		65	110	mA	All inputs V_{IL} or V_{IH} All outputs open CAN bus open
Input H voltage	V_{IH}	0.8 * VCC		VCC + 0.3	V	
Input L voltage	V_{IL}	VSS – 0.3		0.2 * VCC	V	
Output H voltage	V_{OH}	VCC – 0.5			V	I_{OH} = -4.0 mA
Output L voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Input leakage current	I_{LKC}	-5		5	uA	
Crystal frequency	f_{osc}		4		MHz	
Reset pulse width	t_{res}	10			us	
Power on rise time	t_{RESLH}	0.05		30	ms	
Maximum CANopen Delay input pin to bus telegram	t_{DITB}	0.05	1	2	ms	No additional bus distribution delay
Maximum CANopen Delay bus telegram to output pin	t_{DBTO}	0.05	1	2	ms	
Watchdog trigger frequency	f_{WDT}	0.5	1	2	kHz	Delayed max. 500 ms after reset
Maximum Power dissipation	P_{MAX}			300	mW	
Operating temperature	T_A	0		+70	ºC	CO401GW1-BD
	T_A	-40		+85	ºC	CO401GW1E-BD

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Package Dimension CO401GW1-BD

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Schematics CO401GW1-BD

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