CO4031A-BD

Controller Board for Keyboard + LED + LCD-Display Interfaces

frenzel + berg
electronic

General Description

The CO4031A-Bd is a CANopen module for interfacing keyboards, LEDs and LCD modules to a CANopen network. The module uses the single chip controller CO4031. So this data sheet is an appendix of the CO4031 data sheet.

The CO4031A-BD is a low cost, high performance module for CANopen Keyboards, LED-Panels and LCD-Display modules. It is especially designed for automotive and industrial applications. The device offers the complex implementation of the CANopen standards DS301 and DS401 in a single chip. The Matrix-Keyboard is processed as digital input lines. Additionally a special object describing a key status is implemented.

The LEDs are accessed as LED-Array. They are set from the digital output objects. For interfacing an alphanumeric LCD module special data objects are implemented.

The board is suitable for simple CANopen HMI interfaces and operator panels with matrix keyboards up to 64 keys, up to 32 status LEDs arranged in a LED matrix and an alphanumeric LCD module. LCD size can be up to 4 lines with 20 characters per line. The chip can address nearly all modules based on the Hitachi HD44780 or compatible LCD controllers.

Features

-
- **According to CiA Draft Standards DS301 Version 4.0 and DS401 Version 2.0**
- **Additional Objects for Matrix Keyboard, LEDs and LCD module**
- **Debounce logic for Keyboard**
- **Temperature ranges up to –40 to 85 ºC**
- **Package 60 pin module**
- **Dimensions (41mm x 31mm x 18mm)**
-

Applications

The boards are optimized for automotive and industrial applications such as:

- **CANopen Operator panels**
- **Information terminals**
- **Industrial HMI for automation control**
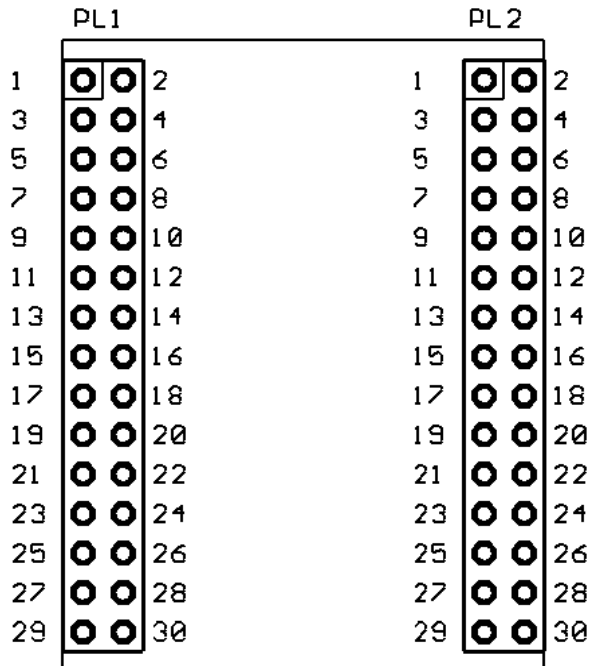- **CANopen Interface for keyboards and control panels**

CANopen Features

-
- **2 Transmit- and 2 Receive PDOs**
- **Dynamic PDO mapping**
- **Variable PDO identifier**
- **All CANopen specific PDO transmission types supported:** synchronous, asynchronous, event driven, cyclic, acyclic and remote frame dependent.
- **Event timer and inhibit timer features for all transmit PDOs.**
- **Storing and restoring of object dictionary to non-volatile memory**
- **Node guarding, Life guarding, Heartbeat**
- **Baudrate up to 1MBit**
- **Emergency messages**
- **Minimum boot up**

Ordering Information

CO4031A-BD (license included)

Part	Temp. Range	Package
CO4031A-BD	0 ºC to 70 ºC	60 Pin module
CO4031AE-BD	–40 ºC to 85 ºC	60 Pin module

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Pin Assignment

PL1   PL2

1 ● ● 2   1 ● ● 2
3 ● ● 4   3 ● ● 4
5 ● ● 6   5 ● ● 6
7 ● ● 8   7 ● ● 8
9 ● ● 10   9 ● ● 10
11 ● ● 12   11 ● ● 12
13 ● ● 14   13 ● ● 14
15 ● ● 16   15 ● ● 16
17 ● ● 18   17 ● ● 18
19 ● ● 20   19 ● ● 20
21 ● ● 22   21 ● ● 22
23 ● ● 24   23 ● ● 24
25 ● ● 26   25 ● ● 26
27 ● ● 28   27 ● ● 28
29 ● ● 30   29 ● ● 30

Top view (component side)

PL1		
Pin No.	Pin Name	Function
20	AVCC	Supply for A/D-Converter
21	AVREF	Reference Voltage for A/D-Converter
22	AVSS	Ground for A/D-Converter
23 to 25	BD2 .. BD0	Baud rate selection input
26 to 29	CF3 .. CF0	Configuration bits 0 to 3 for I/O setting
30	VCC	Power supply

PL2		
Pin No.	Pin Name	Function
1	VCC	Power supply
2	CANH	CAN high line
3	CANL	CAN low line
4	BUZ#	Buzzer output
5	RESET#	Reset in/out
6 to 13	KBD-R7 .. KBD-R0	Keyboard interface Return input lines for reading keyboard column
14 to 21	KBD-S7 .. KBD-S0	LED-/Keyboard interface Scan output lines for selecting matrix keyboard line Column for LED matrix
22 to 28	ID6 .. ID0	Identifier selection input
29	FWUD#	Firmware Update
30	VSS	Ground

Pin Listing CO4031A-BD

PL1		
Pin No.	Pin Name	Function
1	VSS	Ground
2	LED	4 mA limited output (anode) for a status LED
3	WD#	Watch dog out
4 to 7	LED0# .. LED3#	LED line output
8	CFG4	Configuration bit 4
9	LCD-RW	LCD-Interface Read write control output line
10	LCD-RS	LCD-Interface. Register Select Line
11	LCD-EN	LCD-Interface Display Enable
12 to 19	LCD-D0 .. LCD-D7	LCD-Interface 8 Bit Data Bus to LCD module

Pin Description

All input / output pins are high impedance during reset. The CO4031 does not support internal pull up/down resistors. Use external components where needed. All input pins have Schmitt trigger characteristics. See chapter "Typical Applications" for additional information.

LCD-Interface Pins

The LCD interface allows direct drive of a alpha-numeric LCD module based on HD44780 or compatible LCD controllers. Nearly all modules are based on this standard.

LCD-D0 to LCD-D7: Data bus of LCD module

Bi-directional data bus to the LCD module. Connect this port directly to the LCD modules data port.

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LCD-RS: LCD Register Select Output

The Register Select output line selects whether the actual data bus cycle addresses either the display RAM or the command register of the LCD module. LCD-RS at LOW level addresses the command register, while LCD-RS at HIGH level addresses the display data RAM. Connect this port directly to pin RS of the LCD module.

LCD-R/W: LCD Read / Write Control Output

The Read / Write control output line selects whether the actual data bus cycle is a read or a write cycle. LCD-R/W at LOW level indicates a write cycle while LCD-R/W at HIGH level indicates a read cycle. Connect this port directly to pin R/W of the LCD module.

LCD-EN: LCD Enable Control Output

The LCD Enable control output line controls a data bus cycle. During access to the LCD module, the CO4031 forces this pin to HIGH level. Connect this port directly to pin EN of the LCD module.

LED-/Keyboard-Interface Pins

The LED-/Keyboard interface allows direct connection of a 8x8 matrix keyboard.
A maximum of 32 LEDs can be driven from the CO4031s LED controller. The LEDs must be arranged in an array of 4 lines (with common anode) and 8 columns. The LED lines will be multiplexed within the keyboard scan cycle. For interfacing a LED array of max 4x8 LEDs additional driver circuits must be used.
The LED-/Keyboard-Interface uses two different cycles to scan the keyboard and set the LEDs. This two cycles are multiplexed from the CO4031. They use the common lines KBD-S0 to KBD-S7
See also typical Application for further information.

KBD-S0 to KBD-S7 : Scan Lines

The keyboard scan lines output the Keyboard line address during Keyboard Scan Cycle. A low level is driven to the output driver to select a keyboard line. All other output lines stay at high impedance during this time. So the Keyboard-Scan-Cycle scans one keyboard line after the other by pulling one output line to low level and then reading the columns of the keyboard using the keyboard return lines KBD-R0 to KBD-R7.
During LED cycle the KBD-S0 to KBD-S7 output drivers output the LED information for the LED column selected by the LED line outputs LED0# to LED3#. For switching a LED on, the appropriated scan line is forced to low level.

The output drivers for LEDs that must be switched off are held in tristated mode, so it is strongly recommended, to use pull up resistors of approx 4.7 kOhms at this port.
See also typical Application for further information.

KBD-R0 to KBD-R7 : Keyboard Return Lines

The keyboard return input lines are used to read the key column values for the line selected with KBD-Sx. A pressed key must force this line to LOW level. Use pull up resistors of approx 4.7kOhms at this port to meat this requirements.

LED0# to LED3# : LED Line Select

This LED line select output lines select the LED line of the LED array, that will be controlled by the actual cycle. The output drivers are set to LOW level to select a line, so PFET transistors may be used for this purposes.
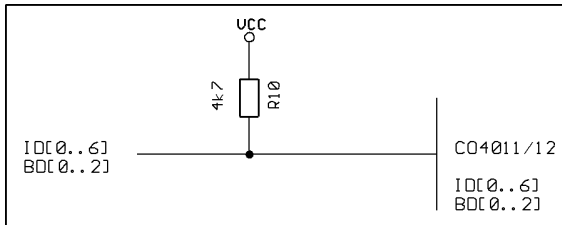
Configuration / Interface / Supply Pins

CF0 .. CF3: Configuration input pins
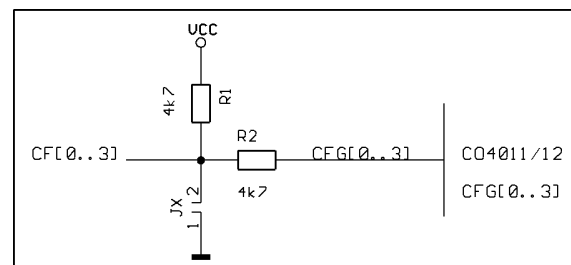
Note: These pins have also jumper on board. To preventing malfunctions and short circuits check the jumper settings before using this pins.

Set device configuration to preferred operation mode using CF0 to CF3. If you leave any configuration input unconnected make sure, that the correct configuration is set via the on board jumpers.

Refer to chapter 'Device Configuration' for details and functionality.

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ID0 .. ID6, BD0 .. BD2: Identifier / baud rate input pins

Refer to chapter 'Device Configuration' for details and functionality.

CANH, CANL (CANTx, CANRx) CAN Interface

The CAN Bus with its associated protocol allows communication between a number of stations which are connected to this bus with high efficiency. (Transfer speed up to 1 MBaud)

The on board CAN transceiver (82C251) can be used or not, depending on the setting of Jumper J8 and J9.

Without using the CAN transceiver:
In case without using the on board CAN transceiver, a user specific (opto isolated) CAN driver circuit may be realized on the application board. Therefore the Jumpers J8 and J9 have to be set to position 1-2.

In this condition the CANH pin is connected to signal CANRX and CANL to CANTX (TTL level).

With using the CAN transceiver:
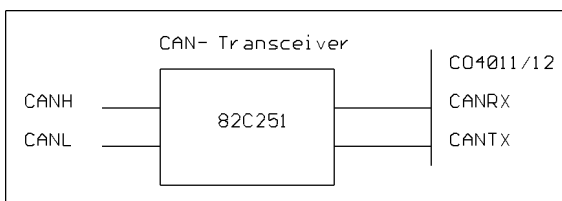
By using the on board CAN transceiver it is possible to connect the board directly to a two wire CAN bus associated to ISO11898. Therefore the Jumpers J8 and J9 have to be set to position 2-3.

Note: It is not allowed to set the Jumper J7 or J8 in position 1-2-3 same times. This might cause permanent damage to the device.

RESET#: Reset input/output pin

The on board reset chip does the power up reset. It pulls the RESET# line low. So it is possible to reset external components during power up using this signal.
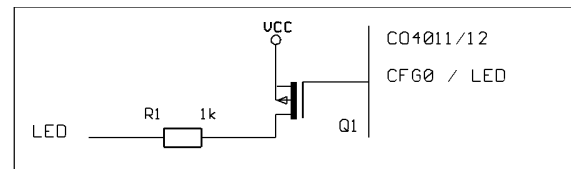
The reset pin may also be used as reset input. For a correct device reset by external components, provide a low level longer than 50 ms to the input RESET#.

Note: Do never drive a high level to the RESET# pin. This may cause permanent damage to the device. Use a push button or an open drain driver for this condition.

WD: Watch dog output pin
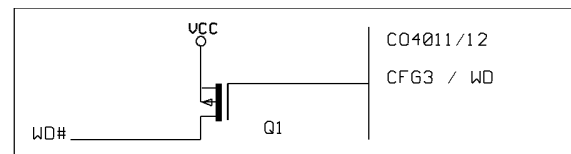
LED: Status LED output pin

BUZ#: Buzzer output

Buzzer output. Digital output line to switch a buzzer on. (active low)

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Handling the Device

Preventing latch up

The CO4031 is a CMOS devices and may suffer latch up under the following conditions:
1) A voltage higher than VCC or lower than VSS is applied to any pin.
2) Absolute maximum ratings are exceeded
3) AVCC power is provided before VCC supply

Handling unused input Pins

Do not leave unused <u>input</u> pins open. This might cause malfunction of the device.

Power Supply Pins

Make sure that all ground and power supply pins are connected to the same potential. Do not leave any ground or power pins open. Connect at least two ceramic capacitors of 100 nF and a tantalum capacitor of 1 uF between VCC and VSS as close as possible to the device.

Power Supply for A/D converter

The power supply for the A/D converter must not be turned on before the power supply VCC.
If the A/D converter is not used, connect the pins as follows: AVCC = AVREF = VCC, AVSS = VSS.

Note! Make sure, that Jumper J5, J6 and J7 are open in this case!

Pull up/down resistors

The CO4031A-BD does not support internal pull up/down resistors at the LCD / Keyboard interface pins. Use external components where needed.

Device Configuration

The following sections describe the device configuration with meaning:
1: ViH   logic high level
0: ViL   logic low level

CAN Identifier

The CAN Identifier will be set with Pins ID0 to ID6. This configuration pins use internal inverter. The ID is set as follows:

ID6	ID5	ID4	ID3	ID2	ID1	ID0	CAN-Identifier
1	1	1	1	1	1	1	Programmable ID
1	1	1	1	1	1	0	1 = 0x01
1	1	1	1	1	0	1	2 = 0x02
1	1	1	1	1	0	0	3 = 0x03
1	1	1	1	0	1	1	4 = 0x04
			….				….
1	0	0	0	0	0	0	63 = 0x3F
0	1	1	1	1	1	1	64 = 0x40
0	1	1	1	1	1	0	65 = 0x41
			….				….
0	0	0	0	0	1	0	125 = 0x7C
0	0	0	0	0	0	1	126 = 0x7E
0	0	0	0	0	0	0	127 = 0x7F

All Identifiers from 1 to 127 are valid settings. Identifier 0 is used to load the ID from object 2100.

Baud rate

The baud rate configuration will be done with configuration inputs BD0 to BD2

BD2	BD1	BD0	CAN-Baud Rate / Bus length		
1	1	1	1	Mbit/sec	25 m *1)
1	1	0	800	kbit/sec	50 m *1)
1	0	1	500	kbit/sec	100 m *2)
1	0	0	250	kbit/sec	250 m *2)
0	1	1	125	kbit/sec	500 m *3)
0	1	0	50	kbit/sec	1000 m *3)
0	0	1	20	kbit/sec	2500 m *3)
0	0	0	10	kbit/sec	5000 m *3)

*1) Calculation without optocouplers.
For optocouplers bus length is reduced for about 4m per 10 nsec propagation delay of employed optocoupler type
*2) Calculation with 40 nsec optocoupler propagation delay
*3) Calculation with 100 nsec optocoupler propagation delay

The calculation of the bus length is based on a line propagation delay of 5 nsec/m.

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LCD-Configuration

With configuration bits CFG0 and CFG1 the number of LCD lines that are supported from by the LCD module is set.

CFG 1	CFG 0	Nr of LCD-lines
1	1	No LCD module present
1	0	1
0	1	2
0	0	4

If there is no LCD interface present, the CO4031 controller disables the corresponding PDO.

With configuration bits CFG2 and CFG3 the number of LCD characters per line that are supported from by the LCD module are set.

CFG 3	CFG 2	Characters per line
1	1	8
1	0	16
0	1	20
0	0	40

The CO4031 uses exact setting of this bits in order to enable correct calculation of the display RAM addresses.
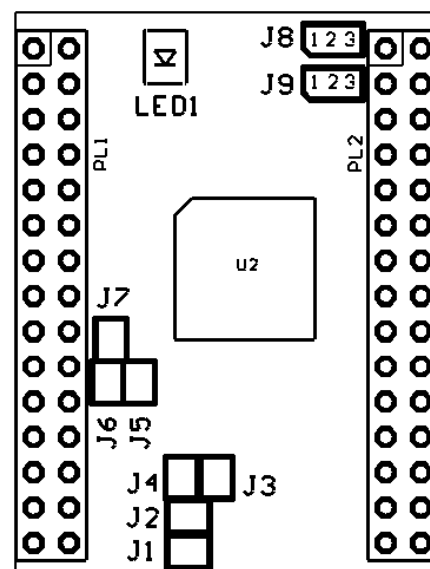
CFG4 is reserved for future use and should be held at high level to keep compatibility to future versions.

Note: CFGx pins are input pins during start up and output pins in normal operation mode. In order to prevent short circuit overload a series resistor between CFGx and configuration device (example DIP switch) should be used. See also "typical application" for details.

Jumper-Setting

Jumper	Setting	Prescription
J1	open	CFG0 = 1 (or configured by the CF0 pin)
	closed	CFG0 = 0
J2	open	CFG1 = 1 (or configured by the CF1 pin)
	closed	CFG1 = 0
J3	open	CFG2 = 1 (or configured by the CF2 pin)
	closed	CFG2 = 0
J4	open	CFG3 = 1 (or configured by the CF3 pin)
	closed	CFG3 = 0
J5	open	AVSS set by pin
	closed	AVSS connected to Ground
J6	open	AVREF set by pin
	closed	AVREF connected to VCC
J7	open	AVCC set by pin
	closed	AVCC connected to VCC
J8	1-2	Signal CANTX on PL2A Pin 2
	3-2	Signal CANH on PL2A Pin 2
J9	1-2	Signal CANRX on PL2A Pin 3
	3-2	Signal CANL on PL2A Pin 3

Note: Most jumpers are alternative to module pins with the same functionality. To prevent malfunctions and short circuits leave the corresponding pin open if the corresponding jumper is used.

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	Absolute Maximum Ratings

Stresses greater than those listed parameters may cause permanent damage to the device. Functional operation should be restricted to recommended operation conditions. Exposure to absolute maximum rating conditions for extended times may affect reliability.
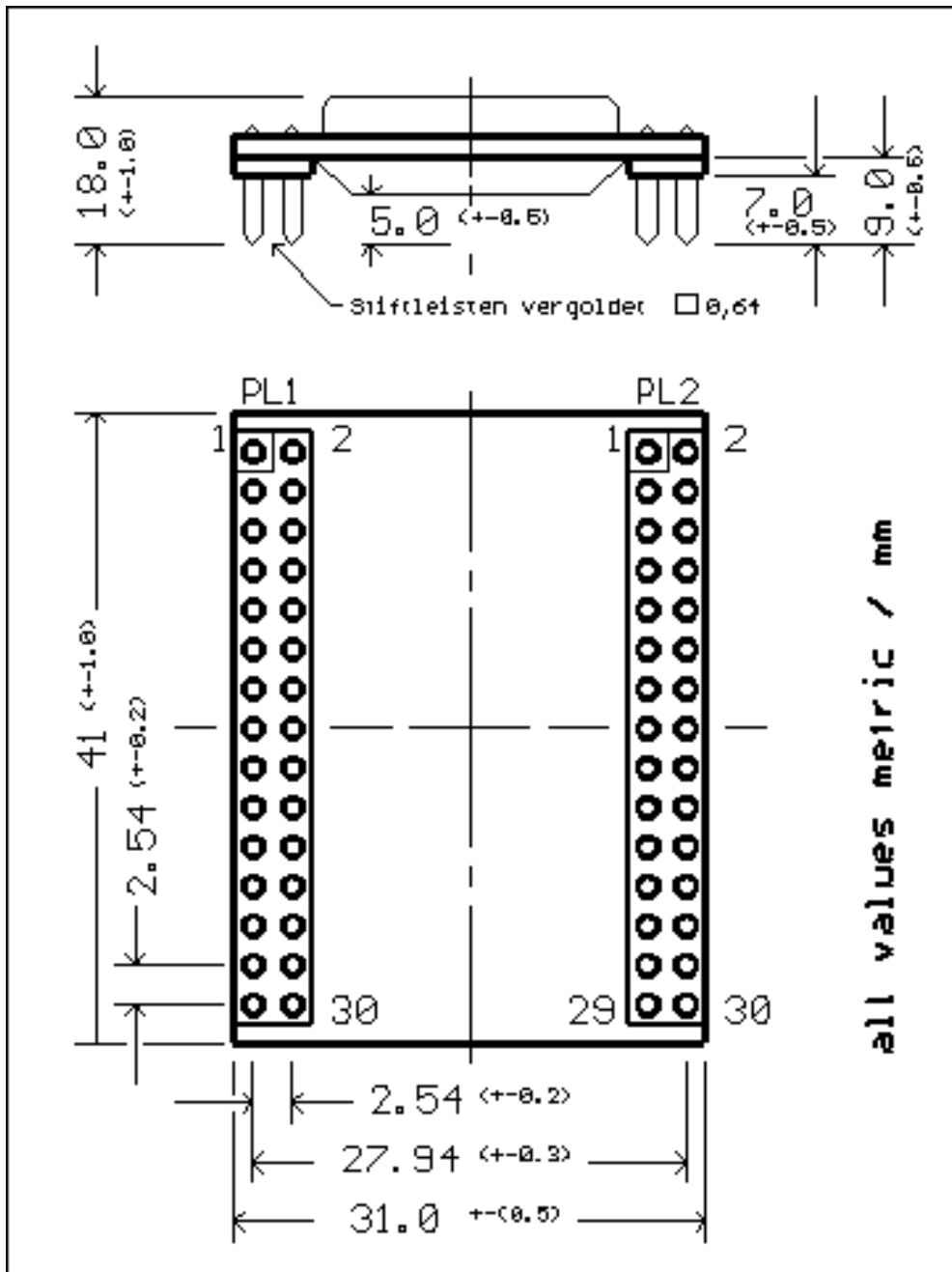
Parameter	Symbol	Rated Value		Units	Remarks
		Min.	Max.		
Power supply voltage	VCC	VSS – 0.3	VSS + 6.0	V	
Analog power supply voltage	AVCC	VSS – 0.3	VCC	V	
Analog reference voltage	AVREF	VSS – 0.3	VCC	V	
Input voltage	Vi	VSS – 0.3	VSS + 6.0	V	Vi < VCC + 0.3V
Output voltage	Vo	VSS – 0.3	VSS + 6.0	V	Vo < VCC + 0.3V
L level maximum output current	I_{OLMAX}		15	mA	Time < 20 msec
L level maximum output current	I_{OL}		4	mA	
H level maximum output current	I_{OHMAX}		15	mA	Time < 20 msec
H level maximum output current	I_{OH}		4	mA	
Maximum Power dissipation	P_{MAX}		800	mW	
Operating temperature	T_A	0	+70	°C	CO401xA-BD
	T_A	-40	+85	°C	CO401xAE-BD
Storing temperature	T_A	-55	+150	°C	

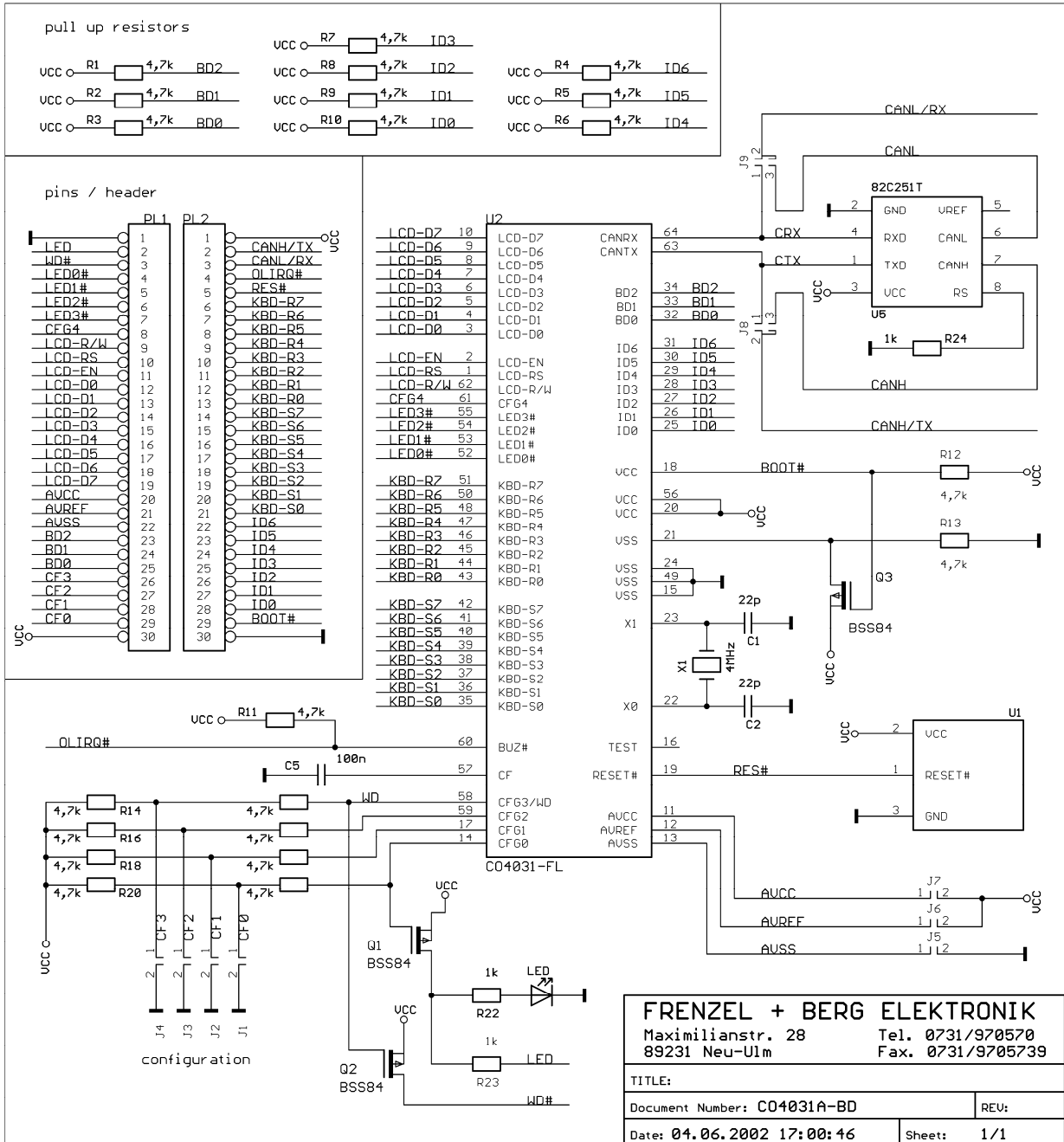|	Recommended Operation Conditions and Characteristics

Functional operation should be restricted to recommended operation conditions.

Parameter	Symbol	Rated Value			Units	Remarks
		Min.	Typ.	Max.		
Power supply voltage	VCC	4.5	5.0	5.5	V	
Analog power supply voltage	AVCC			VCC	V	
Analog reference voltage	AVREF			VCC	V	
Power supply current	I_{CC}		65	110	mA	All inputs V_{IL} or V_{IH} All outputs open CAN bus open
Input H voltage	V_{IH}	0.8 * VCC		VCC + 0.3	V	
Input L voltage	V_{IL}	VSS – 0.3		0.2 * VCC	V	
Output H voltage	V_{OH}	VCC – 0.5			V	I_{OH} = -4.0 mA
Output L voltage	V_{OL}			0.4	V	I_{OL} = 4.0 mA
Input leakage current	I_{LKC}	-5		5	uA	
Reset pulse width	t_{res}	10			us	
Power on rise time	t_{RESLH}	0.05		30	ms	
Maximum CANopen Delay input pin to bus telegram	t_{DITB}	0.05	1	2	ms	No additional bus distribution delay
Maximum CANopen Delay bus telegram to output pin	t_{DBTO}	0.05	1	2	ms	
Maximum CANopen Receive-PDO frequency	f_{RPDO}			1	kHz	
Watchdog trigger frequency	f_{WDT}	0.5	1	2	kHz	Delayed max. 500 ms after reset
Maximum Power dissipation	P_{MAX}			300	mW	
Operating temperature	T_A	0		+70	°C	CO403xA-BD
	T_A	-40		+85	°C	CO403xAE-BD

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Package Dimension

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Schematic

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