



General Description

The CO401GW-EVA is an evaluation board for the high performance CANopen-Gateway-Chip CO401GW1. The chip enables serial connections to a standard CANopen network.

The Chip CO401-Gateway1 is implemented as CO401A-BD module. The CO401GW-Eva allows to start serial transmission to CANopen network immediately. It's only necessary to configure the serial baud rate and the CAN-baud rate and Identifier. A RS232 driver is on board and allows the connection to a standard asynchronous serial interface.

All configuration pins are wired to dipswitches and the I/O signals of the CO401GW1 chip are wired to plugs. Additionally the I/O signals of the CO401GW1 are indicated by LEDs and the inputs can be connected to low or high potential by jumper settings.

Applications

- Connection of microcontroller applications to CANopen networks
- CANopen slave controller for existing applications

Features

- Evaluation Board for CANopen-Gateway-Chip CO401GW1 - Interface for using UART with programmable baud rate
- According to CiA Draft Standards DS301 Version 4.0 and DS401 Version 2
- CAN Transceiver 80C251
- RS232 Drivers
- CAN baud rate up to 1MBit
- Watchdog output
- Dimensions (126mm x 80 mm)

CANopen Features

- 2 Transmit- and 2 Receive PDOs
- Variable PDO identifier
- All CANopen specific PDO transmission types supported: synchronous, asynchronous, event driven, cyclic, acyclic and remote frame dependent.
- Event timer and inhibit timer features for all transmit PDOs.
- Storing and restoring of object dictionary to non-volatile memory
- Node guarding, Life guarding, Heartbeat
- Emergency messages
- Minimum boot up

frenzel + berg electronic GmbH & Co.KG - Turmgasse 4 - 89073 Ulm - Germany - phone +49(0)731/970 570 - www.frenzel-berg.de



Configuration

The configuration of the CO401-Gateway-Chip will be set with dip switches SW1, SW2 and SW3.

DIP switch SW1									
	Switch Nr. and CO401 Pin							Function	
1	2	3	4	5	6	7	8		
CAN-	ID6	ID5	ID4	ID3	ID2	ID1	ID0		
Terminator									
ON								CAN-Terminator-Resistor On	
OFF	1							CAN-Terminator-Resistor OFF	
	Χ	Х	Χ	Х	Χ	Х	Х	Node ID	
	OFF	OFF	OFF	OFF	OFF	OFF	OFF	Node ID = Programmable ID	
	OFF	OFF	OFF	OFF	OFF	OFF	ON	Node ID = 1	
	OFF	OFF	OFF	OFF	OFF	ON	OFF	Node ID = 2	
	OFF	OFF	OFF	OFF	OFF	ON	ON	Node ID = 3	
	ON	ON	ON	ON	ON	ON	OFF	Node ID = 126	
	ON	ON	ON	ON	ON	ON	ON	Node ID = 127	

	DIP switch SW2								
Switch Nr. and CO401 Pin							Function		
1	2	3	4	5	6	7	8		
BD2	BD1	BD0	CFG2	CFG1	CFG0	EMY1#	EMY0#		
Χ	Χ	X						Baud rate selection	
OFF	OFF	OFF				1 Mbit / sec			
OFF	OFF	ON						800 kbit / sec	
OFF	ON	OFF						500 kbit / sec	
OFF	ON	ON						250 kbit / sec	
ON	OFF	OFF						125 kbit / sec	
ON	OFF	ON						50 kbit / sec	
ON	ON	OFF	.]					20 kbit / sec	
ON	ON	ON						10 kbit / sec	
			Χ	X	Х			Operation Mode (CFG1 and CFG2 are reserved for	
							future applications)		
		Χ	Χ	OFF			Digital inputs enabled		
		Χ	Χ	ON			Digital inputs disabled		
				Χ	Χ	Emergency Inputs			

DIP switch SW3							
Switch	Nr. and CO40)1 Pin	Function				
RSBD2	RSBD1	RSBD0	Serial Interface Baud Rate				
X	Х	X	nominal	exact			
OFF	OFF	OFF	9600	9615			
OFF	OFF	ON	4800	4807			
OFF	ON	OFF	2400	2404			
OFF	ON	ON	Reserverd	-			
ON	OFF	OFF	76900	76923			
ON	OFF	ON	38400	38461			
ON	ON	OFF	19200	19230			
ON	ON	ON	Reserved	-			



Jumper-Settings:

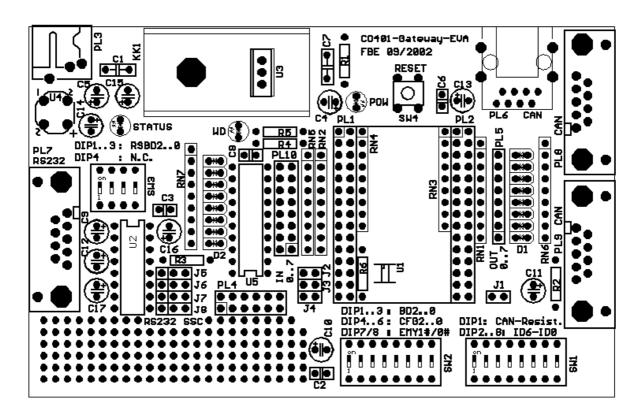
If the Jumper J1 is set after reset, the firmware update mode is activated.

With the jumpers J2, J3 and J4 the reference voltages for the AD-Converter can be applied to VCC and VSS.

The jumpers J5 and J6 are used to connect RSRXD and RSTXD to the on board RS232 driver or to the PIN-Header PL4 (TTL-levels).

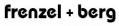
The jumpers J7 and J8 are used to connect SSC0 and SSC1 to the on board RS232 driver, working as CTS and RTS of a synchronous serial interface (for future applications), or to the PIN-Header PL4 (TTL-levels).

Placeplan



PL5 and PL10 are implemented to connect the I/O port bits to an application hardware using simple flat cable. PL10 also may be used to place any jumpers for activation of input bits.

PL4 is implemented to connect the asynchronous serial interface signals RSTXD and RSRXD on TTL Levels, the Emergency Inputs, as well as the signals off the synchronous serial interface for future applications.





Schematic

