## 2" X 2" Precision Hardware Solution

Design engineers now have a precision dual channel hardware solution that acts as its own evaluation board to facilitate algorithm development.

After the unit is programmed, SPP-01's can be directly inserted into production applications as a finished subassembly, minimizing product development time and space while shortening manufacturing cycle-time and providing repeatability.

### **Description**

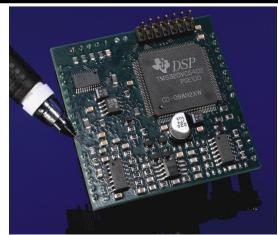
The SPP-01 Series of Signal Processing Platforms are programmable over a 20 kHz audio frequency range and offer up to 9-bits of addressing. This dual channel DSP design and development solution, in a 2" x 2" footprint, contains anti-alias filters, reconstruction filters, ADC's and DAC's sampling at 48 kHz. SPP-01 platforms are small subassemblies that provide low noise and distortion signal processing with THD approaching –100 dB. The fixed point DSP utilizes 32-bit math to achieve 24-bits of precision.

SPP-01's can be programmed with standard or customer specific algorithms. Algorithms are easily verified via an on-board JTAG port that allows the emulator to communicate with the SPP-01 hardware. Designers can directly load algorithms into the SPP-01 via the RS232 interface on the SPPDB-01 development board.

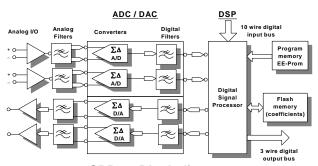
#### Features/ Benefits:

- Compact 2" x 2" dual channel design combined with large program memory (256 k EE-Prom) and 4 Mbits of flash memory optimizes your DSP processing power in minimal board space.
- Socketed SPPDB-01 development hardware offers rapid set-up, programming and performance evaluation, shortening the product development cycle while insuring high precision field installation.
- Analog inputs, storage for 100's of standard or customer application specific algorithms, and analog or digital outputs, provides unmatched flexibility for design and implementation.
- For multi-channel applications, design engineers can have phase synchronous operation by providing an external buffer to the SLAVE clock input.

## Dual Channel, Differential Input Signal Processing Platform



SPP-01 Platform



SPP-01 Block diagram

#### **Applications**

- Brick-Wall; High-Pass, Low-Pass, Band-Pass, Band-Reject and Multi-Rate filters with Linear Phase and Signal Generators for Data Acquisition Systems.
- Speech analysis, research, pathology
- Sound and vibration testing
- Signal correlation / data analysis
- Low distortion waveform generator: sine / cosine, quadrature or custom.

#### **AVAILABLE PLATFORM PRODUCTS**

**SPP-01:** Plug and play hardware / evaluation board, programmable with turnkey or customer generated algorithms.

**SPPDB-01:** Development Board, for SPP-01 family products. Also may be used as a mounting assembly.

**SPPDS-01:** Development Suite for all SPP platform products. Requires TI's Code Composer Studio<sup>™</sup>.

**SPPDF-01:** Development Suite for SPPDM-01 FIR filter products. Requires MatLab<sup>TM</sup> V5.3 or V6.0.

## Dual Channel, Differential Input Signal Processing Platform

## **Typical Program Selection Port Protocol**

## Suggested 8 - Bit programming table

## **Data Format**

Logic "0" 0VDC Min – 2VDC Max
 Logic "1" 3.5VDC Min – 5Vdc Max

Bit Weighting (Binary Coded)

Hardware Solution

 $\begin{array}{cc} D_0 & \quad \text{LSB} \\ D_7 \, \text{or} \, D_8 & \quad \text{MSB} \end{array}$ 

Program Selection: 256 or 512

| MSB                              |                                  |                                  |                                  |                                  |                                  |                                  | LSB                              | Bit<br>Weight      |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|--------------------|
| 2 <sup>7</sup><br>D <sub>7</sub> | 2 <sup>6</sup><br>D <sub>6</sub> | 2 <sup>5</sup><br>D <sub>5</sub> | 2 <sup>4</sup><br>D <sub>4</sub> | 2 <sup>3</sup><br>D <sub>3</sub> | 2 <sup>2</sup><br>D <sub>2</sub> | 2 <sup>1</sup><br>D <sub>1</sub> | 2 <sup>0</sup><br>D <sub>0</sub> | Program<br>address |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1                  |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 2                  |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 4                  |
| 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 8                  |
| 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 16                 |
| 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 32                 |
| 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 64                 |
| 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 128                |
| 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 256                |

## Suggested 9 - Bit programming table

- 1. The program selection data word bus consists of  $D_0$  to  $D_7$  for 8 bit programming ( $D_8 = 0$  Channel 1 and logic 1 for Channel 2) and  $D_0$  to  $D_8$  for 9-bit programming.
- 2.  $D_9$  channel 1 or 2 select. Low is channel 1 and is logic 0. Channel 2 is a logic 1 and is high at 5 volts.

| MSB                              |                                  |                                  |                                  |                                  |                                  |                                  |                                  | LSB                              | Bit<br>Weight   |
|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|-----------------|
| 2 <sup>8</sup><br>D <sub>8</sub> | 2 <sup>7</sup><br>D <sub>7</sub> | 2 <sup>6</sup><br>D <sub>6</sub> | 2 <sup>5</sup><br>D <sub>5</sub> | 2 <sup>4</sup><br>D <sub>4</sub> | 2 <sup>3</sup><br>D <sub>3</sub> | 2 <sup>2</sup><br>D <sub>2</sub> | 2 <sup>1</sup><br>D <sub>1</sub> | 2 <sup>0</sup><br>D <sub>0</sub> | Program address |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1               |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 2               |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 4               |
| 0                                | 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 8               |
| 0                                | 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 16              |
| 0                                | 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 32              |
| 0                                | 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 64              |
| 0                                | 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 128             |
| 0                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 256             |
| 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 1                                | 512             |



# 2" X 2" Precision Hardware Solution

## Dual Channel, Differential Input Signal Processing Platform

| SPP-01   |                           |  |  |  |  |
|--|---------------------------|--|--|--|--|
| Performance Specifications   |                           |  |  |  |  |
| Available bandwidth  | DC to 20 kHz              |  |  |  |  |
| Frequency Accuracy   | < ± 0.05 %                |  |  |  |  |
| Amplitude Accuracy at unity gain.                                      | < ± 0.1 dB                |  |  |  |  |
| Total Broad Band Noise<br>(Ref to input 3.53 VRMS)                     | < -100dB Max              |  |  |  |  |
| Total Harm. Dist.(THD) (10V peak to peak)                              | <-100 dB Max. to 20 kHz   |  |  |  |  |
| Channel to Channel phase tracking                                      | < ± 0.10°                 |  |  |  |  |
| Cross talk dual channel version with different signals on each channel | DC to 20K < - 100 dB Typ. |  |  |  |  |

There are two development systems available for SPP platforms.

## **Development Options:**

- SPPDS-01: Suite for all SPP platform products.
  - Requires Tl's Code Composer Studio<sup>TM</sup>.
- 2. **SPPDF-01:** Suite for SPPDM-01 FIR filters. Requires MatLab<sup>TM</sup> V5.3 or V6.0.

All SPP-01 Family Platforms can be purchased with standard and custom algorithms.

Consult factory for a quotation.

Custom programs will be assigned a unique suffix (CXX) at the time of order.

(@25°C and  $Vs = \pm 15 Vdc$ )

## **Analog Input Characteristics**

 $\begin{array}{ll} \text{Maximum Input Impedance} & 1.0 \text{ M}\Omega \\ \text{Input voltage} & \pm 10 \text{ V peak} \end{array}$ 

#### **Analog Output Characteristics**

 $\begin{array}{lll} \mbox{Minimum load Impedance} & 10 \ \mbox{k}\Omega \\ \mbox{Maximum capacitive load} & 50 \ \mbox{pF} \\ \mbox{Output voltage} & \pm 10 \ \mbox{V peak} \\ \mbox{Offset Voltage} & 2 \ \mbox{mV Typ. } 10 \mbox{mV Max}. \end{array}$ 

### Power Supply (±Vs)

Analog Vs range ±12Vdc Min to ±15 Vdc Max.

Analog supply current at Max. Vs 70 mA Typ.

Digital PS Voltage +5 Vdc

Digital supply current 370 mA Typ.

Power consumption at Max. Vs 4.0 watts Typ.

Care must be taken to stay above the minimum Vs in order to maintain the linearity and distortion performance of the DSP platform.

#### **Temperature**

Operating  $0 \text{ to } +70^{\circ}\text{C}$ Storage  $-25 \text{ to } +85^{\circ}\text{C}$ Size  $2.0^{\circ} \times 2.0^{\circ} \times 0.5^{\circ}$ 

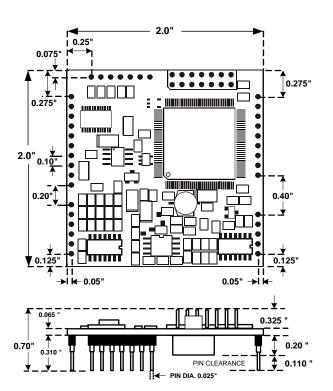
The **SPPDB-01** development board can double as an SPPDM-01 mounting assembly, to facilitate product evaluation or laboratory use. The **SPPDB-01** development board is specified and sold separately or is shipped as part of the SPPDS-01 and SPPDF-01 development suites.

## **Specifications**

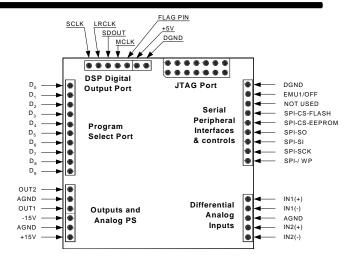


Hardware Solution

## Dual Channel, Differential Input Signal Processing Platform



SPP-01 AND SPPPF-01 TOP VIEW AND DIMENSIONS All normal pin spacing 0.10"



## SPP-01 TOP VIEW PIN IDENTIFICATION

 $D_0 - D_8$  9-bit program select pins

D<sub>8\*</sub> \*8-bit Ch select; Ch 1= 0, Ch 2=1

D<sub>9</sub> Channel 1 or 2 select

Out 1 & 2 Analog outputs

±Inputs 1&2 Differential analog inputs ± 15 Vdc Analog Dc power In + 5 Vdc Digital Power In A Gnd Analog Grounds (3) D Gnd Digital Grounds (2)

JTAG<sup>™</sup> JTAG port, see SPPDS-01

## **Ordering information**

SPP-01M MASTER

SPP-01S SLAVE

**SPP-01M or S- CXX** Custom algorithms

will be individually quoted.

We hope the information given here will be helpful. The information is based on data and our best knowledge, and we consider the information to be true and accurate. Please read all statements, recommendations or suggestions herein in conjunction with our conditions of sale which apply to all goods supplied by us. We assume no responsibility for the use of these statements, recommendations or suggestions, nor do we intend them as a recommendation for any use which would infringe any patent or copyright.