



Application Notes

AN_370

FT60X Configuration Programmer User Guide

Version 1.3

Issue Date: 2016-07-07

This document provides a guide on how to use the FT60X Chip Configuration Programmer application for customizing the chip configuration.

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1 Introduction

This document explains how to use the FT60X Series Chip Configuration Programmer, a utility application for customizing the chip configuration.

1.1 Overview

The FT600 and FT601 are the first USB devices in a brand new SuperSpeed series from FTDI Chip. The devices provide a USB 3.0 SuperSpeed to FIFO Bridge, with up to 5Gbps of bandwidth. Delivering the option of 16 bit (FT600) and 32 bit (FT601) wide parallel FIFO interfaces; the FT60X series enables connectivity for numerous applications including high resolution cameras, displays, multifunction printers and much more.

During initialization, the FT60X devices read configuration data and initialize the system using these values. If the chip configuration data read is empty or invalid, the default chip configuration data will be used. The Chip Configuration Programmer application allows the user to get, set or update this chip configuration data.

1.2 Prerequisite

A PC running Windows 7 Operating System or greater is required.

The PC should also be installed with D3XX Direct Drivers. FT60X uses D3XX (FTDI's latest USB driver targeted for USB 3.0 SuperSpeed devices). They can be obtained here:

<http://www.ftdichip.com/Drivers/D3XX.htm>

The PC should also be installed with the Microsoft Visual C++ 2013 Redistributable (x86) package. Please use the following steps to install it:-

1. Go to <https://www.microsoft.com/en-us/download/details.aspx?id=40784>
2. Click '**Download**' button
3. Check the '**vc redistrib_x86.exe**' and click '**Next**'.
4. After download completes, run '**vc redistrib_x86.exe**' to install the package

2 User Interface

Below is a screenshot of the FT60X Chip Configuration Programmer application.

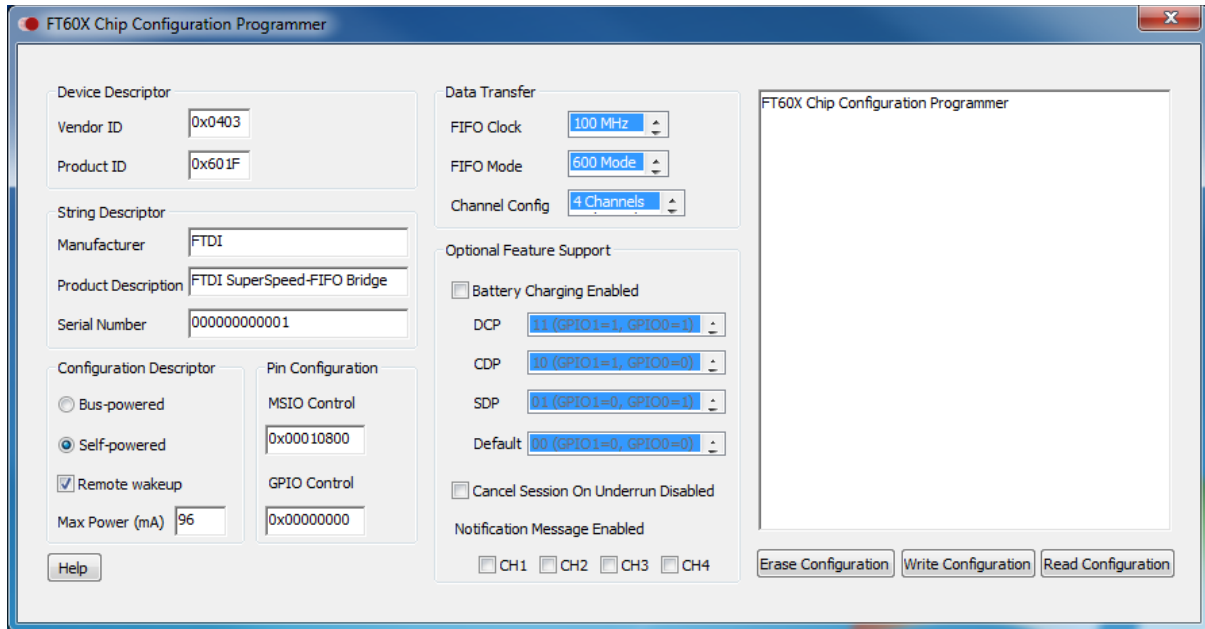


Figure 2.1 Application Screenshot

The application allows the user to reset/clear, write and read the device configuration.

Main Buttons	Description
Erase Configuration	Clicking this button will erase the custom configuration in the device. After erasing, the chip will automatically reset using its default configuration and the application template values will also change to reflect the configuration from the chip.
Write Configuration	Clicking this button will set the custom configuration that the user has selected. The chip will automatically reset using the new configuration.
Read Configuration	Clicking this button will show the current settings that the device is configured with.

Table 2.1 Description of Main UI Controls

Note: when changing FIFO Clock, or any of the drop-down menus, you must scroll to the selected item and click on it. Make sure the selection is highlighted in blue before writing the configuration. If the selection is not highlighted, the chip configuration will not change.

3 Chip Configuration Configurable

Controls	Default Value	Description
Vendor ID	0x0403	<p>Vendor identification as specified in the idVendor field of the USB Device Descriptor</p> <p>This should match the VID in the Windows installation file (INF).</p> <p>If this parameter is changed, then the corresponding change is required in the INF installation file.</p> <p>NOTE: changes to the INF file will invalidate any driver certification.</p>
Product ID	0x601F	<p>Product identification as specified in the idProduct field of the USB Device Descriptor</p> <p>This should match the PID in the Windows installation file (INF).</p> <p>If this parameter is changed, then the corresponding change is required in the INF installation file.</p> <p>NOTE: changes to the INF file will invalidate any driver certification.</p>
Manufacturer	FTDI	Name of Manufacturer as specified in the USB Device Descriptor
Product Description	FTDI SuperSpeed-FIFO Bridge	Product name as specified in the USB Device Descriptor
Serial Number	000000000001	<p>Serial Number as specified in the USB Device Descriptor</p> <p>The Serial Number field may be customised to uniquely identify a device and does not require the INF file to be updated.</p> <p>The total number of bytes for this field is 128 bytes, which is shared across the string descriptors for Manufacturer, Product Description and Serial Number.</p>
Bus-powered/Self-powered	Self-powered	Bus-powered or self-powered capability as specified in Bit 6 of the bmAttributes field of the USB Configuration Descriptor
Remote Wakeup	Enabled	Remote wakeup capability as specified in the bmAttributes field of the USB Configuration Descriptor
Max Power	96 (mA)	Maximum power consumption derived from the bMaxPower field of the USB Configuration Descriptor. This value is equivalent to bMaxPower/8 if USB 3 and bMaxPower/2 if USB 2.
FIFO Clock	100 MHz	Clock speed of the FIFO in MHz

Controls	Default Value	Description
FIFO Mode	600 Mode	<p>Mode of the FIFO (245 mode or 600 mode)</p> <p>Note that FIFO mode selected should match the protocol used by the external FIFO master.</p> <p>Data transfer will not work if the FIFO protocol used does not match.</p>
Channel Configuration	4 Channels	<p>Number of channels or pipes. A channel is equivalent to 2 pipes – 1 for OUT and 1 for IN. (4 channels, 2 channels, 1 channel, 1 OUT pipe only, 1 IN pipe only)</p> <p>Note that maximum performance decreases as the number of pipes increases. To achieve maximum performance, use as few pipes or channels as possible.</p>
Battery Charging Enabled	Disabled	Enables/disables detection of the power source type. E.g. Standard Downstream Port (SDP), Charging Downstream Port (CDP) or Dedicated Charging Port (DCP)
Battery Charging Settings	DCP (11) CDP (10) SDP (01) Default (00)	GPIO Pin Configuration used to indicate the type of power source detected by the Battery Charging module of the chip.
Cancel Session On Underrun Disabled	Not set	<p>Enable/disable the ability to cancel sessions when the chip receives an underrun from the FIFO master.</p> <p>When this is set, the chip will not cancel or invalidate IN requests from the host application when it receives an underrun condition from the FIFO master and if the packet size received from the FIFO master is a multiple of the USB max packet size (USB3:1024, USB2:512).</p> <p>By default, the chip always cancels or invalidates IN requests from the host application when it receives an underrun condition from the FIFO master.</p> <p>Underrun conditions happen when the FIFO master provides data less than the FIFOsegmentSize. The FIFOsegmentSize is as follows:</p>

Controls	Default Value	Description
		CHANNEL_CONFIG_4: 1KB CHANNEL_CONFIG_2: 2KB CHANNEL_CONFIG_1: 4KB CHANNEL_CONFIG_1_OUTPIPE: 8KB CHANNEL_CONFIG_1_INPIPE: 8KB
Notification Message Enabled	Disabled for all IN pipes	<p>Enables/disables sending of a notification message for unexpected IN data where there is no existing read requests.</p> <p>When this is set on a pipe, the host application should not actively read on this pipe, instead it will register a callback function. The callback function will be called when there is data available for the pipe.</p> <p>This feature is intended for unexpected short packets (maximum of 4kb), such as error status information from the FIFO master to the host application.</p> <p>For example, for a camera device, the user can select 2-channel configuration because it needs 2 IN pipes – 1 for camera data, 1 for control/error status information. Notification messages should be used for the control/error status information pipe but not for the camera data pipe.</p>
MSIO Control	0x00010800	<p>Configuration to control the drive strengths of the FIFO pins</p> <p>Bit 1-0: Output driving strength setting for FIFO data bus</p> <p>2'b00: 50 ohm (default)</p> <p>2'b01: 35 ohm</p> <p>2'b10: 25 ohm</p> <p>2'b11:18 ohm</p> <p>Bit 5-4: Output driving strength setting for FIFO clock</p> <p>2'b00: 50 ohm (default)</p> <p>2'b01: 35 ohm</p> <p>2'b10: 25 ohm</p> <p>2'b11:18 ohm</p>
GPIO Control	0x00000000	<p>Configuration to control the drive strengths of the GPIO pins</p> <p>Bit 9-8: Output driving strength setting for gpio0</p> <p>2'b00: 50 ohm (default)</p> <p>2'b01: 35 ohm</p> <p>2'b10: 25 ohm</p> <p>2'b11:18 ohm</p>

Controls	Default Value	Description
		Bit 11-10: Output driving strength setting for gpio1 2'b00: 50 ohm (default) 2'b01: 35 ohm 2'b10: 25 ohm 2'b11:18 ohm

Table 3.1 Description of User Configurable

FTDI provides a set of APIs to query and set the chip's configuration. Please refer to the [D3XX Programmer's Guide](#).

4 Chip Configuration Initialization Status

When the user clicks on the **Read Configuration** button, the current configuration values used during initialization will be displayed, including the status information. The status reflects the FT60X actual configuration result when the chip has completed the startup process. Below is a table showing the description of the status information of the chip configuration initialization.

Status Information	Values	Description
Custom Configuration Validity	Invalid or Valid	Indicates whether the configuration data read is valid or not. If custom configuration is invalid, chip will use the default configuration.
Custom Configuration Checksum	Invalid or Valid	Indicates whether the configuration data is corrupted or not by validating the checksum. If the custom configuration checksum is invalid, the chip will use the default configuration.
GPIO Input	Used or Ignored	Indicates whether the GPIOs are used as configuration input. Note that the GPIOs will only be used as a configuration input when the device is running a default configuration. Below is the pin setting corresponding to mode and channel configuration. GPIO1 0 – GPIO0 0 – 245 mode – 1 channel GPIO1 0 – GPIO0 1 – 600 mode – 1 channel GPIO1 1 – GPIO0 0 – 600 mode – 2 channels GPIO1 1 – GPIO0 1 – 600 mode – 4 channels
GPIO 0	High or Low	Indicates whether GPIO is set to high or low .
GPIO 1	High or Low	Indicates whether GPIO is set to high or low .
Configuration Used	Default or Custom	Indicates whether chip was initialized using some custom chip configuration or the default chip configuration.

Table 4.1 Status Information of Chip Configuration Initialization

Below is a sample illustration where the device is detected to be running using the default chip configuration.

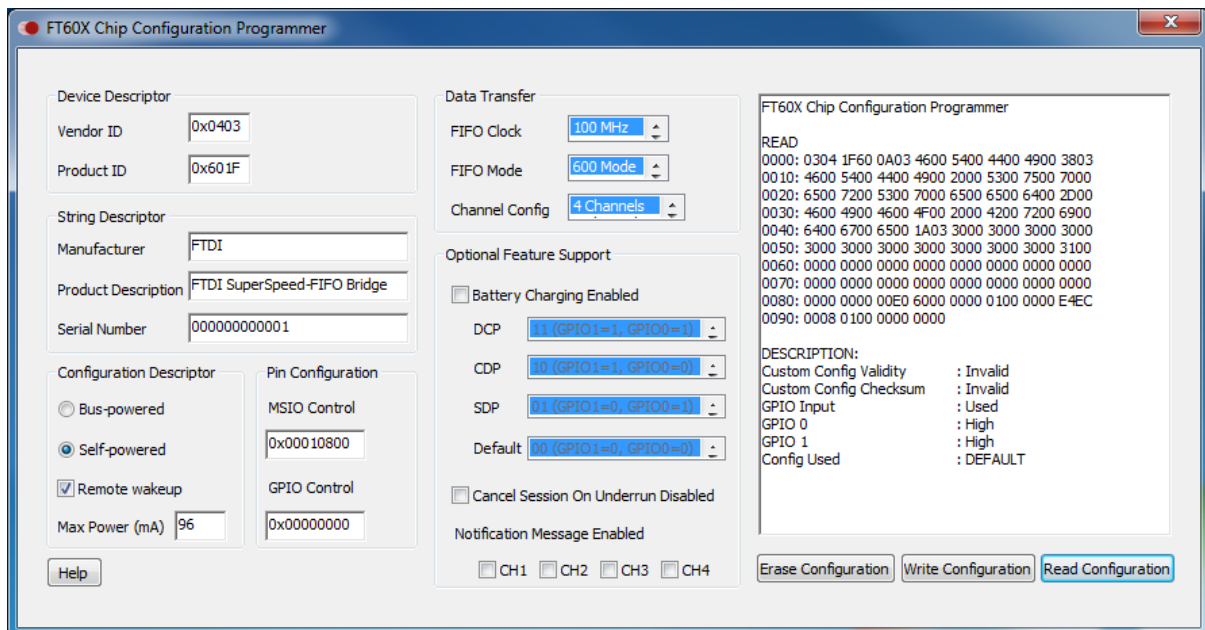


Figure 4.1 Chip Configuration Status - Default Chip Configuration

Below is a sample illustration where the device is detected to be running using some custom chip configuration. If user wants to go back to the default chip configuration, the user can click on the Erase Configuration button. This will erase the custom setting in the chip.

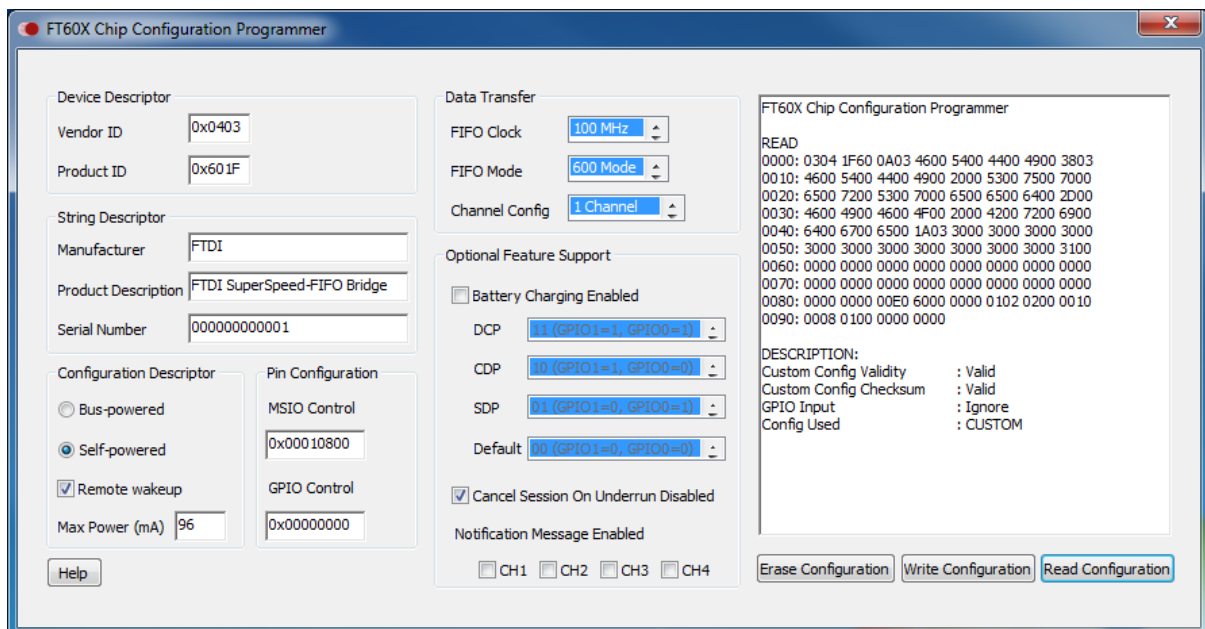


Figure 4.2 Chip Configuration Status - Custom Chip Configuration

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Appendix A – References

Document References

[FT600Q-FT601Q SuperSpeed USB3.0 IC Datasheet](#)

[DS_UMFT60xx module datasheet](#)

[D3XX Programmer's Guide](#)

Acronyms and Abbreviations

Terms	Description
CDP	Charging Downstream Port
DCP	Dedicated Charging Port
FIFO	First In First Out
GPIO	General Purpose Input / Output
ID	Identification
INF	Windows driver installation file
SDP	Standard Downstream Port
UI	User Interface
USB	Universal Serial Bus
VID	Vendor Identification

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Appendix C – Revision History

Document Title: AN_370 FT60X Configuration Programmer User Guide
Document Reference No.: FT_001164
Clearance No.: FTDI#460
Product Page: <http://www.ftdichip.com/FTPProducts.htm>
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Revision	Changes	Date
1.0	Initial Release	2015-09-03
1.1	In Section 3.Chip Configuration Configurable table, updated the following parameters - Controls -> FIFO Clock; Default Value->100 MHZ;	2015-12-21
1.2	Updated Section 1.2 Prerequisites	2016-04-05
1.3	Updated section 3, to remove the references to GPIO2.	2016-07-07