General Standards Corporation

*High Performance Bus Interface Solutions*

**Rev: 040213**

# *PMC-16AICS32,*
# *CCPMC-16AICS32R*

## 32-CHANNEL 16-BIT
## TRANSDUCER INPUT PMC

***With Scanning Input Current Source***

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# REFERENCE MANUAL

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# SECTION 1.0

# INTRODUCTION

## 1.1 General Description

The PMC-16AICS32 board is a single-width PCI mezzanine card (PMC) that provides 16-bit analog input capability for PMC applications. 64 analog input lines can be configured either as 64 single-ended input channels or as 32 differential channels, and are digitized at rates up to 100,000 conversions per second. Current excitation can be selectively applied to as many as 32 input channels. The voltage range is software controlled as ±2.5V, ±5V or ±10V. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

Power requirements consist of +5 VDC from the PCI bus in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PMC-16AICS32 product specification. Figure 1.1-1 shows the physical configuration of the board, and the general arrangement of major components.

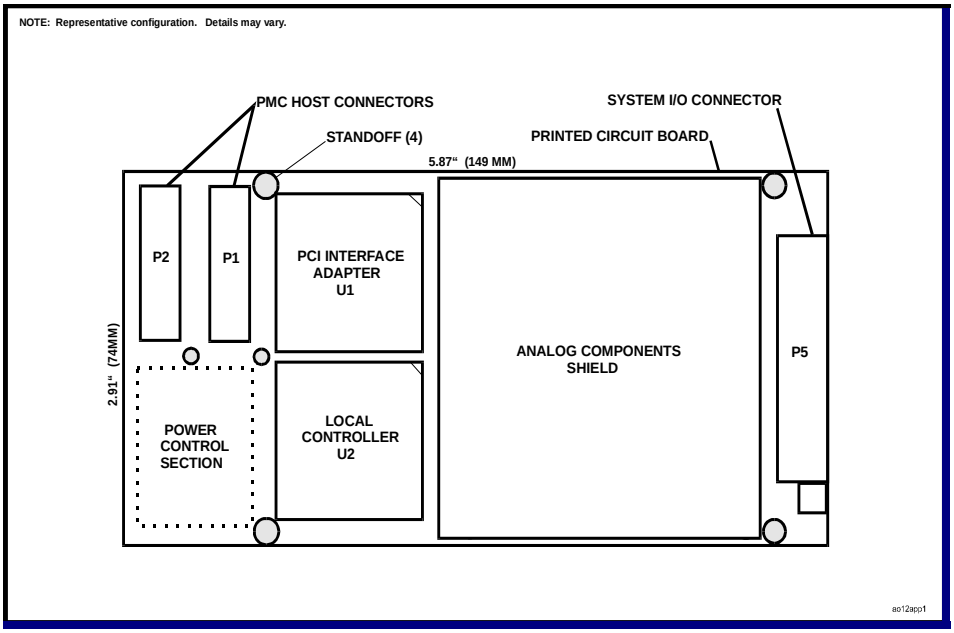


**Figure 1.1-1. Physical Configuration**

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that minimize the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 68-pin, dual-ribbon front-access I/O connector.

## 1.2 Functional Overview

Principal capabilities of the PMC-16AICS32 board are summarized in the following list of features:

- ❑ 64 Single-Ended or 32 Differential 16-Bit Scanned Analog Input Channels
- ❑ Transducer Scanning Excitation Current Available on 32 Inputs
- ❑ Software-Selectable Analog Input Ranges of ±10V, ±5V or ±2.5V
- ❑ Precision Current Excitation for Resistance Transducers; 0.4ma to 10ma options
- ❑ 64K-Sample Analog Input FIFO Buffer
- ❑ Conversion Rates to 100 KSPS
- ❑ Multiple-Channel and Single-Channel Input Scanning Modes
- ❑ Dual cascadable Internal Rate Generators
- ❑ Supports Multiboard Synchronization of Analog Inputs
- ❑ Internal Autocalibration
- ❑ DMA Engine

The PMC-16AICS32 board is a scanning analog digitizer that performs sampling and 16-bit A/D conversion of as many as 64 single-ended or 32 differential analog input channels. The resulting 16-bit sampled data is available to the PCI bus through a 64K-sample FIFO data buffer. A scanning precision current source can be assigned as excitation for up to 32 input channels to support resistance transducers such as RTD's. All operational parameters are software configurable.

The analog inputs can be sampled in scans of 2, 4, 8, 16, 32 or 64 single-ended channels, or in scans of 2, 4, 8, 16 or 32 differential channels. Or any single channel can be monitored. The scan rate can be controlled internally or externally up to 50,000 scans per second for a 2-channel scan. Sync input and output signals permit multiple boards to perform synchronous scanning.

An internal autocalibration utility corrects for offset and gain errors in the input signal path. A selftest switching network routes calibration signals through the input multiplexer to the A/D converter to support internal autocalibration, and permits board integrity to be tested by the host. Autocalibration is performed on demand from the PCI bus, and calibrates the offset and gain of the A/D converter to a precision internal reference voltage.

## 1.3 Conduction-Cooled Version

The PMC-16AICS32 is also available in a conduction-cooled configuration as the CCPMC-16AICS31R, which implements rear-panel system access. Refer to the CCPMC-16AICS31R product specification for details.

# SECTION 2.0

# INSTALLATION AND MAINTENANCE

## 2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

## 2.2 Installation

### 2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs and bezel are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

### 2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with a 68-pin dual-ribbon connector, equivalent to AMP #749621-7. The insulation displacement (IDC) cable connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. Contact the factory if preassembled cables are required.

**NOTE: Refer to the CCPMC-16AICS32R product specification for details pertaining to system I/O connections for the conduction-cooled version of this product.**

## Table 2.2-1. System I/O Connector Pin Functions

**(Standard air-cooled product configuration)**

| | ROW-A SIGNAL | |
|---|---|---|
| PIN | S.E. MODE | DIFF MODE |
| 1 | INP00 * | INP00 HI * |
| 2 | INP01 * | INP00 LO |
| 3 | INP02 * | INP01 HI * |
| 4 | INP03 * | INP01 LO |
| 5 | INP04 * | INP02 HI * |
| 6 | INP05 * | INP02 LO |
| 7 | INP06 * | INP03 HI * |
| 8 | INP07 * | INP03 LO |
| 9 | INP08 * | INP04 HI * |
| 10 | INP09 * | INP04 LO |
| 11 | INP10 * | INP05 HI * |
| 12 | INP11 * | INP05 LO |
| 13 | INP12 * | INP06 HI * |
| 14 | INP13 * | INP06 LO |
| 15 | INP14 * | INP07 HI * |
| 16 | INP15 * | INP07 LO |
| 17 | AGND | AGND |
| 18 | AGND | AGND |
| 19 | INP16 * | INP08 HI * |
| 20 | INP17 * | INP08 LO |
| 21 | INP18 * | INP09 HI * |
| 22 | INP19 * | INP09 LO |
| 23 | INP20 * | INP10 HI * |
| 24 | INP21 * | INP10 LO |
| 25 | INP22 * | INP11 HI * |
| 26 | INP23 * | INP11 LO |
| 27 | INP24 * | INP12 HI * |
| 28 | INP25 * | INP12 LO |
| 29 | INP26 * | INP13 HI * |
| 30 | INP27 * | INP13 LO |
| 31 | INP28 * | INP14 HI * |
| 32 | INP29 * | INP14 LO |
| 33 | INP30 * | INP15 HI * |
| 34 | INP31 * | INP15 LO |

| | ROW-B SIGNAL | |
|---|---|---|
| PIN | S.E. MODE | DIFF MODE |
| 1 | INP32 | INP16 HI * |
| 2 | INP33 | INP16 LO |
| 3 | INP34 | INP17 HI * |
| 4 | INP35 | INP17 LO |
| 5 | INP36 | INP18 HI * |
| 6 | INP37 | INP18 LO |
| 7 | INP38 | INP19 HI * |
| 8 | INP39 | INP19 LO |
| 9 | INP40 | INP20 HI * |
| 10 | INP41 | INP20 LO |
| 11 | INP42 | INP21 HI * |
| 12 | INP43 | INP21 LO |
| 13 | INP44 | INP22 HI * |
| 14 | INP45 | INP22 LO |
| 15 | INP46 | INP23 HI * |
| 16 | INP47 | INP23 LO |
| 17 | AGND | AGND |
| 18 | AGND | AGND |
| 19 | INP48 | INP24 HI * |
| 20 | INP49 | INP24 LO |
| 21 | INP50 | INP25 HI * |
| 22 | INP51 | INP25 LO |
| 23 | INP52 | INP26 HI * |
| 24 | INP53 | INP26 LO |
| 25 | INP54 | INP27 HI * |
| 26 | INP55 | INP27 LO |
| 27 | INP56 | INP28 HI * |
| 28 | INP57 | INP28 LO |
| 29 | INP58 | INP29 HI * |
| 30 | INP59 | INP29 LO |
| 31 | INP60 | INP30 HI * |
| 32 | INP61 | INP30 LO |
| 33 | INP62/ SYNC HI ** | INP31 HI/ * SYNC HI ** |
| 34 | INP63/ SYNC LO ** | INP31 LO/ SYNC LO ** |

* Selectable for current excitation

** Software-selected Sync I/O.

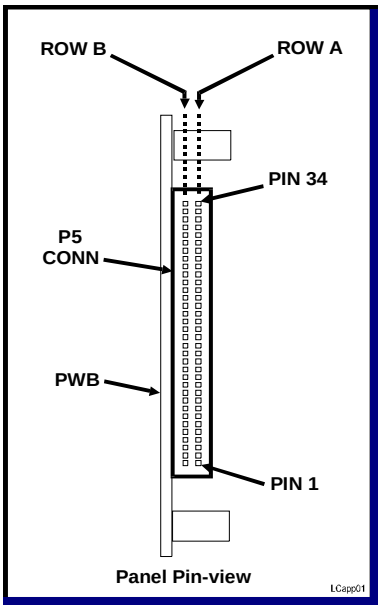


**Figure 2.2-1. Input/Output Connector**

## 2.3 System Configuration

### 2.3.1 Analog Inputs

#### 2.3.1.1 Single-Ended Inputs

Analog inputs can be configured either as 64 single-ended channels or as 32 differential channels. The hardware input configuration must be acknowledged by the control software, which configures the controller for either single-ended or differential operation. High-resistance pull-down resistors are provided on all analog inputs. Table 2.2-1 provides separate pin assignment columns for single-ended and differential input configurations.

Single-ended operation (Figure 2.3-1b) offers the maximum number of input channels, but generally provides optimum performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or may generate excessive ground current and damage the board.

#### 2.3.1.2 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other and have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum acceptable measurement error.

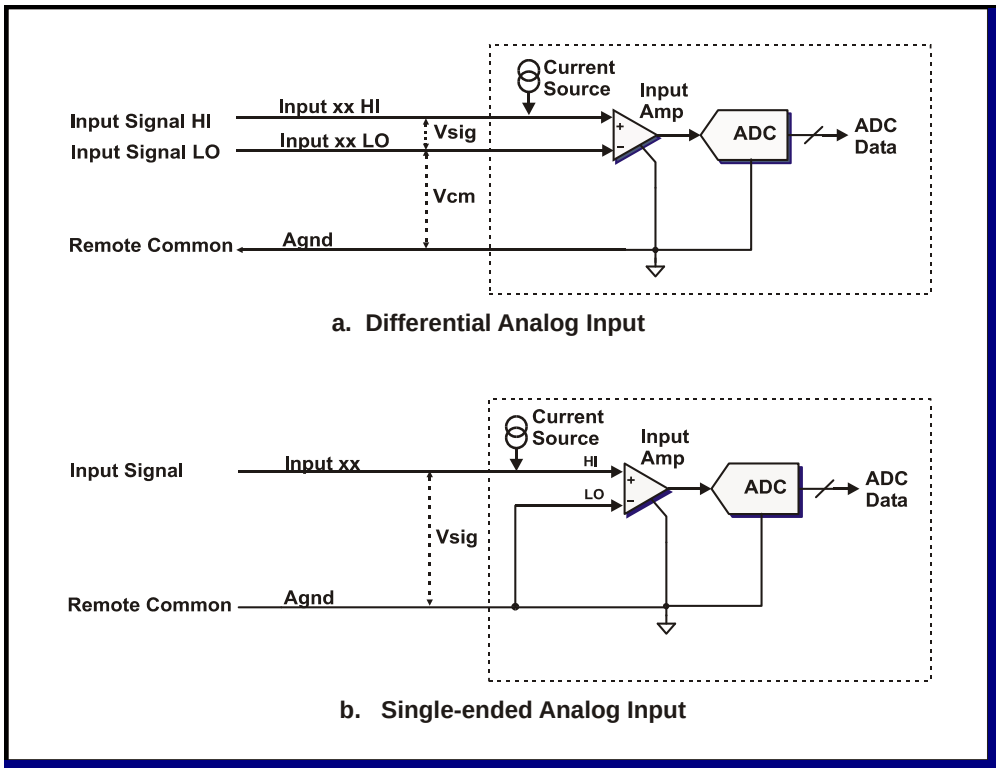


**Figure 2.3-1. Analog Input Configurations**

Differential operation also offers the highest rejection of the common mode noise that is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode (Figure 2.3-1a), the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (AGND in Table 2.2-1) is connected to a ground point that ensures that the common mode voltage of all signals remains within the range specified for the board.

### 2.3.1.3 Excitation Current Source

An excitation current source (Figure 2.3.1) can be connected to any input channel as the channel is scanned in the multiplexer sequence. Application software assigns the excitation to as many as 32 input channels, as indicated in Table 2.2-1.

### 2.3.2 External Sync

Pins 33 and 34 of I/O connector Row-B can be software-configured as a bidirectional TTL SYNC signal that provides external control of analog input scan timing. The SYNC signal is present on the SYNC HI pin, and is referenced to the SYNC LO pin, which is connected internally to digital ground.

When configured as an input, this signal initiates a single scan of all active input channels. The SYNC input signal is asserted LOW, and is pulled HIGH internally through a 4.7 KOhm resistor. Minimum input pulse width is 100 nanoseconds.

When configured as an output, the SYNC signal is asserted for approximately 130 nanoseconds at the beginning of each scan. The SYNC output signal is a TTL level that is available for synchronizing the operation of multiple target boards to a single initiator board. Like the SYNC input signal, the SYNC output signal is asserted LOW. Loading of the SYNC output should be limited to 10 milliamps or less.

Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

### 2.3.3 Multiboard Synchronization

If multiple boards are to be synchronized together, the SYNC HI and LO pins from one board, the *initiator*, are connected to the SYNC HI and LO pins of as many as eight *target* boards (Figure 2.3-2). The controlling software determines specific synchronization functions.

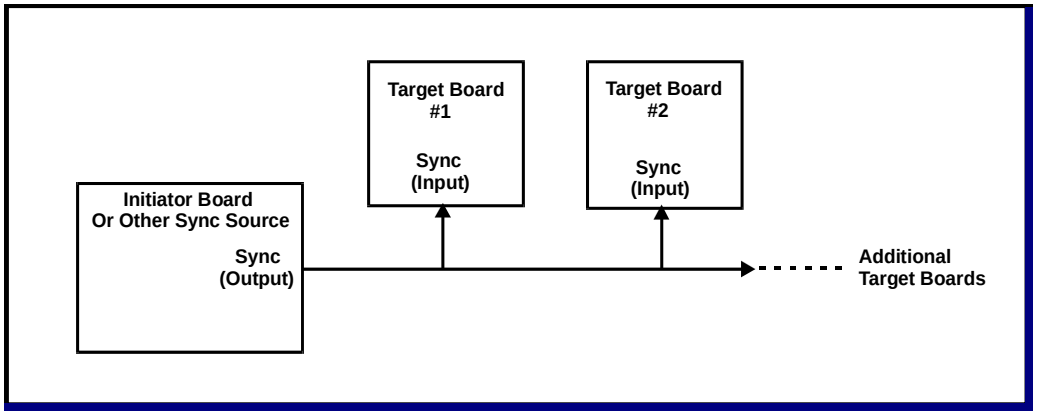


**Figure 2.3-2. Multiboard Synchronization**

## 2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic verification of the internal voltage reference and current source, and possible adjustment of these functions. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that is suspected to be defective should be returned to the factory for detailed problem analysis and repair.

## 2.5 Reference Voltage and Current Source Verification

All analog input channels are software-calibrated to a single internal voltage reference by an embedded autocalibration software utility. A precision internal current source provides excitation current for input transducers, and is not adjusted during autocalibration. The procedure presented here describes the verification and adjustment of the voltage reference and current source.

### 2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

**Table 2.5-1. Calibration Verification Equipment**

| EQUIPMENT DESCRIPTION | MANUFACTURER | MODEL |
|---|---|---|
| Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts. 0.02% accuracy for DC current measurement in the range of 0.4-3.0ma. | Hewlett Packard | 34401A |
| Host board with single-width PMC adapter | (Existing host) | --- |
| Test cable; suitable for connecting the digital multimeter to two 0.024-inch square test posts. | --- | --- |

### 2.5.2 Verification and Adjustment

This procedure describes the verification and adjustment of the reference voltage and current source that ensure conformance to the product specification. Adjustment of the voltage reference or current source, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1. A right-angle 0.024-inch pin header provides side-access to the necessary test points.

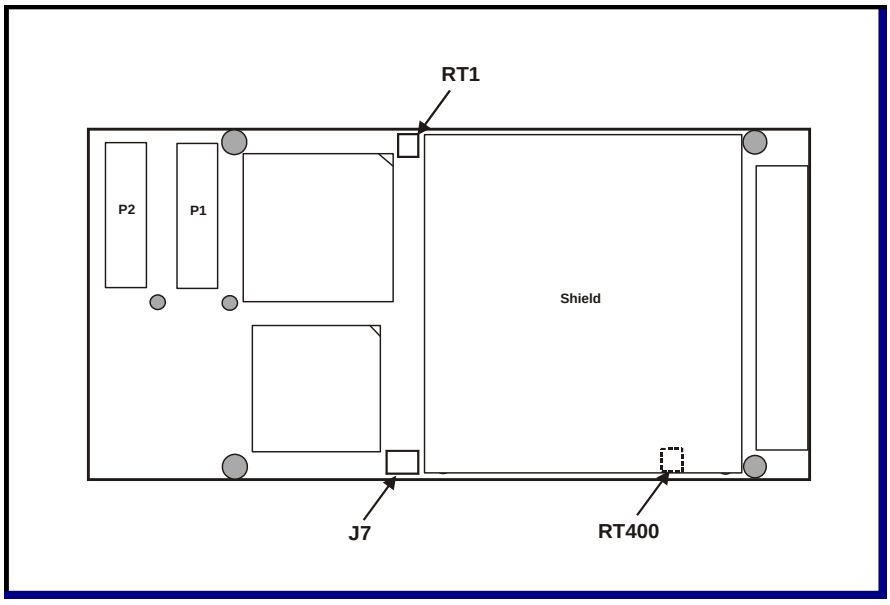


**Figure 2.5-1. Calibration Adjustment Access**

This procedure assumes that the board is installed on a host board, and that the host is installed in an operating system. The board must be in the default (reset) operating mode while these adjustments are performed.

1. Adjust the multimeter for ***voltage measurement***, and connect the multimeter between the VTEST Pin-1 (+) and the REF RTN Pin-2 (-) in J7 at the edge of the board (Figure 2.5-1). Reverse the test leads if a negative voltage is indicated.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is +9.4780 VDC ±0.0009 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer RT1 until the digital multimeter indication is within the specified range.
4. Move the digital multimeter (+) connection to the CURRENT TEST Pin-5 in J7, and ***adjust for current measurement***.
5. Verify that the digital multimeter indication is as indicated below for the current source installed on the board.

    - (0.4ma): 0.4000±0.0002ma,
    - (1.0ma): 1.0000±0.0004ma,
    - (2.0ma): 2.0000±0.0008ma,
    - (3.0ma): 3.0000±0.0012ma,
    - (5.0ma): 5.0000±0.0020ma,
    - (10.0ma): 10.0000±0.0040ma.

    If the multimeter indication is not within this range, adjust the CURRENT SOURCE trimmer RT400 until the digital multimeter indication is within the specified range.
6. Verification and adjustment is completed. Remove all test connections.

# SECTION 3.0

# CONTROL SOFTWARE

## 3.1 Introduction

The PMC-16AICS32 board is compatible with the PCI Local Bus specification, and supports auto configuration at the time of power-up. A PLX™ PCI-9080 adapter device controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space. After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer.

**Table 3.1-1. Control and Data Registers**

| OFFSET (Hex) | REGISTER | ACCESS MODE * | DEFAULT | PRIMARY FUNCTION |
|---|---|---|---|---|
| 0000 | BOARD CONTROL (BCR) | R/W | 0000 4060h | Board Control Register (BCR) |
| 0004 | INTERRUPT CONTROL | R/W | 0000 0008h | Interrupt conditions and flags |
| 0008 | INPUT DATA BUFFER | RO | --- | Analog input data buffer |
| 000C | INPUT BUFFER CONTROL | R/W | 000X FFFEh | Input buffer threshold and control |
| 0010 | RATE-A GENERATOR | R/W | 0001 4E20h | Rate-A generator freq selection |
| 0014 | RATE-B GENERATOR | R/W | 0000 0018h | Rate-B generator freq selection |
| 0018 | BUFFER SIZE | RO | 0000 0000h | Number of values in the input buffer |
| 001C | (Reserved) | --- | --- | Inactive |
| 0020 | SCAN AND SYNC CONTROL | R/W | 0000 040Dh | Channels per scan; Clocking and Sync sources. |
| 0024 | (Reserved) | --- | --- | Inactive |
| 0028 | Board Configuration ** | RO | --- | Inactive |
| 002C | Autocal Values ** | R/W | --- | Inactive |
| 0030 | EXCITATION MASK 00-15 | R/W | --- | Channels 00-15 excitation control |
| 0034 | EXCITATION MASK 16-31 | R/W | --- | Channels 16-31 excitation control |
| 0038-3F | (Reserved) | --- | --- | Inactive |

***** R/W = Read/Write, RO = Read-Only.
****** Maintenance register. Shown for reference only.

## 3.2 Board Control Register (BCR)

As Table 3.2-1 indicates, the BCR consists of 16 control bits and status flags. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of Section 3.

**Table 3.2-1. Board Control Register (BCR)**

**Offset: 0000h** **Default: 0000 4060h**

| DATA BIT | MODE | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00 | R/W | AIM0 | 0 | Analog input mode. Selects input configuration or |
| D01 | R/W | AIM1 | 0 | selftest mode. Defaults to differential input mode. |
| D02 | R/W | AIM2 | 0 | . |
| D03 | R/W | (Reserved) | 0 | --- |
| D04 | R/W | RANGE0 | 0 | Analog input range. Defaults to ±10V range. |
| D05 | R/W | RANGE1 | 1 | |
| D06 | R/W | OFFSET BINARY | 1 | Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW. |
| D07 | R/W | ENABLE EXTERNAL SYNC | 0 | Configures the board for external sync I/O when HIGH. (SYNC I/O pins are reassigned as a TTLI/O pair). |
| D08 | R/W | EXCITATION TEST | 0 | Turns the excitation current ON when HIGH, regardless of the scanning state or the values in the channel mask registers. Used primarily for calibrating the current source. |
| D09-11 | R/W | (Reserved) | 0 | --- |
| D12 | R/W | *INPUT SYNC | 0 | Triggers a single sample of active channels when BCR Input Sync is selected in the Scan and Sync Control Register. Clears automatically upon scan completion, |
| D13 | R/W | *AUTOCAL | 0 | Initiates an autocalibration operation when set HIGH. Clears automatically upon autocal completion, |
| D14 | RO | AUTOCAL PASS | 1 | Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration. |
| D15 | R/W | *INITIALIZE | 0 | Initializes the board when set HIGH. Sets defaults for all registers. |
| D16-D31 | RO | (Reserved) | 0 | Inactive |

## 3.3 Configuration and Initialization

### 3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted as described in Section 3.7.

**Table 3.3-1. Configuration Operations**

| Operation | Maximum Duration |
|---|---|
| PCI configuration registers are loaded from internal ROM | 3 ms |
| Internal control logic is configured from internal ROM | 300 ms |
| Internal control logic is initialized | 3 ms |

Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI bus reset, and should be required only once after the initial application of power. PCI register configuration terminates with the PCI interrupts disabled (Section 3.7).

### 3.3.2 Initialization

Internal control logic is initialized without invoking configuration, by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked.
- Calibration D/A converters are initialized to midrange.
- Analog input voltage range is ±10 Volts.
- Analog inputs are configured as 32 differential channels.
- Current excitation is enabled for all 32 input channels.
- Cascaded Rate-A/B generators provide scan clocking at 50 scans per second.
- Input scanning is disabled by the Rate-A generator DISABLE control bit
- Analog input data coding format is offset binary.
- The analog input buffer is reset to empty.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

## 3.4 Analog Input Parameters

### 3.4.1 Input Voltage Range

BCR control field RANGE[], as shown in Table 3.4-1 selects the analog input voltage range.

**Table 3.4-1. Analog Voltage Range Selection**

| RANGE[1:0] | ANALOG INPUT RANGE |
|---|---|
| 0 | ±2.5 Volts |
| 1 | ±5 Volts |
| 2 | ±10 Volts |
| 3 | ±10 Volts |

### 3.4.2 Timing Organization

Figure 3.4-1 illustrates the manner in which timing signals are organized within the board. The input scan clock multiplexer is controlled by the Scan and Sync control register, which provides direct software control of clocking and sync operations. The external sync input and output lines permit external control of timing. Two rate generators operate directly from the master clock, which has a frequency of 24 MHz on the PMC-16AICS32 board.

Each Input Scan Clock initiates a complete scan of all active input channels. An input scan can contain from two to 64 channels, or any single channel can be digitized at the maximum conversion rate. Each multiple-channel scan commences with Channel 00, and proceeds upward through consecutive channels until the selected number of channels has been digitized.

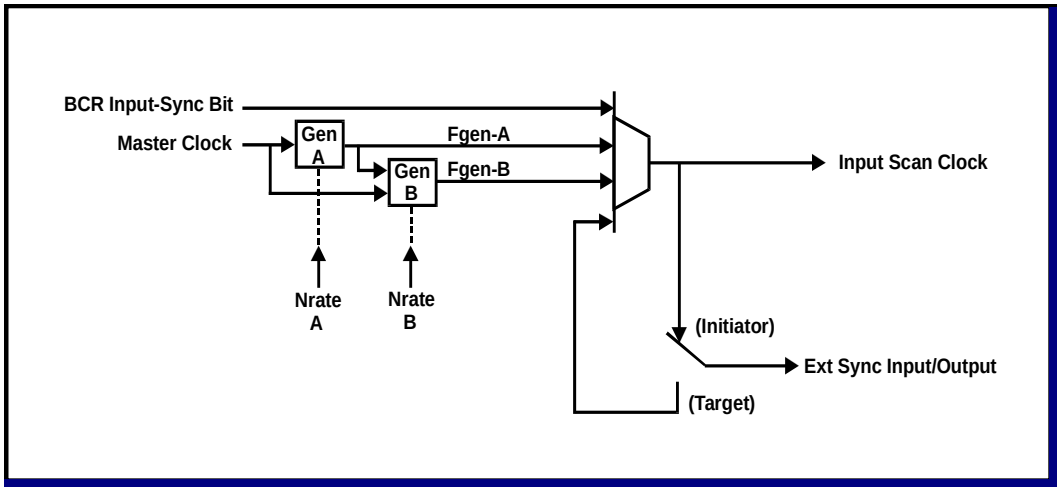


**Figure 3.4-1. Clock and Sync Organization**

### 3.4.3 Scan and Sync Control Register

The Scan and Sync control register (Table 3.4-2) controls the configuration of internal timing signals. Bits D00-02 select the number of channels in an input scan size from two channels to 64 channels, or select the single-channel mode if zero. (See Paragraph 3.5.5; Scanning Modes).

### 3.4.4 Scan-Rate Generators

Each of the two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate register. The two rate generator control registers are organized as shown in Table 3.4-3. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. To prevent the input buffer from filling with extraneous data at power-up, D16 defaults to the HIGH state in the Rate-A control register.

**Table 3.4-2. Scan and Sync Control Register**

**Offset: 0020h** **Default: 0000 040Dh**

| DATA BIT | MODE | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00-D02 | R/W | SCAN SIZE | 5 | Number of input channels per scan:<br>0 => Single-Channel mode *<br>1 => 2 channels per scan<br>2 => 4 channels per scan<br>3 => 8 channels per scan<br>4 => 16 channels per scan<br>**5 => 32 channels per scan (Default)**<br>6 => 64 channels per scan (S.E. mode only)<br>7 =>(Reserved)<br>* Channel selected by Single-Channel Select field below. |
| D03-D04 | R/W | ANALOG INPUTS SCAN CLOCK | 1 | Selects the analog input scan clocking source:<br>0 => Internal Rate-A generator output<br>**1 => Internal Rate-B generator output (Default)**<br>2 => External Sync input line<br>3 => BCR Input Sync control bit. |
| D05-D09 | R/W | (Reserved) | 0 | --- |
| D10 | R/W | RATE-B CLOCK SOURCE | 1 | Selects the clock input source for the Rate-B generator:<br>0 => Master clock<br>**1 => Rate-A generator output (Default)** |
| D11 | R/W | (Reserved) | 0 | --- |
| D12-17 | R/W | SINGLE-CHANNEL SELECT | 0 | Selects the input channel number when operating in the Single-Channel scanning mode. |
| D18 | R/W | (Reserved) | 0 | --- |
| D19-D31 | RO | (Reserved) | 0 | Inactive |

3.4.4.1 Scan Rate Control

Each rate generator contains a divisor that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of 24 MHz, the output frequency **Fgen** of each generator is determined as:

**Fgen (Hz) = 24,000,000 / Nrate,**

where **Nrate** is the decimal equivalent of D0-D15 in the rate generator register. **Fgen** is the scanning trigger frequency, and establishes the rate at which complete scans are initiated. The maximum permissible scanning frequency **Fgen-max** equals the maximum conversion rate **Fconv-max**, divided by the number of channels in a scan:

**Fgen-max = Fconv-max / Nchan,**

where **Fconv-max** is 100 kHz. Values for **Fgen** higher than **Fgen-max** will produce unpredictable results and are not recommended. Table 3.4-5 provides examples of various scan rates and scan sizes.

**Table 3.4-3. Scan-Rate Generator Register**

**Offset: 0010h (Rate-A), 0014h (Rate-B)** **Default: 0001 4E20 (Rate-A), 0000 0018h (Rate-B)**

| DATA BIT | MODE* | DESIGNATION | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| D00-D15 | R/W | NRATE | --- | Rate generator frequency control |
| D16 | R/W | GENERATOR DISABLE | 1 | Disables the rate generator when HIGH |
| D17-D31 | RO | (Inactive) | 0 | --- |

**Table 3.4-4. Scan-Rate Generator Frequency Selection**

| Nrate ( RATE[15..0] ) | | FREQUENCY Fgen * |
|---|---|---|
| (Dec) | (Hex) | (Hz) |
| 240 | 00F0 | 100,000 |
| 241 | 00F1 | 99,585 |
| --- | --- | Fgen (Hz) = 24,000,000 / Nrate |
| 65534 | FFFE | 366.222 |
| 65535 | FFFF | 366.217 |

* ±0.015 percent.

**Table 3.4-5. Scan-Rate Examples**

| Channels Per Scan (Nchan) | Maximum Scan Rate (Fgen-max, Hz) | Required Scan Rate (Fgen, Hz) | Rate Generator Register (Nrate, Dec) |
|---|---|---|---|
| 64 | 1,562 | 1,000 | 24,000 |
| 64 | 1,562 | 500 | 48,000 |
| 32 | 3,125 | 3,000 | 8,000 |
| 32 | 3,125 | 500 | 48,000 |
| 8 | 12,500 | 10,000 | 2,400 |
| 2 | 50,000 | 20,000 | 1,200 |
| 1 * | 100,000 | 100,000 | 240 |
| 1 * | 100,000 | 20,000 | 1,200 |

* Single-scan mode.

### 3.4.4.2 Generator Cascading

To provide very low scanning rates, the Rate-B generator can be configured to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

**Fgen-B (Hz) = 24,000,000 / (Nrate-A * Nrate-B ) ,**

which can produce scan triggering rates as low as 0.0056 Hz. This is the default rate generator configuration.

### 3.4.5 Multiboard Synchronization

Multiple boards can be externally interconnected to produce analog input scans simultaneously. Figure 2.3-2 illustrates the interconnections required. External sync I/O is enabled by setting the ENABLE EXTERNAL SYNC control bit HIGH in the BCR. One of the boards is designated as the *Initiator*, and the remaining boards are designated as *targets*.

A board that is enabled for external sync I/O is designated as a *target* by selecting the External Sync Input Line with the ANALOG INPUTS SCAN CLOCK field in the Scan and Sync control register. Any other value for the ANALOG INPUTS SCAN CLOCK field designates the board as an *initiator*, and routes the internal scan clock to the I/O connector. The sync signal can originate either on the initiator board itself, or externally as an input to a group of targets.

The initiator generates a sync pulse at the beginning of each scan, and each of the target boards responds to the sync pulse by initiating a single input scan. The initiator and target boards can be operating with various scan sizes, but the duration, or period, of the initiator scan must equal or exceed those of the targets in order to avoid "dropping" target scans. That is, the scan rate selected for the target boards should be slightly higher than that of the initiator board.

NOTE: Enabling external sync I/O reassigns the function of the SYNC pins in the I/O connector as a bidirectional TTL port. Voltages applied externally in this configuration must not extend outside the range of -0.5V to +7V.

## 3.5 Analog Input Control

### 3.5.1 Input Data Organization

Conversion data from the analog-to-digital converter (ADC) flows through a transfer register into the analog input data buffer, and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

#### 3.5.1.1 Input Data Buffer

Analog input data is read from the Analog Input Data Buffer in longword-serial format, as shown in Table 3.5-1. Each value is right-justified to the LSB, and occupies bit positions D00 through D15. D16-D31 are always returned as zeros. The capacity of the input data buffer is 64K-samples.

**Table 3.5-1. Input Data Buffer**

**Offset: 0008h** **Default: N/A**

| DATA BIT | MODE* | DESIGNATION | DESCRIPTION |
|---|---|---|---|
| D00 | RO | DATA00 | Least significant data bit |
| D01-D14 | RO | DATA01 - DATA14 | Intermediate data bits |
| D15 | RO | DATA15 | Most significant data bit |
| D16-D31 | RO | (Inactive) | --- |

* RO indicates read-only access. Write-data is ignored.

3.5.1.2 Data Coding Format

Analog input data is arranged as 16 active right-justified data bits with the coding conventions shown in Table 3.5-2. The default format is offset binary. Two's complement format is selected by clearing the Offset Binary control bit LOW in the BCR.

Note: Unless indicated otherwise, offset binary coding is assumed throughout this document.

**Table 3.5-2. Input Data Coding; 16-Bit Data**

| ANALOG INPUT LEVEL | DIGITAL VALUE (Hex) | |
|---|---|---|
| | OFFSET BINARY | TWO'S COMPLEMENT |
| Positive Full Scale minus 1 LSB | 0000 FFFF | 0000 7FFF |
| Zero plus 1 LSB | 0000 8001 | 0000 0001 |
| Zero | 0000 8000 | 0000 0000 |
| Zero minus 1 LSB | 0000 7FFF | 0000 FFFF |
| Negative Full Scale plus 1 LSB | 0000 0001 | 0000 8001 |
| Negative Full Scale | 0000 0000 | 0000 8000 |

3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-3 controls and monitors the flow of data through the analog input data buffer. Asserting the Clear Buffer control bit HIGH clears, or empties, the buffer, and aborts any input scan that might be in progress. The Threshold Flag is HIGH when the number of values in the input data buffer exceeds the input threshold value defined by bits D00-D15, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.7) can be programmed to occur on either the rising or falling edge of the threshold flag.

The Buffer Size register shown in Table 3.5-4 contains the number of input values present in the buffer, and is updated continuously.

**Table 3.5-3. Input Data Buffer Control Register**

**Offset: 000Ch** **Default: 0000 FFFEh**

| DATA BIT | MODE* | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00-15 | R/W | THRESHOLD VALUE | FFFEh | Input buffer threshold value. |
| D16 | R/W | CLEAR BUFFER * | 0 | Clears (empties) the input buffer when asserted HIGH. Aborts current input scan. |
| D17 | RO | THRESHOLD FLAG | 0 | Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE. |
| D18-D31 | RO | (Inactive) | 0 | --- |

*Clears automatically when operation is completed

**Table 3.5-4. Buffer Size Register**

**Offset: 0018h** **Default: 0000 0000h**

| DATA BIT | MODE* | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00-15 | RO | BUFFER SIZE | 0000h | Number of values in the input buffer |
| D16-D31 | RO | (Inactive) | 0 | --- |

### 3.5.3 Analog Input Function Modes

BCR control bits D00-D02 (AIM0-AIM2) control the analog input configuration, and provide selftest modes for monitoring the integrity of the analog input networks. Table 3.5-5 summarizes the input function modes.

NOTE: See Section 3.9 for information pertaining to input excitation current.

**Table 3.5-5. Analog Input Function Selection**

| AIM[2:0] | FUNCTION OR MODE |
|---|---|
| 0 | Differential analog input mode (Default mode). |
| 1 | Single-Ended analog input mode. |
| 2 | ZERO test. Internal ground reference is connected to all analog input channels. |
| 3 | +VREF test. Internal voltage reference is connected to all analog input channels. |
| 4-7 | (Reserved) |

#### 3.5.3.1 Differential Inputs

The analog inputs default to the differential configuration when power is applied or after initialization. In this mode, the 64 analog input lines are arranged as 32 differential pairs, with each HI/LO pair representing a single input channel.

#### 3.5.3.2 Single-Ended Inputs

With the single-ended input mode selected, each of the 64 analog input lines is measured in reference to a common *Input Return*, and represents an individual input channel.

#### 3.5.3.3 Selftest Modes

In the selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and for critical measurements the average value of multiple readings should be used.

The ZERO selftest measures a dead-zero reference signal and should produce a nominal midscale reading of 0000 8000h. For the +VREF test, a precision reference voltage equal to 94.780% of fullscale is applied as an analog input, and should produce a nominal reading of 0000 F951h.

### 3.5.4 Input Scan Timing

#### 3.5.4.1 Scan Sequence

For each analog input scan clock, all selected analog inputs are scanned once, with one conversion performed per channel. The number of channels included in each scan is controlled from two to 64 channels by the Scan Size control bit field in the Scan and Sync control register, or any single channel can be selected. Each multichannel scan commences with Channel 00 and proceeds upward through successive input channels until the selected number of channels has been digitized.

As each channel is selected in a scan, a dwell interval is inserted before the A/D conversion occurs. The dwell interval ensures maximum settling time for channels that are selected for excitation current (Section 3.9). The dwell is determined automatically to produce equal dwell intervals for all channels in a scan, regardless of the scan rate selected.

#### 3.5.4.2 Scan Clocking Source

The Scan and Sync control register (Table 3.4.2) provides multiple sources for analog input scan clocks. The clock can be provided by (a) either or both of the two rate generators on the board, (b) the External Sync hardware input line, or (c) the INPUT SYNC control bit in the BCR.

If the BCR input sync control bit is selected as the analog input clock source, an input scan occurs each time the INPUT SYNC control bit is set HIGH. The INPUT SYNC bit remains HIGH until the scan is completed, after which the bit clears automatically.

If the External Sync input line is the analog input clock source, each HIGH-to-LOW transition of the input line initiates an input scan.

### 3.5.5 Scanning Modes

The analog inputs can be scanned in groups of 2, 4, 8, 16, 32 or 64 channels (32 maximum for differential inputs), or any single channel can be selected for digitizing. The number of channels in a scan is selected by the SCAN SIZE[] field in the scan and sync control register. An input scan commences with Channel-00, and proceeds upward through successive channels until the selected number of channels has been digitized and stored in the input data buffer.

For Single-Channel sampling (SCAN SIZE[] = 0), the channel to be digitized is selected by the SINGLE-CHANNEL SELECT control field.

## 3.6 Autocalibration

To obtain maximum accuracy, autocalibration should be performed after: (a) power warmup, (b) each initialization, and (c) after a change in voltage range selection. Autocalibration uses current settings for the analog input voltage range, and ignores other control parameters such as input configuration, clocking rates, etc. No control settings are altered during autocalibration, and external analog input signals are ignored.

Autocalibration is invoked by setting the Autocal control bit HIGH in the BCR. The control bit returns LOW (normal operation) automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of approximately 2-4 seconds. Completion of the operation can be detected either by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.7) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in calibration DAC's. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR will be cleared LOW at the end of the autocalibration interval, and will remain LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

NOTE: Autocalibration does not adjust the excitation source, which must be calibrated manually.

## 3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.7.1)
b. The *PCI interrupt* must be enabled (Section3.7.2).

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.7.2.

### 3.7.1 Local Interrupt Request

The Interrupt Control Register shown in Table 3.7-1 controls the single local interrupt request line. Two simultaneous source conditions (IRQ 0 and1) are available for the request, with multiple conditions available for each source. IRQ 0 and 1 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for either of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while the condition is selected.

**Table 3.7-1. Interrupt Control Register**

**Offset: 0000 0004h** **Default: 0000 0008h**

| DATA BIT | MODE | DESIGNATION | DEF | VALUE | INTERRUPT CONDITION |
|---|---|---|---|---|---|
| D00-02 | R/W | IRQ0 A0,1,2 | 0 | 0 | Idle. Interrupt disabled unless initializing. Default state after reset. |
| | | | | 1 | Autocalibration operation completed |
| | | | | 2 | Input scan initiated (Sync) |
| | | | | 3 | Input scan completed |
| | | | | 4-7 | (Reserved) |
| D03 | R/W | IRQ0 REQUEST | 1* | --- | Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus. |
| D04-06 | R/W | IRQ1 A0,1 | 0 | 0 | Idle; no interrupt condition selected. |
| | | | | 1 | Input buffer threshold LOW-HIGH transition |
| | | | | 2 | Input buffer threshold HIGH-LOW transition |
| | | | | 3-7 | (Reserved) |
| D07 | R/W | IRQ1 REQUEST | 0 | --- | Group 1 interrupt request flag. See D03. |
| D08-31 | RO | (Inactive) | 0 | --- | |

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

### 3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX$^{TM}$ PCI-9080 reference manual..

## 3.8 DMA Operation

DMA transfers from the analog input buffer are supported in block-mode with the board operating as bus master. Table 3.8-1 illustrates a typical PCI register configuration that would control a non-chaining, non-incrementing DMA transfer, and in which a PCI interrupt is generated when the transfer has been completed. Bit 02 in the PCI Command register (04h) must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 data manual for a detailed description of these registers.

**Table 3.8-1. Typical DMA Register Configuration**

| PCI Offset | PCI Register | Function | Typical Value |
|---|---|---|---|
| 80h | DMA Mode | Bus width (32); Interrupt on done | 0002 0D43h |
| 84h | DMA PCI Address | Initial PCI data source address | * |
| 88h | DMA Local Address | Initial Analog Input Buffer local address (Analog input buffer) | 0000 0008h |
| 8Ch | DMA Transfer Byte Count | Number of bytes in transfer | * |
| 90h | DMA Descriptor Counter | Transfer direction; Local bus to PCI bus (Analog inputs) | 0000 000Ah |
| A8h | DMA Command Status | Command and Status Register | 0000 0001h<br>0000 0003h<br>(See Text) |

* Determined by specific transfer requirements.

For most applications, the DMA Command Status Register (A8h) should be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

## 3.9 Input Excitation Current

Transducer excitation current can be applied through the HI input line of any channel from 00 through 31. The voltage developed in an input channel is positive and equals the excitation current times the *total resistance between the pins*, including the resistance of the input and return lines as well as the resistance of the transducer itself.

### 3.9.1 Current Source Control

#### 3.9.1.1 Channel Excitation Masks

The excitation current for each input channel is controlled by a control bit in one of the two Channel Excitation Mask registers shown in Table 3.9-1. If the control bit for a channel is HIGH, the channel receives excitation current during the interval in which the channel is sampled in each scan sequence.

If the control bit is LOW, excitation is not applied and the channel can be used as a basic voltage input channel. Single-ended channels not assigned an excitation control bit have no excitation applied, and can also be used as basic voltage input channels.

**Table 3.9-1. Channel Excitation Mask Registers**

**Excitation Mask 00-15:**
Offset: 0000 0030h
Default: 0000 FFFFh

| REG BIT | EXCITATION APPLIED TO: DIFF CHAN | EXCITATION APPLIED TO: S.E. CHAN |
|---|---|---|
| D00 | 00 | 00 |
| D01 | 01 | 02 |
| D02 | 02 | 04 |
| D03 | 03 | 06 |
| D04 | 04 | 08 |
| D05 | 05 | 10 |
| D06 | 06 | 12 |
| D07 | 07 | 14 |
| D08 | 08 | 16 |
| D09 | 09 | 18 |
| D10 | 10 | 20 |
| D11 | 11 | 22 |
| D12 | 12 | 24 |
| D13 | 13 | 26 |
| D14 | 14 | 28 |
| D15 | 15 | 30 |
| D16-D31 | (Inactive) | (Inactive) |

**Excitation Mask 16-31:**
Offset: 0000 0034h
Default: 0000 FFFFh

| REG BIT | EXCITATION APPLIED TO: DIFF CHAN | EXCITATION APPLIED TO: S.E. CHAN |
|---|---|---|
| D00 | 16 | 32 |
| D01 | 17 | 34 |
| D02 | 18 | 36 |
| D03 | 19 | 38 |
| D04 | 20 | 40 |
| D05 | 21 | 42 |
| D06 | 22 | 44 |
| D07 | 23 | 46 |
| D08 | 24 | 48 |
| D09 | 25 | 50 |
| D10 | 26 | 52 |
| D11 | 27 | 54 |
| D12 | 28 | 56 |
| D13 | 29 | 58 |
| D14 | 30 | 60 |
| D15 | 31 | 62 |
| D16-D31 | (Inactive) | (Inactive) |

| COMMENTS |
|---|
| Channels with assigned register bits HIGH have excitation current applied during. input scanning<br><br>Channels with assigned bits LOW (or with no assigned control bits in the case of odd-numbered single-ended inputs) have no excitation applied, and can be used as voltage inputs. |
| --- |

(All active bits R/W)

3.9.1.2 Excitation Test Mode

If the EXCITATION TEST control bit is set HIGH in the BCR, the excitation source is turned on for all channels and the excitation masks are ignored. This excitation mode can be used in the single-channel scan mode to apply sustained excitation current to any single input channel from Channel 00 through Channel 31.

3.9.2 Scan Timing

Each scan is divided into **Nchan** equal channel intervals, where **Nchan** equals the number of channels in the scan. Each channel interval consists of a dwell interval followed by a conversion interval. The length of the dwell interval should be selected to allow the excitation current to charge the input line capacitance to the final transducer voltage before the conversion occurs. The conversion interval is fixed at approximately 3 microseconds.

In the default state after a reset, the rate generators are cascaded (3.4.4.2), and the Rate-B control register is initialized to the value 24 (18h). This value for Rate-B conveniently scales the Rate-A register to equal the scan interval in microseconds. For example, the default value of 20,000 (4E20h) for the Rate-A register produces a scan interval of 20,000 microseconds, or 20 milliseconds, which is equivalent to the default scan rate of 50 scans per second. (For intervals greater than 65.535 milliseconds, the Rate-B register requires a value larger than 20).

In general, the scan rate **Fscan** is determined from the Rate-A and Rate-B register values **Nrate-A** and **Nrate-B** as:

**Fscan (Hz) = 24,000,000 / (Nrate-A * Nrate-B ) ,**

while the scan interval **Tscan** is the reciprocal of the scan rate, or:

**Tscan (Seconds) = (Nrate-A * Nrate-B ) / 24,000,000.**

Each scan provides a uniform interval **Tchan** for each channel, where:

**Tchan = Tscan / Nchan,**

and **Nchan** equals the number of channels in a scan. **Tscan** is the sum of the dwell and conversion intervals, and has a minimum value of 10 microseconds, making the minimum value for Tscan:

**Tscan-min = Nscan * 10 microseconds.**

### 3.10 Board Configuration Register

The read-only board configuration register (Table 3.10.1) contains the existing firmware revision, and a status field that indicates the availability of optional features.

**Table 3.10.1. Board Configuration Register**

**Offset: 0000 0028h** **Default: 000X XXXXh**

| BIT FIELD | DESCRIPTION |
|---|---|
| D00-D11 | Firmware Revision |
| D12-D15 | (Reserved status flags). |
| D16-18 | Excitation Current:<br>0 => 1.0 ma<br>1 => 2.0 ma<br>2 => 3.0 ma<br>3 => 5.0 ma<br>4 => 0.4 ma<br>5 => 10.0 ma<br>6-7 => (Reserved) |
| D19-D31 | (Reserved) |

# SECTION 4.0

# PRINCIPLES OF OPERATION

## 4.1 General Description

The PMC-16AICS32 board contains a 64-channel analog multiplexer and a 16-bit A/D converter for digitizing up to 64 single-ended or 32 differential analog input channels. A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller (Figure 4.1-1). Gain and offset corrections of the analog input channels are performed by calibration DAC's that are loaded with channel correction values during autocalibration

The analog inputs are software-configurable either as 64 single-ended channels, or as 32 differential signal pairs, and a scanning excitation current source provides excitation for resistance transducers such as RTD's. A selftest switching network routes a precision reference to the A/D converter during autocalibration. Analog input data accumulates in a 64K-sample buffer until retrieved by the PCI bus.

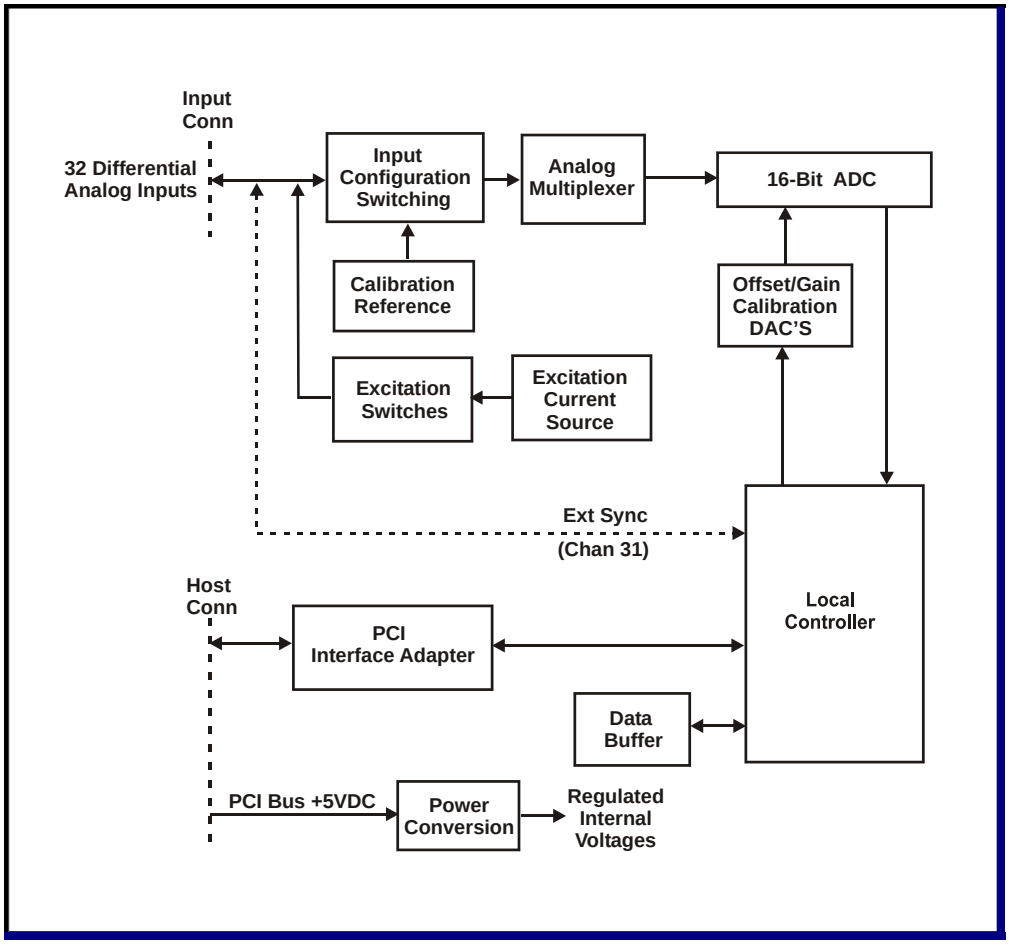


**Figure 4.1-1. Functional Block Diagram**

Analog input scanning on multiple PMC-16AICS32 target boards can be synchronized to the analog scanning sequence on a single software-designated initiator board.

An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer. The analog input voltage range for all channels is software-selectable as ±2.5V, ±5V or ±10V.

## 4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches and analog multiplexer shown in Figure 4.1-1. During normal operation, analog input channels from the input/output connector are scanned and digitized. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC. The analog multiplexer establishes the input configuration as either single-ended or differential, in response to software control.

An excitation current source can be software-assigned to any of 32 input channels, and is injected into the HI input line as each channel is selected in the multiplexer sequence.

The selected input signals are selected by an analog multiplexer for digitizing by the 16-bit ADC. By routing all inputs through the same signal path, the errors introduced by all components in that path are accounted for during autocalibration.

The output of the multiplexer is buffered by a differential amplifier and finally is converted by the ADC into a 16-bit digital code. Data is extracted from the ADC in parallel format, and passes through a transfer register into the main analog input data buffer. Offset and gain trimming of the ADC is provided by a pair of 10-bit DAC's that are loaded with trim values determined during autocalibration.

Analog channels from the input/output connector are scanned in a pipeline sequence, in which the subsequent channel in the scanning sequence is selected and allowed to settle, while the current sample is being digitized. This approach increases the effective scan rate without requiring shorter settling or conversion times. The input scan rate can be controlled from: (a) either of two internal rate generators, (b) software, through a control register, or (c) an external hardware sync source.

## 4.3 Rate Generators

The local controller contains two independent rate generators, each of which divides a master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a clocking source for the analog inputs, and the generators can be cascaded to produce very long clocking intervals.

### 4.4 Data Buffer

A 64 K-sample analog input data buffer and the PCIbus share a common memory element that is arbitrated to produce effectively independent read/write buffer functions. To avoid the data loss that might occur otherwise during arbitration cycles, data to the input buffer passes through a transfer register that ensures an uninterrupted flow of data in the critical input data paths. Buffer control is supported by an adjustable threshold, and by a threshold flag that can be programmed to generate an interrupt request.

### 4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the control software, and has an approximate duration of 2-4 seconds.

An internal voltage reference is used to calibrate the span of each channel, and a dead-zero ground reference is used to calibrate the offset value. Each of the two 10-bit calibration DAC's is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit initially is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response from the channel, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 10 bits have been tested and adjusted. The final value in the calibration DAC remains in the DAC until the autocalibration sequence is repeated, or until power is removed.

### 4.6 Power Control

Regulated supply voltages of ±5 Volts and ±15 Volts are required by the analog networks, and are derived from the +5-Volt input provided by the PCI bus. A DC/DC converter produces preregulated voltages that are subsequently series-regulated to the required output levels. Series regulation ensures minimum noise and optimum performance of the power supply outputs.

# APPENDIX A

# LOCAL REGISTER QUICK REFERENCE

# APPENDIX A
# LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

**Table 3.1-1. Control and Data Registers**

| OFFSET (Hex) | REGISTER | ACCESS MODE * | DEFAULT | PRIMARY FUNCTION |
|---|---|---|---|---|
| 0000 | BOARD CONTROL (BCR) | R/W | 0000 4060h | Board Control Register (BCR) |
| 0004 | INTERRUPT CONTROL | R/W | 0000 0008h | Interrupt conditions and flags |
| 0008 | INPUT DATA BUFFER | RO | --- | Analog input data buffer |
| 000C | INPUT BUFFER CONTROL | R/W | 000X FFFEh | Input buffer threshold and control |
| 0010 | RATE-A GENERATOR | R/W | 0001 4E20h | Rate-A generator freq selection |
| 0014 | RATE-B GENERATOR | R/W | 0000 0018h | Rate-B generator freq selection |
| 0018 | BUFFER SIZE | RO | 0000 0000h | Number of values in the input buffer |
| 001C | (Reserved) | --- | --- | Inactive |
| 0020 | SCAN AND SYNC CONTROL | R/W | 0000 040Dh | Channels per scan; Clocking and Sync sources. |
| 0024 | (Reserved) | --- | --- | Inactive |
| 0028 | Board Configuration ** | RO | --- | Inactive |
| 002C | Autocal Values ** | R/W | --- | Inactive |
| 0030 | EXCITATION MASK 00-15 | R/W | --- | Channels 00-15 excitation control |
| 0034 | EXCITATION MASK 16-31 | R/W | --- | Channels 16-31 excitation control |
| 0038-3F | (Reserved) | --- | --- | Inactive |

***** R/W = Read/Write, RO = Read-Only.
****** Maintenance register. Shown for reference only.

**Table 3.2-1. Board Control Register (BCR)**

**Offset: 0000h** **Default: 0000 4060h**

| DATA BIT | MODE | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00 | R/W | AIM0 | 0 | Analog input mode. Selects input configuration or |
| D01 | R/W | AIM1 | 0 | selftest mode. Defaults to differential input mode. |
| D02 | R/W | AIM2 | 0 | . |
| D03 | R/W | (Reserved) | 0 | --- |
| D04 | R/W | RANGE0 | 0 | Analog input range. Defaults to ±10V range. |
| D05 | R/W | RANGE1 | 1 | |
| D06 | R/W | OFFSET BINARY | 1 | Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW. |
| D07 | R/W | ENABLE EXTERNAL SYNC | 0 | Configures the board for external sync I/O when HIGH. (SYNC I/O pins are reassigned as a TTLI/O pair). |
| D08 | R/W | EXCITATION TEST | 0 | Turns the excitation current ON when HIGH, regardless of the scanning state or the values in the channel mask registers. Used primarily for calibrating the current source. |
| D09-11 | R/W | (Reserved) | 0 | --- |
| D12 | R/W | *INPUT SYNC | 0 | Triggers a single sample of active channels when BCR Input Sync is selected in the Scan and Sync Control Register. Clears automatically upon scan completion, |
| D13 | R/W | *AUTOCAL | 0 | Initiates an autocalibration operation when set HIGH. Clears automatically upon autocal completion, |
| D14 | RO | AUTOCAL PASS | 1 | Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration. |
| D15 | R/W | *INITIALIZE | 0 | Initializes the board when set HIGH. Sets defaults for all registers. |
| D16-D31 | RO | (Reserved) | 0 | Inactive |

**Table 3.4-1. Analog Voltage Range Selection (BCR field)**

| RANGE[1:0] | ANALOG INPUT RANGE |
|---|---|
| 0 | ±2.5 Volts |
| 1 | ±5 Volts |
| 2 | ±10 Volts |
| 3 | ±10 Volts |

**Table 3.4-2. Scan and Sync Control Register**

**Offset: 0020h** **Default: 0000 040Dh**

| DATA BIT | MODE | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00-D02 | R/W | SCAN SIZE | 5 | Number of input channels per scan:<br>0 => Single-Channel mode *<br>1 => 2 channels per scan<br>2 => 4 channels per scan<br>3 => 8 channels per scan<br>4 => 16 channels per scan<br>**5 => 32 channels per scan (Default)**<br>6 => 64 channels per scan (S.E. mode only)<br>7 =>(Reserved)<br>* Channel selected by Single-Channel Select field below. |
| D03-D04 | R/W | ANALOG INPUTS SCAN CLOCK | 1 | Selects the analog input scan clocking source:<br>0 => Internal Rate-A generator output<br>**1 => Internal Rate-B generator output (Default)**<br>2 => External Sync input line<br>3 => BCR Input Sync control bit. |
| D05-D09 | R/W | (Reserved) | 0 | --- |
| D10 | R/W | RATE-B CLOCK SOURCE | 1 | Selects the clock input source for the Rate-B generator:<br>0 => Master clock<br>**1 => Rate-A generator output (Default)** |
| D11 | R/W | (Reserved) | 0 | --- |
| D12-17 | R/W | SINGLE-CHANNEL SELECT | 0 | Selects the input channel number when operating in the Single-Channel scanning mode. |
| D18 | R/W | (Reserved) | 0 | --- |
| D19-D31 | RO | (Reserved) | 0 | Inactive |

**Table 3.4-3. Scan-Rate Generator Register**

**Offset: 0010h (Rate-A), 14 (Rate-B)** **Default: 0001 4E20 (Rate-A), 0000 0018h (Rate-B)**

| DATA BIT | MODE* | DESIGNATION | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| D00-D15 | R/W | NRATE | --- | Rate generator frequency control |
| D16 | R/W | GENERATOR DISABLE | 1 | Disables the rate generator when HIGH |
| D17-D31 | RO | (Inactive) | 0 | --- |

R/W = Read/Write, RO = Read-Only.

**Table 3.4-4. Scan-Rate Generator Frequency Selection**

| Nrate ( RATE[15..0] ) | | FREQUENCY Fgen * |
|---|---|---|
| (Dec) | (Hex) | (Hz) |
| 240 | 00F0 | 100,000 |
| 241 | 00F1 | 99,585 |
| --- | --- | Fgen (Hz) = 24,000,000 / Nrate |
| 65534 | FFFE | 366.222 |
| 65535 | FFFF | 366.217 |

**Table 3.4-5. Scan-Rate Examples**

| Channels Per Scan (Nchan) | Maximum Scan Rate (Fgen-max, Hz) | Required Scan Rate (Fgen, Hz) | Rate Generator Register (Nrate, Dec) |
|---|---|---|---|
| 64 | 1,562 | 1,000 | 24,000 |
| 64 | 1,562 | 500 | 48,000 |
| 32 | 3,125 | 3,000 | 8,000 |
| 32 | 3,125 | 500 | 48,000 |
| 8 | 12,500 | 10,000 | 2,400 |
| 2 | 50,000 | 20,000 | 1,200 |
| 1 * | 100,000 | 100,000 | 240 |
| 1 * | 100,000 | 20,000 | 1,200 |

* Single-scan mode.

**Table 3.5-1. Input Data Buffer**

**Offset: 0008h** **Default: N/A**

| DATA BIT | MODE* | DESIGNATION | DESCRIPTION |
|---|---|---|---|
| D00 | RO | DATA00 | Least significant data bit |
| D01-D14 | RO | DATA01 - DATA14 | Intermediate data bits |
| D15 | RO | DATA15 | Most significant data bit |
| D16-D31 | RO | (Inactive) | --- |

* RO indicates read-only access. Write-data is ignored.

**Table 3.5-2. Input Data Coding; 16-Bit Data**

| ANALOG LEVEL | DIGITAL VALUE (Hex) | |
|---|---|---|
| | OFFSET BINARY | TWO'S COMPLEMENT |
| Positive Full Scale minus 1 LSB | 0000 FFFF | 0000 7FFF |
| Zero plus 1 LSB | 0000 8001 | 0000 0001 |
| Zero | 0000 8000 | 0000 0000 |
| Zero minus 1 LSB | 0000 7FFF | 0000 FFFF |
| Negative Full Scale plus 1 LSB | 0000 0001 | 0000 8001 |
| Negative Full Scale | 0000 0000 | 0000 8000 |

**Table 3.5-3. Input Data Buffer Control Register**

**Offset: 000Ch** **Default: 0000 FFFEh**

| DATA BIT | MODE* | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00-15 | R/W | THRESHOLD VALUE | FFFEh | Input buffer threshold value. |
| D16 | R/W | CLEAR BUFFER * | 0 | Clears (empties) the input buffer when asserted HIGH. Aborts current input scan. |
| D17 | RO | THRESHOLD FLAG | 0 | Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE. |
| D18-D31 | RO | (Inactive) | 0 | --- |

*Clears automatically when operation is completed

**Table 3.5-4. Buffer Size Register**

**Offset: 0018h** **Default: 0000 0000h**

| DATA BIT | MODE* | DESIGNATION | DEF | DESCRIPTION |
|---|---|---|---|---|
| D00-15 | RO | BUFFER SIZE | 0000h | Number of values in the input buffer |
| D16-D31 | RO | (Inactive) | 0 | --- |

**Table 3.5-5. Analog Input Function Selection (BCR field)**

| AIM[2:0] | FUNCTION OR MODE |
|---|---|
| 0 | Differential analog input mode (Default mode). |
| 1 | Single-Ended analog input mode. |
| 2 | ZERO test. Internal ground reference is connected to all analog input channels. |
| 3 | +VREF test. Internal voltage reference is connected to all analog input channels. |
| 4-7 | (Reserved) |

**Table 3.7-1. Interrupt Control Register**

**Offset: 0000 0004h** **Default: 0000 0008h**

| DATA BIT | MODE | DESIGNATION | DEF | VALUE | INTERRUPT CONDITION |
|---|---|---|---|---|---|
| D00-02 | R/W | IRQ0 A0,1,2 | 0 | 0 | Idle. Interrupt disabled unless initializing. Default state after reset. |
| | | | | 1 | Autocalibration operation completed |
| | | | | 2 | Input scan initiated (Sync) |
| | | | | 3 | Input scan completed |
| | | | | 4-7 | (Reserved) |
| D03 | R/W | IRQ0 REQUEST | 1* | --- | Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus. |
| D04-06 | R/W | IRQ1 A0,1 | 0 | 0 | Idle; no interrupt condition selected. |
| | | | | 1 | Input buffer threshold LOW-HIGH transition |
| | | | | 2 | Input buffer threshold HIGH-LOW transition |
| | | | | 3-7 | (Reserved) |
| D07 | R/W | IRQ1 REQUEST | 0 | --- | Group 1 interrupt request flag. See D03. |
| D08-31 | RO | (Inactive) | 0 | --- | |

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

**Table 3.8-1. Typical DMA Register Configuration**

| PCI Offset | PCI Register | Function | Typical Value |
|---|---|---|---|
| 80h | DMA Mode | Bus width (32); Interrupt on done | 0002 0D43h |
| 84h | DMA PCI Address | Initial PCI data source address | * |
| 88h | DMA Local Address | Initial Analog Input Buffer local address (Analog input buffer) | 0000 0008h |
| 8Ch | DMA Transfer Byte Count | Number of bytes in transfer | * |
| 90h | DMA Descriptor Counter | Transfer direction; Local bus to PCI bus (Analog inputs) | 0000 000Ah |
| A8h | DMA Command Status | Command and Status Register | 0000 0001h<br>0000 0003h<br>(See Text) |

* Determined by specific transfer requirements.

**Table 3.9-1. Channel Excitation Mask Registers**

**Excitation Mask 00-15:** Offset: 0000 0030h Default: 0000 FFFFh

**Excitation Mask 16-31:** Offset: 0000 0034h Default: 0000 FFFFh

| | EXCITATION APPLIED TO: | | | EXCITATION APPLIED TO: | | |
|---|---|---|---|---|---|---|
| REG BIT | DIFF CHAN | S.E. CHAN | REG BIT | DIFF CHAN | S.E. CHAN | COMMENTS |
| D00 | 00 | 00 | D00 | 16 | 32 | Channels with assigned register bits HIGH have excitation current applied during. input scanning<br><br>Channels with assigned bits LOW (or with no assigned control bits in the case of odd-numbered single-ended inputs) have no excitation applied, and can be used as voltage inputs. |
| D01 | 01 | 02 | D01 | 17 | 34 | |
| D02 | 02 | 04 | D02 | 18 | 36 | |
| D03 | 03 | 06 | D03 | 19 | 38 | |
| D04 | 04 | 08 | D04 | 20 | 40 | |
| D05 | 05 | 10 | D05 | 21 | 42 | |
| D06 | 06 | 12 | D06 | 22 | 44 | |
| D07 | 07 | 14 | D07 | 23 | 46 | |
| D08 | 08 | 16 | D08 | 24 | 48 | |
| D09 | 09 | 18 | D09 | 25 | 50 | |
| D10 | 10 | 20 | D10 | 26 | 52 | |
| D11 | 11 | 22 | D11 | 27 | 54 | |
| D12 | 12 | 24 | D12 | 28 | 56 | |
| D13 | 13 | 26 | D13 | 29 | 58 | |
| D14 | 14 | 28 | D14 | 30 | 60 | |
| D15 | 15 | 30 | D15 | 31 | 62 | |
| D16-D31 | (Inactive) | (Inactive) | D16-D31 | (Inactive) | (Inactive) | --- |

(All active bits R/W)

**Table 3.10.1. Board Configuration Register**

**Offset: 0000 0028h** **Default: 000X XXXXh**

| BIT FIELD | DESCRIPTION |
|---|---|
| D00-D11 | Firmware Revision |
| D12-D15 | (Reserved status flags). |
| D16-18 | Excitation Current:<br>0 => 1.0 ma<br>1 => 2.0 ma<br>2 => 3.0 ma<br>3 => 5.0 ma<br>4 => 0.4 ma<br>5 => 10.0 ma<br>6-7 => (Reserved) |
| D19-D31 | (Reserved) |

# APPENDIX B

# MIGRATION FROM PMC-16AI64

# Appendix-B: MIGRATION FROM PMC-16AI64

Operation of the PMC-16AICS32 is similar to that of the PMC-16AI64. This appendix summarizes the primary issues involved in migrating an application from the PMC-16AI64 to the PMC-16AICS32.

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## PRINCIPAL CHANGES:

1. **New Registers (Sections 3.1, 3.9, 3.10 ):**
   Two new registers at 0030h, 0034h contain current-source control masks.
   Autocal-value and board configuration registers are identified.

2. **Defaults (Sections 3.1, 3.3.2):**
   Rate-A/B and Scan/Sync register defaults have changed.
   Rate-A and Rate-B generators are cascaded.
   Default scan rate is 50 scans per second.

3. **Maximum Sample Rate per-channel (Sections 3.4.4.1, 3.9):**
   The maximum scan rate is 100 KSPS divided by the number of channels in a scan.

4. **New I/O Connector (Section 2.2):**
   The maximum scan rate is 100 KSPS divided by the number of channels in a scan.

5. **Excitation Current Source (Table 2.2-1, Sections 2.3.1.3, 2.5, 3.9):**
   Excitation current can be applied to any of 32 inputs. Assignment of excitation to each channel is controlled under a mask.

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