General Standards Corporation

High Performance Bus Interface Solutions

Rev: 021417

PMC66-18AI64SSC750K

64-CHANNEL 18-BIT SIMULTANEOUS SAMPLING PMC ANALOG INPUT BOARD

With 750KSPS Sample Rate per Channel, 66MHz PCI Support, and Triggered Bursts

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REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC66-18AI64SSC750K is a single-width PCI mezzanine card (PMC) that provides high-speed simultaneous 18-bit analog input capability for PMC applications. 64 analog input lines can be digitized simultaneously at rates up to 750,000 conversions per second per channel, with software-controlled voltage ranges of ±5V, ±10V, 0 to +5V or 0 to +10V. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections digitally during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

Power requirements consist of +5 VDC from the PCI bus in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling. Specific details of physical characteristics and power requirements are contained in the PMC66-18AI64SSC750K product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

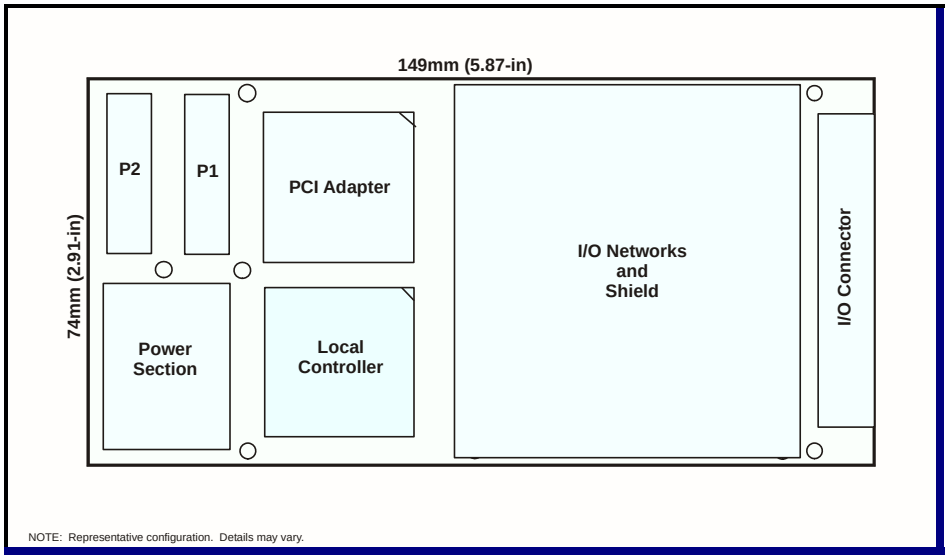

Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 80-pin, dual-ribbon front-access I/O connector.

1.2 Functional Overview

The 18-Bit PMC66-18AI64SSC750K analog input board (Figure 1.2-1) samples and digitizes 64 input channels simultaneously at rates up to 750,000 samples per second for each channel. The resulting 18-bit sampled data is available to the PCI bus through a 256K-Sample FIFO buffer (512K samples with 16-bit data packing). Each input channel contains a dedicated 18-Bit sampling ADC. All operational parameters are software configurable.

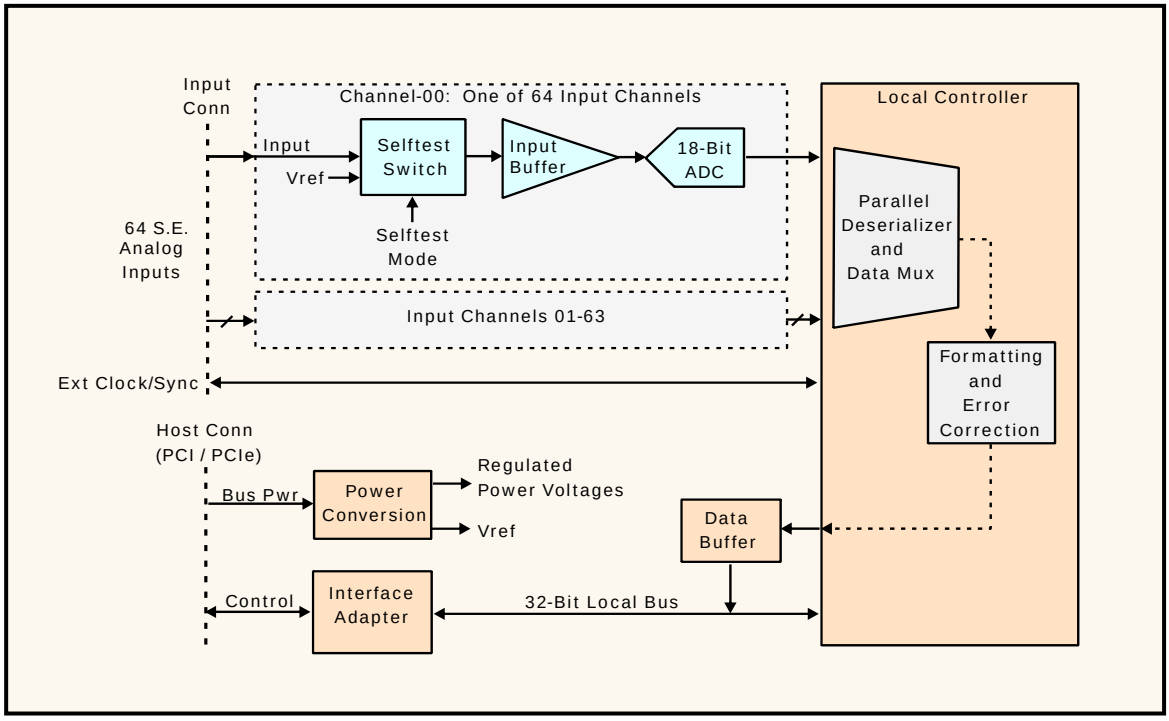

Figure 1.2-1. Functional Organization

Inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 channels, or any first and last channels in a scan can be selected. The sample clock can be generated from an internal rate generator, or directly through software, or by external hardware.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the bezel and standoffs are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the bezel and standoffs on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to 3M# P50E-080S-EA. The insulation displacement (IDC) cable connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. Contact the factory if preassembled cables are required.

Table 2.2-1. System Connector Pin Functions

PIN	ROW-A SIGNAL
1	INP00
2	INP01
3	INP02
4	INP03
5	INPUT RTN
6	INP04
7	INP05
8	INP06
9	INP07
10	INPUT RTN
11	INP08
12	INP09
13	INP10
14	INP11
15	INPUT RTN
16	INP12
17	INP13
18	INP14
19	INP15
20	INPUT RTN
21	INP16
22	INP17
23	INP18
24	INP19
25	INPUT RTN
26	INP20
27	INP21
28	INP22
29	INP23
30	INPUT RTN
31	INP24
32	INP25
33	INP26
34	INP27
35	INPUT RTN
36	INP28
37	INP29
38	INP30
39	INP31
40	INPUT RTN

PIN	ROW-B SIGNAL
1	INP32
2	INP33
3	INP34
4	INP35
5	INPUT RTN
6	INP36
7	INP37
8	INP38
9	INP39
10	INPUT RTN
11	INP40
12	INP41
13	INP42
14	INP43
15	INPUT RTN
16	INP44
17	INP45
18	INP46
19	INP47
20	INP48
21	INPUT RTN
22	INP49
23	INP50
24	INP51
25	INP52
26	INP53
27	INPUT RTN
28	INP54
29	INP55
30	INP56
31	INP57
32	INP58
33	INPUT RTN / CLK I/O [1]
34	INP59
35	INP60
36	INP61
37	INP62
38	INP63 / CLK I/O [2]
39	TRIG I/O RTN
40	TRIG I/O

[1] This pin can be factory configured either as an INPUT RTN. pin or as a CLK I/O pin. See ordering options. (Note: Configuring this pin as a CLK I/O pin prevents 100% pin-compatibility with the 16AI64SSC board).

[2] Software-programmable as either analog Input Channel 63, or as a TTL bidirectional CLK-I/O pin.

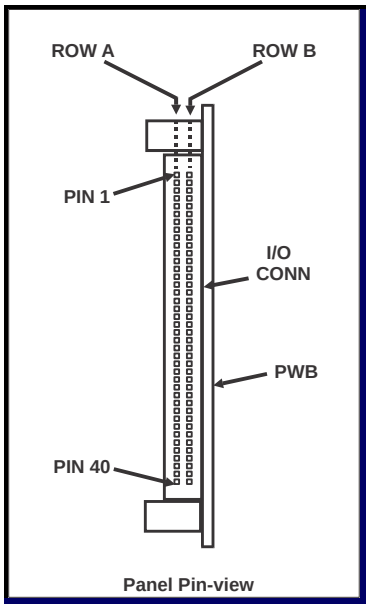

Figure 2.2-1. Input/Output Connector

2.3 System Configuration

2.3.1 Analog Inputs

Analog inputs INP00-INP63 (Table 2.2-1) can be configured as 1, 2, 4, 8, 16, 32 or 64 single-ended channels. Input configurations start at Channel-00, and proceed upward through consecutive channels to the highest-numbered channel in the configuration. The hardware input configuration must be acknowledged by the control software.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or may generate excessive ground current sufficient to damage the board.

A signal return pin (INPUT RTN) is provided in the I/O connector for every group of 4 or 5 input channels. If the signal sources are isolated from each other, and from system ground (Figure 2.3-1a), the returns in each channel group should be connected together at the source, and to at least one INPUT RTN pin in the connector.

For signal sources that have a common isolated return at the source (Figure 2.3-1b), the common return should be connected to at least one INPUT RTN pin for every 4 or 5 active input channels.

To minimize crosstalk between input channels at higher frequencies, all INPUT RTN pins should be connected to signal source returns. The INPUT-RTN pins are connected together internally within the board, and are electrically common to the system or PCIbus ground.

NOTE: Channel-63 can be software-designated alternatively as a bidirectional Clock I/O pin. Ground pin B33 can be factory-configured either as an analog ground or as a bidirectional Clock I/O pin.

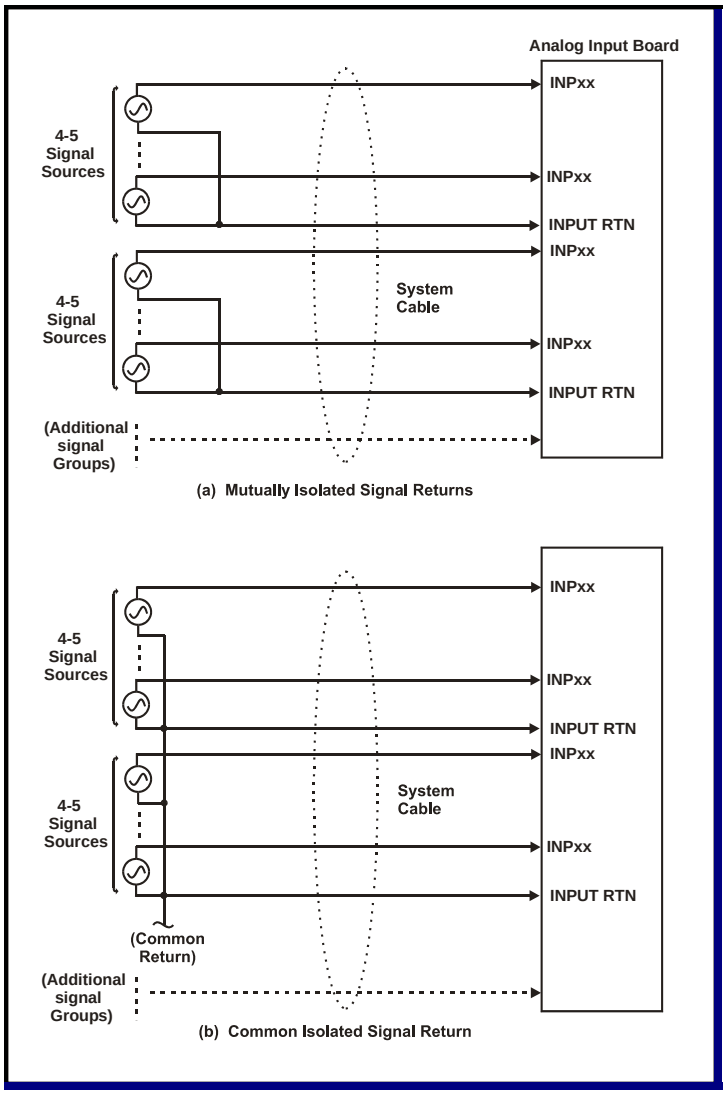

Figure 2.3-1. Analog Input Configurations

2.3.2 External Trigger I/O

The TRIG I/O pin in the I/O connector is a bidirectional TTL synchronization signal that provides external control of acquisition burst triggering. The TRIG I/O signal is referenced to the TRIG I/O RTN pin, which is connected internally to digital ground.

When configured as an input, this signal initiates a data acquisition triggered burst. The TRIG I/O input is asserted on a HIGH-to-LOW transition, and is pulled HIGH internally through a 4.7 KOhm resistor. Minimum input pulse width is 140ns.

When configured as an output, the TRIG I/O signal is asserted for approximately 140 nanoseconds at the beginning of each triggered burst. The TRIG I/O output signal is a TTL level that can synchronize the operation of multiple target boards to a single initiator board. Like the TRIG I/O input signal, the TRIG I/O output signal is asserted LOW. Loading of the SYNC output should be limited to 10 milliamps or less.

2.3.3 External Clock I/O

The CLK I/O pin in the I/O connector is a bidirectional TTL synchronization signal that provides external control of the analog input sample clock. When external clocking is enabled, the CLK I/O pin is configured as an input, and each external clock initiates a single sampling of all active input channels. In the default 'internal clocking' mode, the CLK I/O pin can be software-configured as an output that generates a single clock pulse each time the ADC's are sampled. The CLK I/O pin has the same TTL input and output characteristics as the TRIG I/O pin.

Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

NOTE: Refer to Paragraph 3.4.6 for auxiliary external sync provisions.

2.3.4 Multiboard Synchronization

If multiple boards are to be trigger-synchronized together, the TRIG I/O and TRIG I/O RTN pins from one board, the ***trigger initiator***, are connected to the TRIG I/O and TRIG I/O RTN pins of six or more ***trigger target*** boards (Figure 2.3-2). The controlling software determines specific synchronization functions.

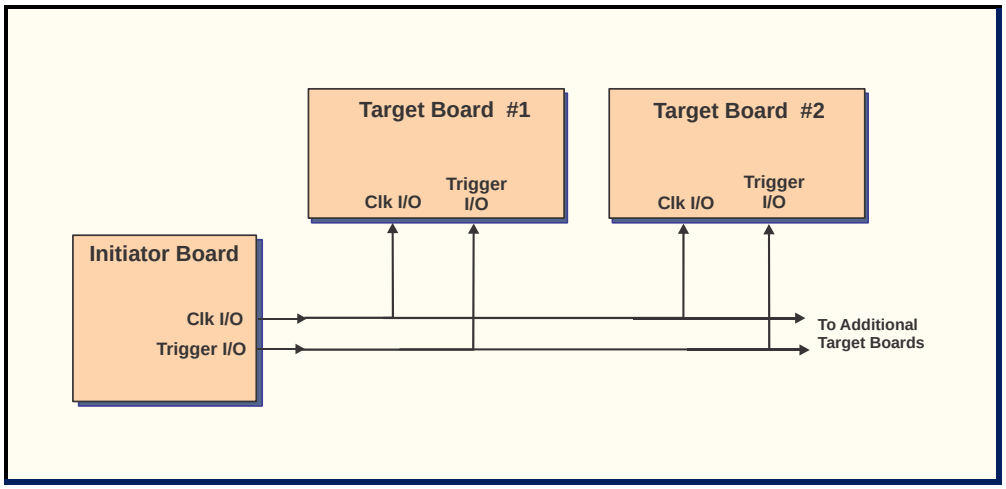

Figure 2.3-2. Multiboard Synchronization

For multiboard clocking from a single ***clock initiator***, the CLK I/O pins on the initiator and target boards are interconnected in the same manner that the TRIG I/O pins are interconnected for multiboard triggering.

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog input channels are software-calibrated to a single internal voltage reference by an embedded autocalibration software utility. The procedure presented here describes the verification and adjustment of the internal reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to two 0.024-inch square test posts.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the single reference voltage that ensures conformance to the product specification. Adjustment of the internal reference, if necessary, is performed with a single trimmer that is accessible as shown in Figure 2.5-1.

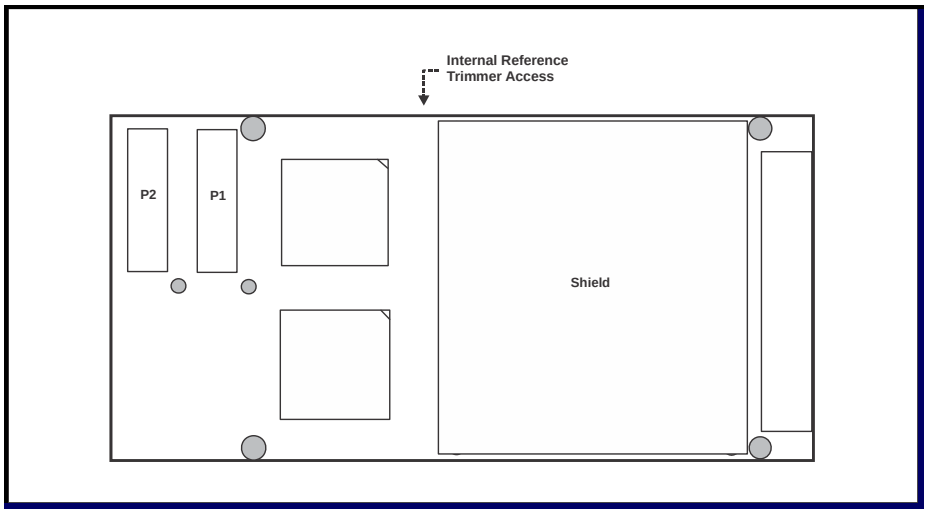

Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the board is installed on an operational host board.

1. Connect the digital multimeter between VCAL (+) Pin-3, and REF RTN (-) Pin-4 in the J3 test connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Select the highest available bipolar input range (Table 3.4-1).
4. Verify that the digital multimeter indication is +9.9900 VDC ±0.0008 VDC if the High range set is installed, or +4.9950 VDC ±0.0006 VDC if the Low range set is installed. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer until the digital multimeter indication is within the specified range. (The presence of the High or Low range set is identified in Table 3.9-1.).
5. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-18AI64SSC750K is compatible with the PCI Local Bus specification, and supports auto-configuration at the time of power-up. A PLX™ PCI-9056 adapter operating in J-mode controls the PCI interface, and supports both 33MHz and 66MHz PCI clock frequencies, as well as D32 PCI bus width. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space (Selection of the Low Latency mode extends the required memory space to 0200h bytes). After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All local data transfers are long-word D32. Specific operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer.

Table 3.1-1. Control and Data Registers

Offset (Hex)	Register	Mode	Default	Primary Function	Ref Para
0000	BOARD CONTROL (BCR)	RW	0000 4060h	Board Control Register (BCR)	3.2
0004	INTERRUPT CONTROL	RW	0000 0008h	Interrupt conditions and flags	3.7
0008	INPUT DATA BUFFER	RO	000X XXXXh	Analog input data buffer	3.5.1.1
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control	3.5.2
0010	RATE-A GENERATOR	RW	0001 07D0h	Rate-A generator frequency selection	3.4.4.1
0014	RATE-B GENERATOR	RW	0001 EA60h	Rate-B generator frequency selection	3.4.4.1
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer	3.5.2
001C	BURST SIZE	R/W	0000 0001h	Number of sample clocks in a triggered burst.	3.10.1
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Triggering sources.	3.4.3
0024	ACTIVE CHANNEL ASSIGNMENT	R/W	0000 0100h	Specific first and last active channels.	3.5.3.2
0028	BOARD CONFIGURATION	RO	000X XXXXh	Firmware revision and option straps.	3.9
002C	Autocal Values *	R/W	0000 080Xh	Autocal value readback.	---
0030	(Reserved)	R/W	0000 0000h	---	---
0034	AUXILIARY SYNC I/O CONTROL	R/W	0000 0000h	Controls auxiliary sync I/O port	3.4.6
0038	SCAN MARKER UPPER WORD	R/W	0000 0000h	Packed-data scan marker D[31..16].	3.5.1.2
003C	SCAN MARKER LOWER WORD	R/W	0000 0000h	Packed-data scan marker D[15..0]..	3.5.1.2
0040-00FC	(Reserved)	---	---	---	---
0100-01FC	LOW-LATENCY DATA	RO	0000 XXXXh	Low Latency data (Paragraph 3.14)	3.11

R/W = Read/Write, RO = Read-Only. * Maintenance register; shown for reference only.

3.2 Board Control Register (BCR)

The Board Control Register (BCR) controls primary board functions, including analog input mode and range. Table 3.2-1 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

Bit	Mode	Designation	Def	Description	Ref Para
D00-D02	R/W	AIM[2..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	UNIPOLAR INPUTS	0	Selects unipolar inputs when HIGH, bipolar inputs when LOW.	3.4.1
D04-D05	R/W	RANGE[1..0]	2	Analog input range. Defaults to the highest bipolar range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.	3.5.1.3
D07	R/W	16 BIT DATA	0	Data width is 16 bits if this bit is HIGH, or if data packing is selected. Otherwise, data width is 18 bits.	3.5.1.1
D08-D09	R/W	DIFFERENTIAL PROCESSING	0	Selects standard or differential processing.	3.5.5
D10	RO	DATA ON HOLD	0	Low-Latency access status flag.	3.11
D11	R/W	DISABLE SCAN MARKER	0	Disables the scan marker in data packing mode.	3.5.1.2
D12	R/W	*BURST TRIGGER	0	Triggers a single acquisition burst when BCR Input Trigger is selected in the Scan and Sync Control Register.	3.4.5.1 3.10.1
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.6
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	3.5.2
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.5.1.2
D19	R/W	*INPUT CLOCK	0	Initiates a single sample of all active channels when BCR Input Clock is selected in the Scan and Sync Control Register.	3.4.5.2
D20-D31	RO	(Reserved)	0	---	---

R/W = Read/Write, RO = Read-Only. *Clears automatically when operation is completed

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset, and should be required only once after the initial application of power. PCI register configuration terminates with the PCI interrupt disabled.

3.3.2 Initialization

Internal control logic can be initialized without reconfiguration of the PCI registers by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all defaults are invoked (3.3.2).
- Analog input voltage range is ±10 Volts (3.4.1).
- 32 channels are active (3.5.3.2).
- Data resolution is 18 bits (3.5.1.1).
- Input sample clocking is from the Rate-A generator at 30.00KSPS (3.4.4.1).
- The input rate generator Rate-A is disabled (3.4.4.1).
- Burst triggering is adjusted to 1000 per second, and is disabled (3.4.4.1, 3.10).
- Analog input data coding format is offset binary (3.5.1.3).
- Data packing is disabled (3.5.1.2).
- The analog input buffer is reset to empty (3.5.2),

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Parameters

3.4.1 Input Voltage Range

BCR control fields RANGE[] and UNIPOLAR_INPUTS select the analog input voltage range as shown in Table 3.4-1. The presence of either the High or Low range set is identified in Table 3.9.1.

Table 3.4-1. Input Voltage Range Selection

	HIGH Range Set Installed		LOW Range Set Installed Set	
Range[1:0]	**Bipolar Inputs 'Unipolar' = Low**	**Unipolar Inputs 'Unipolar' = High**	**Bipolar Inputs 'Unipolar' = Low**	**Unipolar Inputs 'Unipolar' = High**
0				
1	±5 Volts	0/+10 Volts	±2.5 Volts	0/+5 Volts
2	±10 Volts		±5 Volts	0/+10 Volts
3				

(Shaded areas are reserved.)

NOTE: Allow a settling interval of at least 1-second after (a) changing the input range, or (b) performing a reset operation.

3.4.2 Timing Organization

Figure 3.4-1 illustrates the manner in which sample clock timing is organized within the board. The input sample clock selector is controlled by the Scan and Sync control register which provides direct software control of clocking and burst-triggering operations. The external CLK and TRIG I/O lines permit external control of timing. Two rate generators operate directly from the master clock frequency, or can be cascaded.

A sample clock can be generated by either rate generator, by the INPUT CLOCK control bit in the BCR, or by the CLK I/O external line. Each Input Sample Clock initiates a sample of all active input channels. An active channel group can contain from two to 64 channels, or any single channel can be sampled individually.

A burst of a predetermined number of samples can be initiated internally by the Rate-B generator or by the BURST TRIGGER control bit in the BCR. Also, the TRIG I/O line can be programmed to trigger a burst from an external trigger source.

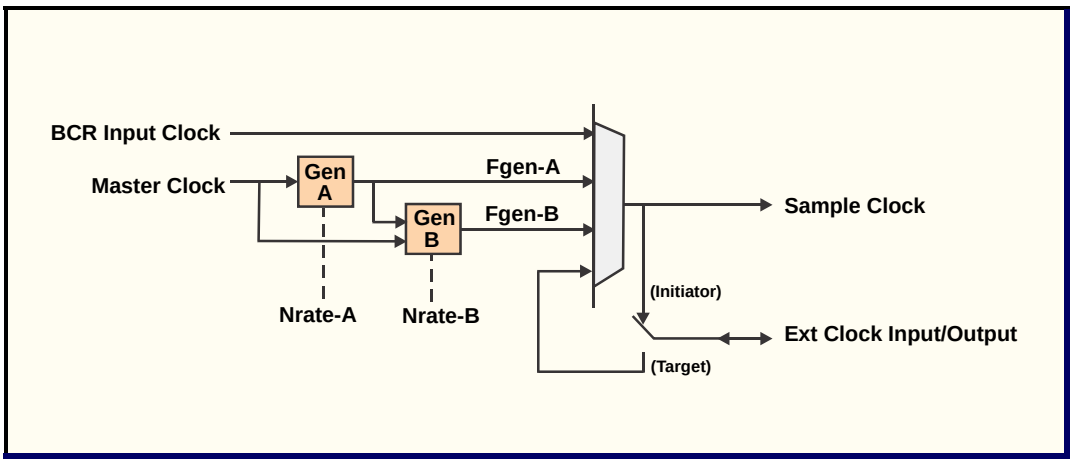

Figure 3.4-1. Sample Clock Organization

3.4.3 Scan and Sync Control Register

The Scan and Sync control register (Table 3.4-2) controls the configuration of internal timing signals.

3.4.4 Sample Rate Generators

Each of the two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate register. The two rate registers are organized as shown in Table 3.4-3. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. To prevent the input buffer from filling with extraneous data at power-up, D16 defaults to the HIGH state in both the Rate-A and Rate-B control registers.

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

Bit	Mode	Designation	Def	Description	Ref Para
D00-D02	R/W	ACTIVE CHANNELS	5	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 32 channels (00-31); Default value 6 => 64 channels (00-63) 7 => Channel group assignment * Channel selected by the Single-Channel Select field below.	3.5.3.2
D03-D04	R/W	SAMPLE CLOCK SOURCE	0	Selects the analog input sample clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External CLK I/O input line (Selects ***Clock-Target*** mode) 3 => BCR Input Clock control bit.	3.4.5.2 3.10.2
D05-D06	R/W	BURST TRIGGER SOURCE	0	Selects the analog input burst trigger source: 0 => Internal Rate-B generator output 1 => Internal Rate-A generator output 2 => External TRIG I/O pin (Selects ***Trigger-Target*** mode) 3 => BCR Burst Trigger control bit.	3.4.5.1 3.10.1
D07	RO	BURST BUSY	0	Indicates a burst in progress.	3.10.1
D08	R/W	ENABLE BURST	0	When HIGH, enables triggered bursts.	3.10
D09	R/W	INPUT 63 AS CLOCK IO	0	When High, configures the INP63 pin in the system I/O connector as a bidirectional TTL CLK I/O pin.	3.4.5.2
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.	3.10.1
D11	R/W	ENABLE CLOCKING	0	Enables the currently selected clocking process.	3.4.5.2
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.	3.5.3.2
D18	R/W	ENABLE CLOCK OUT	0	Configures the CLK I/O pin as an output if external clocking is not selected.	3.4.5.2
D19	R/W	ENABLE TRIGGER OUT	0	Configures the TRIG I/O pin as an output if external triggering is not selected.	3.4.5.1
D20-D31	RO	(Reserved)	---	---	---

R/W = Read/Write, RO = Read-Only.

3.4.4.1 Sample Rate Control

Each rate generator is controlled by a *divisor* **Nrate** that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of **Fclk** (MHz), the output frequency **Fgen** of each generator is determined as:

Fgen (Hz) = Fclk (Hz) / Nrate,

where **Nrate** is the decimal equivalent of D00-D15 in the rate generator register. **Fgen** is the sampling frequency, and equals the rate at which all active channels are sampled. **Fclk** has a standard value of 60.000MHz, but may have other values depending upon custom ordering options. The maximum sampling frequency **Fgen-max** is 750 kHz.

NOTE: The acceptable frequency range for both the internal Rate-A generator and the external Clock input and output system I/O is 0-750kHz.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 07D0 (Rate-A), 0001 EA60h (Rate-B)**

Data Bit	Mode*	Designation	Default	Description
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		Fgen Frequency (60 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
80	50	750,000
81	51	740,741
---	---	Fgen (Hz) = 60,000,000 / Nrate

* ±0.015 percent.

3.4.4.2 Generator Cascading

To provide very low sample rates, the Rate-B generator can be configured with the RATE-B CLOCK SOURCE control field to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

Fgen-B (Hz) = Fclk / (Nrate-A * Nrate-B) ,

which can produce sample or burst rates as low as 0.014 Hz with **Fclk** = 60 MHz.

3.4.4.3 Multiboard Synchronization

Multiple boards can be interconnected externally to produce synchronous analog input sampling or burst triggering. Figure 2.3-2 illustrates the interconnections required for synchronized operations. External TRIG I/O is enabled by setting the BURST TRIGGER SOURCE control field in the Scan and Sync control register. One of the boards is designated as the ***trigger initiator***, and the remaining boards are designated as ***trigger targets*** (see also 3.5).

Multiple boards can also be ***sample-clocked*** synchronously by interconnecting their CLK I/O lines and designating one of the boards as the ***clock initiator***, and the others as ***clock targets***.

NOTE: External Clock and Trigger lines are active on the falling edge (High-to-Low transition), for both inputs and outputs.

3.4.5 Triggers and Sample Clocks

3.4.5.1 Burst Triggering

A board is configured as a ***trigger initiator*** setting the ENABLE TRIGGER OUT control bit HIGH in the Scan and Sync control register. The trigger then can originate either as the Rate-B or Rate-A generator output, or by the BURST TRIGGER control bit in the BCR. As a trigger initiator, the board generates an output pulse on the TRIG I/O as each burst is initiated internally.

A board is configured as a ***trigger target*** by selecting the external TRIG I/O pin as the BURST TRIGGER SOURCE, and by clearing the ENABLE TRIGGER OUT control bit LOW. Any other value for the BURST TRIGGER SOURCE field provides the trigger internally. The external trigger signal can originate either from an initiator board, or from any TTL pulse source.

3.4.5.2 Sample Clocking

Clocking is enabled by setting the ENABLE CLOCKING control bit HIGH in the BCR. A board is configured as a ***clock initiator*** by setting the ENABLE CLOCK OUT control bit HIGH in the Scan and Sync control register. The sample clock then can originate either as the Rate-A or Rate-B generator output, or by the INPUT CLOCK control bit in the BCR. As a clock initiator, the board generates an output pulse on the CLK I/O line as each internal sample clock occurs. The external CLK I/O signal can be factory-assigned as a replacement for Ground Pin-B33, or software-assigned as a replacement for the Channel-63 input at Pin-B38.

A board is configured as a ***clock target*** by selecting the external CLK I/O pin as the SAMPLE CLOCK SOURCE, and by clearing the ENABLE CLOCK OUT control bit LOW. Any other value for the SAMPLE CLOCK SOURCE field provides the sample clock internally. The external clock signal can originate either from an initiator board, or from any TTL pulse source.

NOTE: To avoid contention on the TRIG I/O and CLK I/O lines, initiator and target designations should be assigned for all boards before setting the ENABLE CLOCK OUT or ENABLE TRIGGER OUT control bits in the initiator's Scan and Sync control register. Only one board can be designated as an initiator.

NOTE: The acceptable frequency range for both the internal Rate-A generator and the external Clock input and output system I/O is 0-750kHz.

3.4.6 Auxiliary External Sync I/O

Internal auxiliary external connections provide an alternate method of synchronizing sample clocking and burst triggering to external events when the CLK I/O and TRIG I/O lines are selected for the SAMPLE CLOCK SOURCE and BURST TRIGGER SOURCE in the Scan and Sync control register. The auxiliary clock and trigger lines are shown in Table 3.4.6-1.

Table 3.4.6-1. Auxiliary Sync I/O Connections

Signal	Pin
DIGITAL RETURN	1
AUX CLOCK	2
DIGIAL RETURN	3
AUX TRIGGER	4
DIGITAL RETURN	5
(Reserved)	6

These TTL connections are available as AUX-CLOCK and AUX-TRIGGER, and are accessible through a 6-Pin header on one edge of the board (refer to the product specification for connector details). The 'Reserved' pin can either be grounded or left disconnected.

AUX sync signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.4.6-2. When an AUX signal is designated as an *input*, the signal replaces the clock or trigger input from the system connector, ***and the board must be configured to accept an external clock or trigger***, as selected in the Scan and Sync control register (Table 3.4-2). 'Inactive' and 'Active Input' AUX lines are pulled to +5VDC internally through 4.7K.

Active AUX *outputs* produce an output pulse for each ADC sample clock or burst trigger, and are active in both target and initiator external sync modes. Source and sink load capacity of each output is 15 milliamps.

To increase the reliability of external triggering in high-noise environments, selectable noise suppression increases the debounce or detection interval for active inputs, and increases the pulse width of active outputs.

Table 3.4.6-2. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Bit	Mode	Designation	Def	Description
D00-D01	R/W	AUX-CLOCK CONTROL	0	AUX-CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-D03	R/W	AUX-TRIGGER CONTROL	0	AUX-TRIGGER I/O Control Mode 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D04-D07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 90ns and output pulse width is 140ns. When HIGH, input debounce time is 400ns, and output pulse width is 500ns.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

AUX *inputs* are edge-detected as LOW-to-HIGH transitions if the INVERT INPUTS control bit is LOW, or as HIGH-to-LOW transitions if the bit is HIGH. Minimum HIGH and LOW level durations are 90ns if the NOISE SUPPRESSION control bit is LOW, or 400ns if the bit is HIGH. AUX *output pulses* are positive (i.e.: baseline level is LOW) if the INVERT OUTPUTS control bit is LOW, or negative (baseline HIGH) if the control bit is HIGH. Output pulse width is typically 140ns if the NOISE SUPPRESSION control bit is LOW, or 500ns if the bit is HIGH.

3.5 Analog Input Control

3.5.1 Input Data Organization

Processed conversion data from the analog-to-digital converters (ADC's) flows directly into the 256K-sample analog input FIFO data buffer (512 samples with 16-bit data packing), and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

3.5.1.1 Input Data Buffer

Nonpacked analog input data is right-justified to the LSB, and occupies bit positions D00 through D17 (Table 3.5-1). D18 is HIGH for the first (lowest-numbered) channel in any active channel group, and is LOW for data from all other channels. Bits D19-D31 are returned as zeros. An empty buffer returns an indeterminate value. Refer to Paragraph 3-5.1.2 for the configuration of packed data.

NOTE: If the 16 BIT DATA control bit is HIGH in the BCR, input data is 16 bits wide, whether or not data packing is selected. The FIRST CHANNEL TAG however, remains at the D18 position.

Table 3.5-1. Input Data Buffer; Nonpacked 18-Bit Data

Offset: 0008h **Default: N/A**

Data Bit	Mode *	Designation	Description
D00	RO	DATA00	Least significant data bit
D01-D16	RO	DATA01 - DATA16	Intermediate data bits
D17	RO	DATA17	Most significant data bit
D18	RO	FIRST CHANNEL TAG	Accompanies the first channel in any active channel group (3.5.3.2).
D19-D31	RO	(Reserved)	Inactive

* RO indicates read-only access. Write-data is ignored.

3.5.1.2 Data Packing

Data packing effectively doubles the capacity of the input data buffer, but reduces the data resolution from 18 bits to 16 bits. Setting the ENABLE DATA PACKING control bit high in the BCR selects the data packing mode, in which (a) all input data is right-shifted to 16 active bits, and (b) two consecutive 16-bit data values are packed into a single 32-Bit local data longword. In the data packing mode, a 32-bit scan marker code is inserted directly before each Channel-00 data value in the buffer. ***The scan marker can be disabled by setting the DISABLE SCAN MARKER control bit HIGH in the BCR.***

The scan marker code is defined by the 'Scan Marker Upper Word' and 'Scan Marker Lower Word' registers listed in Table 3.1-1, and is inserted immediately before the first (Channel-00) value in each data scan as shown in Table 3.5-2. The lower 16 bits in each register contains one word of the code. The upper 16 bits of these registers are ignored, and should be written as all-zero.

Table 3.5-2. Data Packing

	Buffer Data Field *					
	ENABLE DATA PACKING = 0 DISABLE SCAN MARKER = X		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 0		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 1	
Buffer Lword Order	**D18** (D[31..19] = all zero)	**D[17..0]**	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**
00	1	1st Chan Data	Upper Marker	Lower Marker	2nd Chan Data	1st Chan Data
01	0	2nd Chan Data	2nd Chan Data	1st Chan Data	4th Chan Data	3rd Chan Data
02	0	3rd Chan Data	4th Chan Data	3rd Chan Data	6th Chan Data	5th Chan Data
03	0	4th Chan Data	6th Chan Data	5th Chan Data	8th Chan Data	7th Chan Data
---	---	---	---	---	---	---

* "1st Chan Data" is Chan-00 data unless 'Channel Group Assignment' is selected in the Scan and Sync control register.

Some applications may require the scan marker code to be absolutely unique and not appear randomly in the data. To support this requirement, an all-zero marker code (0000 0000h) causes every all-zero data value (0000h) to be forced to a unit code (0001h) when data packing is enabled. This arrangement supports the uniqueness requirement without affecting the differential nonlinearity of the data itself.

3.5.1.3 Data Coding Format

Analog input data is arranged as 18 active right-justified data bits with the coding conventions shown in Table 3.5-3. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

Refer to Section 3.5.1.2 for the effect of data packing on buffer contents.

Table 3.5-3. Bipolar Input Data Coding; 18-Bit Data

Analog Input Level	**Digital Value (Hex)**	
	Offset Binary	**Two's Complement**
Positive Full Scale minus 1 LSB	0003 FFFF	0001 7FFF
Zero	0002 0000	0000 0000
Zero minus 1 LSB	0001 FFFF	0003 FFFF
Negative Full Scale	0000 0000	0002 0000

NOTE: Only the data MSB is affected by the selected data coding. The 'sign' bit is not extended through the remainder of the data field.

3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-4 controls and monitors the flow of data through the analog input data buffer. Asserting the CLEAR BUFFER control bit HIGH clears, or empties, the buffer. The Threshold Flag is HIGH when the number of values in the input data buffer ***exceeds the input threshold value*** defined by bits D00-D17, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.7) can be programmed to occur on either the rising or falling edge of the threshold flag.

The Buffer Size register shown in Table 3.5-5 contains the number of input values present in the buffer, and is updated continuously.

Buffer underflow and overflow flags in the BCR indicate that the buffer has been read while empty or written to when full. Each of these situations is indicative of data loss. Once set HIGH, each flag remains HIGH until cleared, either by directly clearing the bit LOW, by clearing the buffer or by initializing the board.

Table 3.5-4. Input Data Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

Data Bit	Mode*	Designation	Def	Description
D00-D17	R/W	THRESHOLD VALUE	3_FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D20-D31	RO	(Reserved)	0	Inactive

*Clears automatically within 200ns of being set

Table 3.5-5. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

Data Bit	Mode*	Designation	Def	Description
D00-D18	RO	BUFFER SIZE	0_0000h	Number of values in the input buffer
D19-D31	RO	(Reserved)	0	Inactive

3.5.3 Analog Input Function Modes

BCR control field AIM[] selects the analog input signal source, and provides selftest modes for monitoring the integrity of the analog input networks. Table 3.5-6 summarizes the input function modes.

3.5.3.1 System Analog Inputs

With the default value of 'Zero' selected for the AIM[] field in the BCR, all ADC channels are connected to the system analog inputs from the system I/O connector.

Table 3.5-6. Analog Input Function Selection

AIM[2:0]	Function or Mode
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

3.5.3.2 Active Channel Assignments

The assignment of active channels can be controlled with the ACTIVE CHANNELS control field in the Scan and Sync control register. This field supports the definition of active channel groups with specific sizes that begin with Channel-00, or allows the selection of any single channel as active.

If "Channel group assignment" is selected in the ACTIVE CHANNELS field in the Scan and Sync control register (Table 3.4-2), the first and last active channels are defined by the Active Channels Assignment control register shown in Table 3.5-7. The group of active channels is *contiguous*, beginning with the channel designated by the FIRST CHANNEL SELECT field, and proceeding upward through consecutive channels to (and including) the channel designated by LAST CHANNEL SELECT. The LAST CHANNEL SELECT value must be greater than the FIRST CHANNEL SELECT value.

Table 3.5-7. Active Channel Assignment

Offset: 0000 0024h **Default: 0000 0100h**

Data Bit	Mode	Designation	Default	Description
D00-D07	R/W	FIRST CHANNEL SELECT	0	First (lowest-numbered) active channel
D08-D15	R/W	LAST CHANNEL SELECT	1	Last (highest-numbered) active channel
D16-D31	RO	(Reserved)	0	Inactive. Returns all-zero.

The first, or lowest-numbered, channel in any active group is accompanied by a HIGH state for the FIRST CHANNEL TAG listed in Table 3.5-1. For example, if FIRST CHANNEL SELECT = 05, then D18 in the buffer will be HIGH for Channel-05 data, and LOW otherwise.

NOTE: Because Channel-00 is used as the differential reference for all other input channels in the pseudo-differential processing mode (3.5.5.2), Channel-00 must always be the First Channel when operating in the pseudo-differential mode.

Similarly, when operating in the full-differential mode (3.5.5.3), the First and Last Channels must always be even-numbered and odd-numbered channels, respectively.

3.5.3.3 Selftest Modes

In the selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and the averaged values of multiple samples should be used for critical measurements.

The ZERO selftest applies a Zero reference signal to all input channels, and should produce a nominal midscale reading of 0002 0000h for bipolar inputs, or 0000 0000h for unipolar inputs. For the +VREF test, a precision reference voltage is applied to all inputs. ***The +VREF reference voltage equals 99.90% of the positive fullscale value (nominally 0003 FF7Ch) for bipolar ranges, or 49.95% for unipolar ranges.***

3.5.4 Sampling Modes

The analog inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 active channels, or any single channel can be selected for digitizing. The number of active channels is selected by the ACTIVE CHANNELS[] field in the scan and sync control register. Each active channel group commences with Channel-00, and proceeds upward through successive channels to the selected number of channels.

For Single-Channel sampling (ACTIVE CHANNELS[] = 0), the channel to be digitized is selected by the SINGLE-CHANNEL SELECT control field.

NOTE: Refer to Section 3.5.3.2 to designate a specific group of active channels.

3.5.5 Differential Processing

Although the hardware inputs are single-ended in nature, differential processing allows the inputs to appear as either pseudo-differential or full-differential channels. Each of these processing modes is characterized by the reference from which the signal in each channel is measured. Differential processing is selected by the DIFFERENTIAL PROCESSING control field in the BCR as shown in Table 3.5-8.

3.5.5.1 Default Single-Ended Processing

For single-ended channels, each input signal is measured with respect to the common input return. That is, each channel reports the difference between the input signal voltage and the voltage present on the common input return. This configuration provides the maximum number of input channels, but allows noise and other forms of interference on the common return line to appear in the signal measurement.

Table 3.5-8. Differential Processing Modes

BCR D08,09	Designation	Processing Function
0	SINGLE ENDED	Default operating mode. Processing of input data is limited to gain and offset error correction.
1	PSEUDO-DIFFERENTIAL	Channel-00 is the input LO reference for all other channels.
2	FULL DIFFERENTIAL	Each odd-numbered channel is the LO reference for each even-numbered HI channel. I.e.: Channels 00 and 01 become Channel-00 HI and Channel-00 LO, respectively.
3	(Reserved)	

3.5.5.2 Pseudo-Differential Mode

Pseudo-differential processing designates input Channel-00 as the reference for all other channels, and subtracts the sampled value in Channel-00 from the sampled values in all other channels. With this arrangement, noise and interference on the common return line is essentially cancelled, and the Channel-00 input line can be used as a 'remote sense' line for Channels 01-63. ***Channel-00 can no longer be used as a measurement channel when operating in this mode, and appears in the acquisition sequence with a zero-level value***.

3.5.5.3 Full Differential Mode

If full-differential processing is selected, each odd-numbered channel becomes the reference level for the associated even-numbered channel. For example, Channel-01 becomes the reference for Channel-00, and Channel-00 data is reported as the difference between the actual Channel-00 input signal and the signal in Channel-01. ***Odd-numbered channels do not appear in the data buffer when operating in full-differential mode, which reduces the number of data channels to one-half the selected number of active channels.***

Note: Because the same signal is applied to all channels simultaneously when a selftest operation is selected (3.5.3.3), selftest always produces a zero-level when operating in either differential processing mode.

3.5.5.4 Differential Scaling Considerations

Because differential processing operates by subtracting the signal values in two channels, all input ranges are effectively doubled when either differential mode is selected. With the ±10V range and pseudo-differential operation selected for example, Channel-00 data can have any value from -10V to +10V, and all channels using Channel-00 as a reference also have the same range of values. The difference signal then can have any value from -20V to +20V, and the effective input range becomes ±20V.

Note: Although differential processing effectively doubles the output data range, the hardware input levels are still restricted to the selected input range.

In addition to doubling the effective input voltage range, differential processing also always produces a bipolar output signal. Since a reference channel can have a value that is greater than or less than that in a signal channel, ***differentially processed data is always bipolar in nature.***

Because the input scale is effectively doubled in differential modes, the difference values are halved in order to accommodate all values within the useable digital data range. For example, the difference between the values 31000h and 30000h would be reported as 20800h, in which the 1000h difference is halved to 0800h, and the data is reported in bipolar format.

3.6 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup or a System reset,
- Input range change,

A small error, on the order of 0.04-percent, can be introduced when the input range is changed. Performing autocalibration with the required sample rate selected eliminates this error.

During autocalibration, no control settings are altered and external analog input signals are ignored.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a maximum duration of approximately 4.0 seconds. Completion of the operation can be detected either by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.7) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.7.1)
b. The *PCI interrupt* must be enabled (Section3.7.2).

A local interrupt request will not generate a PCI bus interrupt unless the PCI interrupt has been enabled as described in Paragraph 3.7.2.

3.7.1 Local Interrupt Request

The Interrupt Control Register shown in Table 3.7-1 controls the single local interrupt request line. Two simultaneous source conditions (IRQ 0 and1) are available for the request, with multiple conditions available for each source. IRQ 0 and 1 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for either of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *Local Interrupt Input Enable* control bits HIGH in the *Runtime Interrupt Control/Status Register* described in Section 6 of the PLX™ PCI-9056 reference manual.

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

Data Bit	Mode	Designation	Def	Value	Interrupt Event
D00-02	R/W	IRQ0 A0,1,2	0	0	Initialization completed.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4	Triggered burst initiated (BURST BUSY => HI)
				5	Triggered burst completed (BURST BUSY => LO)
				6-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	Input buffer overflow or underflow
				4-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Reserved)	0	---	---

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

3.8 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master, in either DMA Channel 00 or Channel 01. Set bit D[02] in the PCI Command register HIGH to select the bus mastering mode. Also, clear D[15] LOW in the PCI-9056 DMA Mode register to select *slow-terminate* operation. Refer to the PCI-9056 reference manual for a detailed description of DMA configuration registers.

3.8.1 Block Mode

Table 3.8-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.8.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.8-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty* during a demand-mode DMA sequence, the situation can arise in which the last one or two samples in an active channel group are retained in the buffer until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

3.9 Production Configuration Register

The read-only production configuration register (Table 3.9-1) contains the existing firmware revision, and a status field that indicates the configuration of optional features.

Table 3.9-1. Production Configuration Register

Offset: 0000 0028h **Default: 000X XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12	High if the board contains only 32 input channels.
D13-D14	Master Clock Frequency Fclk: 0 => 60.000 MHz 1-3 => (Reserved)
D15-D16	Input Bandwidth (±20%): 0 => 200kHz 1 => 70kHz 2-3 => (Reserved)
D17	I/O Pin-B33 function: 0 => Pin B33 = Input Return 1 => Pin B33 = CLK I/O
D18	0 => High range set; 1 => Low range set.
D19	Custom Feature:
D20-D31	(Reserved)

3.10 Triggered Bursts

When the ENABLE BURST control bit is HIGH in the Scan and Sync control register (Table 3.4-2), a trigger will initiate an acquisition burst. During a triggered burst, all active channels are sampled a specific number of times.

3.10.1 Burst Size and Trigger Source

The number of sample clocks issued during a burst is controlled by the 20-bit **Burst Size** control register listed in Table 3.1-1, which has a range from 1 to 1,048,575 sample clocks. For Burst-Size values of one or greater, the number of sample clocks in a burst equals the value in the register. For example, if a burst size of 10 is selected while 16 channels are active, then each burst will contain 160 sample values. Selection of the burst trigger source is controlled by the BURST TRIGGER SOURCE control field in the Scan and Sync control register. A Burst-Size of zero produces a burst that extends continuously until stopped, either by disabling the internal clock or by clearing the ENABLE BURST control bit.

The TRIG I/O pin in the system I/O connector can operate as an input or output trigger pin. The trigger output can serve as a burst trigger for target boards in which the ENABLE BURST control bit is asserted and the External TRIG I/O pin is selected in the BURST TRIGGER SOURCE control field.

NOTE: During a triggered burst the BURST BUSY status flag in the Scan and Sync control register goes HIGH at the trigger event, and returns LOW at the end of the burst. Either edge of the BURST BUSY flag is selectable as an interrupt event (Table 3.7-1).

The Rate-B generator frequency source can be selected as either the master clock frequency or the Rate-A generator output, as indicated by the RATE-B CLOCK SOURCE control field in the Scan and Sync control register.

3.10.2 Sample Clock Source

The sample-clock source is selected by the SAMPLE CLOCK SOURCE field in the Scan and Sync control register. The single restriction on the sample clock source is that the burst trigger and the sample clock can not use the same source simultaneously.

The following sequence illustrates the setup for a typical burst operation:

1. Select the Input Range, Sample Clock Source, and Burst Size, with clocking disabled,
2. Select the Burst Trigger Source and set the Enable Burst control bit,
3. Clear the buffer, then enable the clock and trigger rate generators.

3.11 Low Latency Data Access

The Low-Latency data array consists of 64 18-bit Acquisition Registers followed by 64 Holding Registers. During each ADC data acquisition sequence, the acquisition registers are loaded sequentially with processed ADC data as the data for each channel becomes available. When data is loaded into the last (64th) acquisition register, all 64 data values are transferred simultaneously into the holding registers. Low-latency data consists of fully processed ADC samples, with normal calibration and differential processing (if selected) operations applied. Data packing however, is not supported.

The Holding Registers are available as an array of 64 Lword registers, each containing 18-bit ADC data, located at local offsets 0100h through 01FCh. Reading the Channel-00 register at 0100h initiates a 'Data-On-Hold' state in which the holding data registers are no longer updated from the acquisition registers, and in which the last data sample set is 'locked' into the holding registers. Data in the holding registers remains locked until data is read from the 64th channel at the 01FCh location, after which data transfer from the acquisition registers to the holding registers resumes. Low-Latency data is accessible with 'single-read' transfers.

The DATA ON HOLD status flag in the BCR is asserted HIGH while the register array is in the 'Data-On-Hold' state. The Low Latency mode does not affect any other board functions, all of which operate independently of the low latency mode.

NOTE: Low latency data is not subject to the limitations imposed upon the FIFO data buffer (3.5.2), and current input data will continue to appear in the low latency registers, even if the FIFO buffer is full or disabled.

Also, the low latency data always represents all available channels, regardless of the selected 'Active Channels' and related settings that control data channels in the FIFO buffer.

3.12 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance might be suspended. Abrupt changes include:

- ***A change in the input voltage range*****,**
- ***A system or local reset,***
- ***Power application,***
- A change in sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,

NOTE: A change in the input voltage range changes the internal reference voltage, and requires a settling interval of at least 1-second. A similar settling requirement occurs at the initial application of power or after a software reset.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in sample rate, to 1-second after a voltage range change or software reset, to as long as several minutes after the initial application of power. For *most* configuration changes other than the application of power, and range changes, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of 64 single-ended analog input channels contains a dedicated 18-Bit ADC, an input buffer, and a selftest input switching network (Figure 4.1-1). The input buffer contains an attenuator that reduces the input signal to a level compatible with the ADC, and which inserts the offset voltage required when acquiring bipolar input signals. A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller. +5 VDC power from the PCIbus is converted into regulated power voltages for the internal analog networks. Differential processing supports pseudo-differential and full-differential processing modes.

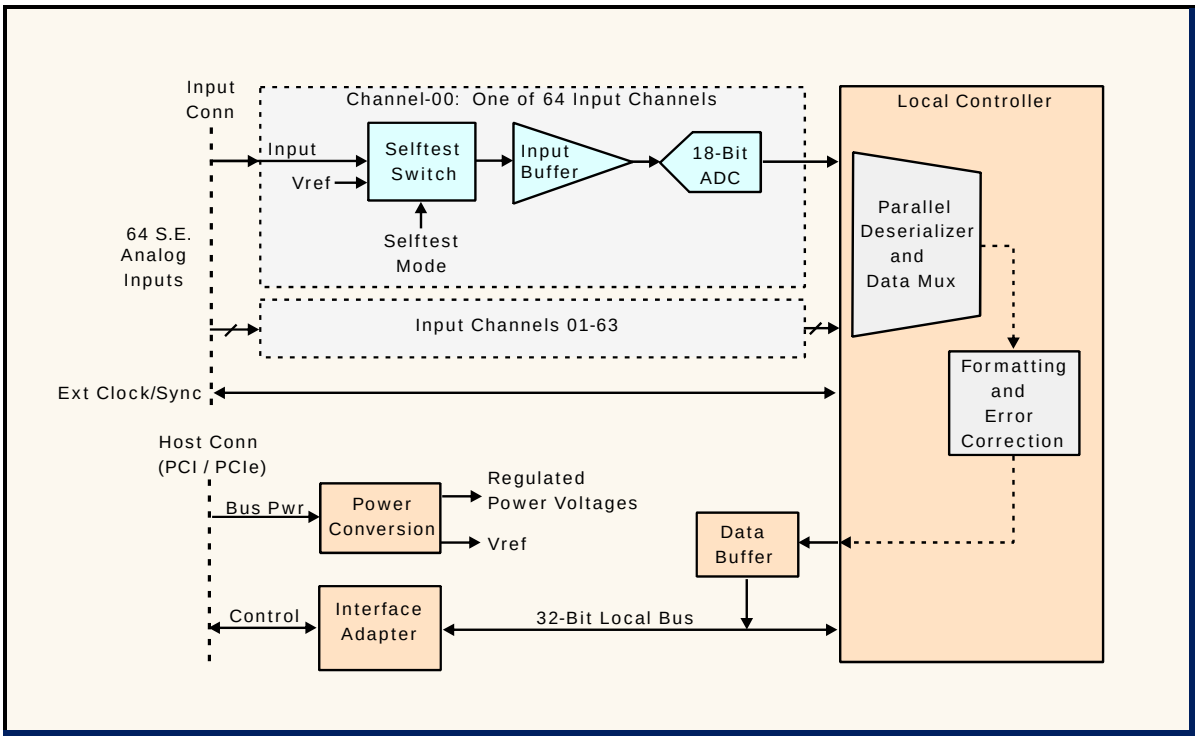

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input channels, and the input attenuator is biased to accept bipolar input ranges. The input range is controlled by adjusting the 18-Bit ADC reference voltage. Each input sample is corrected for gain and offset errors with calibration values determined during autocalibration. A 256 Ksample FIFO buffer (513K samples with data packing) accumulates analog input data for subsequent retrieval by a PMC host.

Analog input sampling on multiple target boards can be synchronized to a single software-designated initiator board. An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, the ADC's receive system analog input signals from the input connector. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC. An input attenuator in each channel provides the necessary scaling and offset parameters to support bipolar input ranges.

Serial data from each ADC is deserialized and multiplexed into a parallel data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies gain and offset correction values obtained during autocalibration. The corrected data is formatted, a tag is attached to the lowest-numbered active data channel, and the data is finally loaded into the analog input data buffer.

4.3 Rate Generators

The local controller contains two independent rate generators, each of which divides the master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a clocking source for the analog inputs, and the generators can be cascaded to produce very long clocking intervals.

4.4 Data Buffer

The FIFO data buffer accumulates analog input data for subsequent retrieval through the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by a threshold flag that can be used to generate an interrupt request when the number of values in the buffer moves above or below a specific count.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

An internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample that is acquired during acquisition. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated supply voltages of +2.5VDC, +5 VDC and ±15 VDC are required for internal analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and subsequently by linear postregulators.

APPENDIX A

Local Control Register Quick Reference

APPENDIX A
Local Control Register Quick Reference

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

Offset (Hex)	Register	Mode	Default	Primary Function	Ref Para
0000	BOARD CONTROL (BCR)	RW	0000 4060h	Board Control Register (BCR)	3.2
0004	INTERRUPT CONTROL	RW	0000 0008h	Interrupt conditions and flags	3.7
0008	INPUT DATA BUFFER	RO	000X XXXXh	Analog input data buffer	3.5.1.1
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control	3.5.2
0010	RATE-A GENERATOR	RW	0001 07D0h	Rate-A generator frequency selection	3.4.4.1
0014	RATE-B GENERATOR	RW	0001 EA60h	Rate-B generator frequency selection	3.4.4.1
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer	3.5.2
001C	BURST SIZE	R/W	0000 0001h	Number of sample clocks in a triggered burst.	3.10.1
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Triggering sources.	3.4.3
0024	ACTIVE CHANNEL ASSIGNMENT	R/W	0000 0100h	Specific first and last active channels.	3.5.3.2
0028	BOARD CONFIGURATION	RO	000X XXXXh	Firmware revision and option straps.	3.9
002C	Autocal Values *	R/W	0000 080Xh	Autocal value readback.	---
0030	(Reserved)	R/W	0000 0000h	---	---
0034	AUXILIARY SYNC I/O CONTROL	R/W	0000 0000h	Controls auxiliary sync I/O port	3.4.6
0038	SCAN MARKER UPPER WORD	R/W	0000 0000h	Packed-data scan marker D[31..16].	3.5.1.2
003C	SCAN MARKER LOWER WORD	R/W	0000 0000h	Packed-data scan marker D[15..0]..	3.5.1.2
0040-00FC	(Reserved)	---	---	---	---
0100-01FC	LOW-LATENCY DATA	RO	0000 XXXXh	Low Latency data (Paragraph 3.14)	3.11

R/W = Read/Write, RO = Read-Only. * Maintenance register; shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

Bit	Mode	Designation	Def	Description	Ref Para
D00-D02	R/W	AIM[2..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	UNIPOLAR INPUTS	0	Selects unipolar inputs when HIGH, bipolar inputs when LOW.	3.4.1
D04-D05	R/W	RANGE[1..0]	2	Analog input range. Defaults to the highest bipolar range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.	3.5.1.3
D07	R/W	16 BIT DATA	0	Data width is 16 bits if this bit is HIGH, or if data packing is selected. Otherwise, data width is 18 bits.	3.5.1.1
D08-D09	R/W	DIFFERENTIAL PROCESSING	0	Selects standard or differential processing.	3.5.5
D10	RO	DATA ON HOLD	0	Low-Latency access status flag.	3.11
D11	R/W	DISABLE SCAN MARKER	0	Disables the scan marker in data packing mode.	3.5.1.2
D12	R/W	*BURST TRIGGER	0	Triggers a single acquisition burst when BCR Input Trigger is selected in the Scan and Sync Control Register.	3.4.5.1 3.10.1
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.6
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	3.5.2
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.5.1.2
D19	R/W	*INPUT CLOCK	0	Initiates a single sample of all active channels when BCR Input Clock is selected in the Scan and Sync Control Register.	3.4.5.2
D20-D31	RO	(Reserved)	0	---	---

R/W = Read/Write, RO = Read-Only. *Clears automatically when operation is completed

Table 3.4-1. Input Voltage Range Selection

	HIGH Range Set Installed		LOW Range Set Installed Set	
Range[1:0]	**Bipolar Inputs 'Unipolar' = Low**	**Unipolar Inputs 'Unipolar' = High**	**Bipolar Inputs 'Unipolar' = Low**	**Unipolar Inputs 'Unipolar' = High**
0				
1	±5 Volts	0/+10 Volts	±2.5 Volts	0/+5 Volts
2	±10 Volts		±5 Volts	0/+10 Volts
3				

(Shaded areas are reserved.)

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

Bit	Mode	Designation	Def	Description	Ref Para
D00-D02	R/W	ACTIVE CHANNELS	5	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 32 channels (00-31); Default value 6 => 64 channels (00-63) 7 => Channel group assignment * Channel selected by the Single-Channel Select field below.	3.5.3.2
D03-D04	R/W	SAMPLE CLOCK SOURCE	0	Selects the analog input sample clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External CLK I/O input line (Selects ***Clock-Target*** mode) 3 => BCR Input Clock control bit.	3.4.5.2 3.10.2
D05-D06	R/W	BURST TRIGGER SOURCE	0	Selects the analog input burst trigger source: 0 => Internal Rate-B generator output 1 => Internal Rate-A generator output 2 => External TRIG I/O pin (Selects ***Trigger-Target*** mode) 3 => BCR Burst Trigger control bit.	3.4.5.1 3.10.1
D07	RO	BURST BUSY	0	Indicates a burst in progress.	3.10.1
D08	R/W	ENABLE BURST	0	When HIGH, enables triggered bursts.	3.10
D09	R/W	INPUT 63 AS CLOCK IO	0	When High, configures the INP63 pin in the system I/O connector as a bidirectional TTL CLK I/O pin.	3.4.5.2
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.	3.10.1
D11	R/W	ENABLE CLOCKING	0	Enables the currently selected clocking process.	3.4.5.2
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.	3.5.3.2
D18	R/W	ENABLE CLOCK OUT	0	Configures the CLK I/O pin as an output if external clocking is not selected.	3.4.5.2
D19	R/W	ENABLE TRIGGER OUT	0	Configures the TRIG I/O pin as an output if external triggering is not selected.	3.4.5.1
D20-D31	RO	(Reserved)	---	---	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 07D0 (Rate-A), 0001 EA60h (Rate-B)**

Data Bit	Mode*	Designation	Default	Description
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		Fgen Frequency (60 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
80	50	750,000
81	51	740,741
---	---	Fgen (Hz) = 60,000,000 / Nrate

* ±0.015 percent.

Table 3.4.6-1. Auxiliary Sync I/O Connections

Signal	Pin
DIGITAL RETURN	1
AUX CLOCK	2
DIGIAL RETURN	3
AUX TRIGGER	4
DIGITAL RETURN	5
(Reserved)	6

Table 3.4.6-2. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Bit	Mode	Designation	Def	Description
D00-D01	R/W	AUX-CLOCK CONTROL	0	AUX-CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-D03	R/W	AUX-TRIGGER CONTROL	0	AUX-TRIGGER I/O Control Mode 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D04-D07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 90ns and output pulse width is 140ns. When HIGH, input debounce time is 400ns, and output pulse width is 500ns.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

Table 3.5-1. Input Data Buffer; Nonpacked 18-Bit Data

Offset: 0008h **Default: N/A**

Data Bit	Mode *	Designation	Description
D00	RO	DATA00	Least significant data bit
D01-D16	RO	DATA01 - DATA16	Intermediate data bits
D17	RO	DATA17	Most significant data bit
D18	RO	FIRST CHANNEL TAG	Accompanies the first channel in any active channel group (3.5.3.2).
D19-D31	RO	(Reserved)	Inactive

* RO indicates read-only access. Write-data is ignored.

Table 3.5-2. Data Packing

	Buffer Data Field *					
	ENABLE DATA PACKING = 0 DISABLE SCAN MARKER = X		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 0		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 1	
Buffer Lword Order	**D18** (D[31..19] = all zero)	**D[17..0]**	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**
00	1	1st Chan Data	Upper Marker	Lower Marker	2nd Chan Data	1st Chan Data
01	0	2nd Chan Data	2nd Chan Data	1st Chan Data	4th Chan Data	3rd Chan Data
02	0	3rd Chan Data	4th Chan Data	3rd Chan Data	6th Chan Data	5th Chan Data
03	0	4th Chan Data	6th Chan Data	5th Chan Data	8th Chan Data	7th Chan Data
---	---	---	---	---	---	---

* "1st Chan Data" is Chan-00 data unless 'Channel Group Assignment' is selected in the Scan and Sync control register.

Table 3.5-3. Bipolar Input Data Coding; 18-Bit Data

Analog Input Level	Digital Value (Hex)	
	Offset Binary	**Two's Complement**
Positive Full Scale minus 1 LSB	0003 FFFF	0001 7FFF
Zero	0002 0000	0000 0000
Zero minus 1 LSB	0001 FFFF	0003 FFFF
Negative Full Scale	0000 0000	0002 0000

Table 3.5-4. Input Data Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

Data Bit	Mode*	Designation	Def	Description
D00-D17	R/W	THRESHOLD VALUE	3_FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D20-D31	RO	(Reserved)	0	Inactive

*Clears automatically within 200ns of being set

Table 3.5-5. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

Data Bit	Mode*	Designation	Def	Description
D00-D18	RO	BUFFER SIZE	0_0000h	Number of values in the input buffer
D19-D31	RO	(Reserved)	0	Inactive

Table 3.5-6. Analog Input Function Selection

AIM[2:0]	Function or Mode
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Table 3.5-7. Active Channel Assignment

Offset: 0000 0024h **Default: 0000 0100h**

Data Bit	Mode	Designation	Default	Description
D00-D07	R/W	FIRST CHANNEL SELECT	0	First (lowest-numbered) active channel
D08-D15	R/W	LAST CHANNEL SELECT	1	Last (highest-numbered) active channel
D16-D31	RO	(Reserved)	0	Inactive. Returns all-zero.

Table 3.5-8. Differential Processing Modes

BCR D08,09	Designation	Processing Function
0	SINGLE ENDED	Default operating mode. Processing of input data is limited to gain and offset error correction.
1	PSEUDO-DIFFERENTIAL	Channel-00 is the input LO reference for all other channels.
2	FULL DIFFERENTIAL	Each odd-numbered channel is the LO reference for each even-numbered HI channel. I.e.: Channels 00 and 01 become Channel-00 HI and Channel-00 LO, respectively.
3	(Reserved)	

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

Data Bit	Mode	Designation	Def	Value	Interrupt Event
D00-02	R/W	IRQ0 A0,1,2	0	0	Initialization completed.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4	Triggered burst initiated (BURST BUSY => HI)
				5	Triggered burst completed (BURST BUSY => LO)
				6-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	Input buffer overflow or underflow
				4-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Reserved)	0	---	---

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.9-1. Production Configuration Register

Offset: 0000 0028h **Default: 000X XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12	High if the board contains only 32 input channels.
D13-D14	Master Clock Frequency Fclk: 0 => 60.000 MHz 1-3 => (Reserved)
D15-D16	Input Bandwidth (±20%): 0 => 200kHz 1 => 70kHz 2-3 => (Reserved)
D17	I/O Pin-B33 function: 0 => Pin B33 = Input Return 1 => Pin B33 = CLK I/O
D18	0 => High range set; 1 => Low range set.
D19	Custom Feature:
D20-D31	(Reserved)

APPENDIX B

Migration from PMC66-16AI64SSC

Appendix B

Migration from PMC66-16AI64SSC

Operation of the PMC66-18AI64SSC750K is very similar to that of the PMC66-16AI64SSC. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 provides a brief comparison of PMC66-16AI64SSC and PMC66-18AI64SSC750K features. The two products differ principally with respect to the conversion resolution, maximum sample rate, and increased local clock frequency.

Table B.1. PMC-16AI64SSC, PMC66-18AI64SSC750K Features Comparison

Feature	PMC66-16AI64SSC	PMC66-18AI64SSC750K
Number of Channels	64	64
Conversion Resolution	**16 Bits**	**18 Bits**
Maximum sample rate	**200KSPS**	**750KSPS**
Local Clock	**50 MHz**	**60 MHz**
Data Buffer	256K-Sample FIFO (512K with data packing)	256K-Sample FIFO (512K with 16-bit data packing)
PCI Interface	PCI 2.3; D32; 33MHz	PCI 2.3; D32; 33MHz/66MHz

B.2. Migration Issues

- Separate I/O lines are provided for external clocking and burst triggering functions.
- In general, the term "Sync" has been replaced with "Trig" or "Trigger".
- Section 3 was reorganized somewhat in order to improve grouping of associated subjects.
- The data width has increased from 16 bits to 18, and the max sample rate to 750KSPS.

Section 2:

Added a CLK I/O pin. The context of the TRIG I/O (previously "SYNC I/O) is now dedicated exclusively to burst triggering.

Table 3.2-1 (BCR):

Deleted the "Enable External Triggering" control bit. This function has been moved to the Scan and Sync control register.
Added "Input Clock", "Input Trigger" and "16 Bit Data" control bits.

Table 3.4-2 (Scan and Sync Control Register):

Added a "Burst Trigger Source" control field.
Added "Enable Trigger Out" and "Enable Clock Out" control bits.
Deleted the "Burst On Sync" control field (See 3.4.5.1).

Table 3.9-1 (Board Configuration Register):

Revised to reflect 18AI64SSC configurations and 20-bit local bus.

Revision History:

05-29-2013: Origination.

11-23-2013:

Para 3.4.5.2:	Added references to two new control bits in the scan/sync control register.
Para 3.5.5:	Corrected table reference.
Para 3.5.5.4:	Elaborated upon the necessary data adjustments in differential modes.
Table 3.4-1:	Revised table.
Table 3.4.-2:	Added control bit D09 as a context switch for the Channel-63 input pin as CLK I/O. Added control bit D11 to enable clocking.
Table 3.9-1:	Shifted option codes down four bits to accommodate 20-bit local bus.

12-22-2013:

Table 3.9-1: Added 70kHz filter option.

01-11-2014:

Table 2.2-1, 3.4-2; Para 3.4.6. 3.5.1.2: Updated table and illustration references.

03-18-2014:

Tables 3.4.1, 3.9.1: Added dual range-sets, High and Low.
Paragraph 3.12: New paragraph.

09-11-2014:

Table 3.5.4. Updated reserved bit-range.

01-19-2015:

Paragraph 2.5.2: Updated connector reference.
Removed 'Preliminary' notices.

10-15-2015:

Paragraphs 3.4.4.1, 3.4.5.2: Added note regarding internal and external clock frequency ranges.

10-15-2015:

Table 3.9-1: Revised input bandwidth.

Additional copies of this manual or other General Standards Co. literature may be obtained from:

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