General Standards Corporation

High Performance Bus Interface Solutions

Rev: 122207

PCI-24DSI32

24-BIT, 32-CHANNEL DELTA-SIGMA, 200 KSPS ANALOG INPUT PCI BOARD

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PCI-24DSI32 board provides 24-bit analog input capability for the PCI bus at sample rates up to 200 KSPS per channel. In addition to providing 32 analog input channels, this product supports multiboard clocking and synchronization. The board is functionally and mechanically compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with minimal (200 LFPM) air cooling. Specific details pertaining to physical characteristics and performance are contained in the PCI-24DSI32 product specification.

The board is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made at the panel bracket through a 100-Pin dual-ribbon cable connector. Figure 1.1 represents the physical configuration of the board.

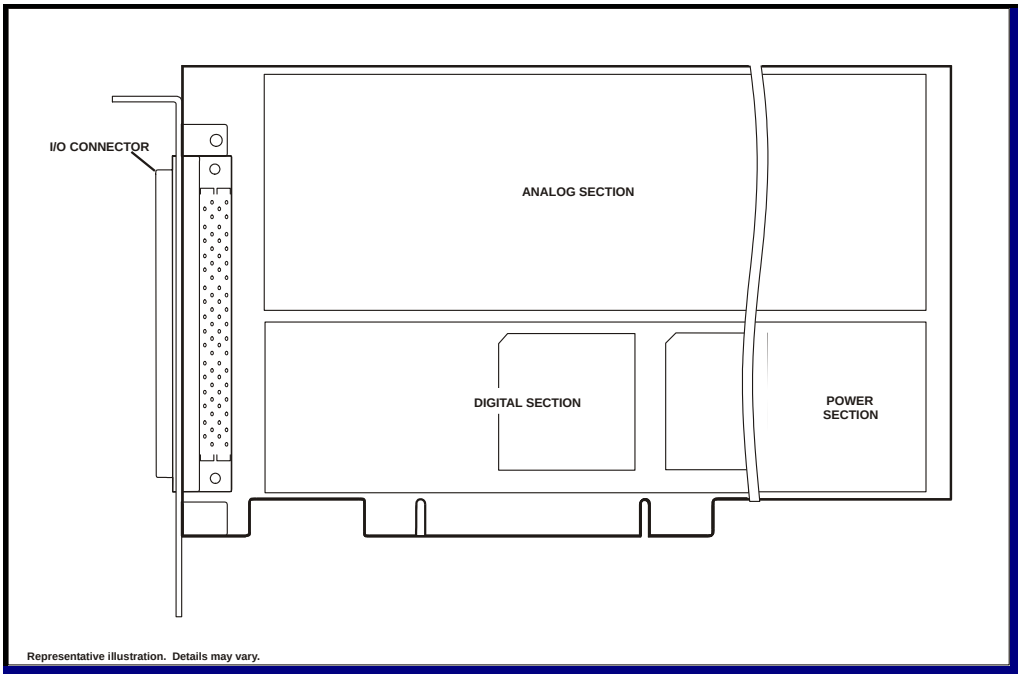

Figure 1.1. Physical Configuration

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1.2). Inputs are organized into four channel groups, three of which can be designated as either active or inactive independently of the other groups. Each input channel consists of configuration switches for selftest and autocalibration operations, as well as range-scaling and analog image filter networks. Each even-odd channel pair also contains a dual delta-sigma A/D converter (ADC) that provides two separate but synchronized conversion channels. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming of the input channels is performed by applying correction values obtained during autocalibration.

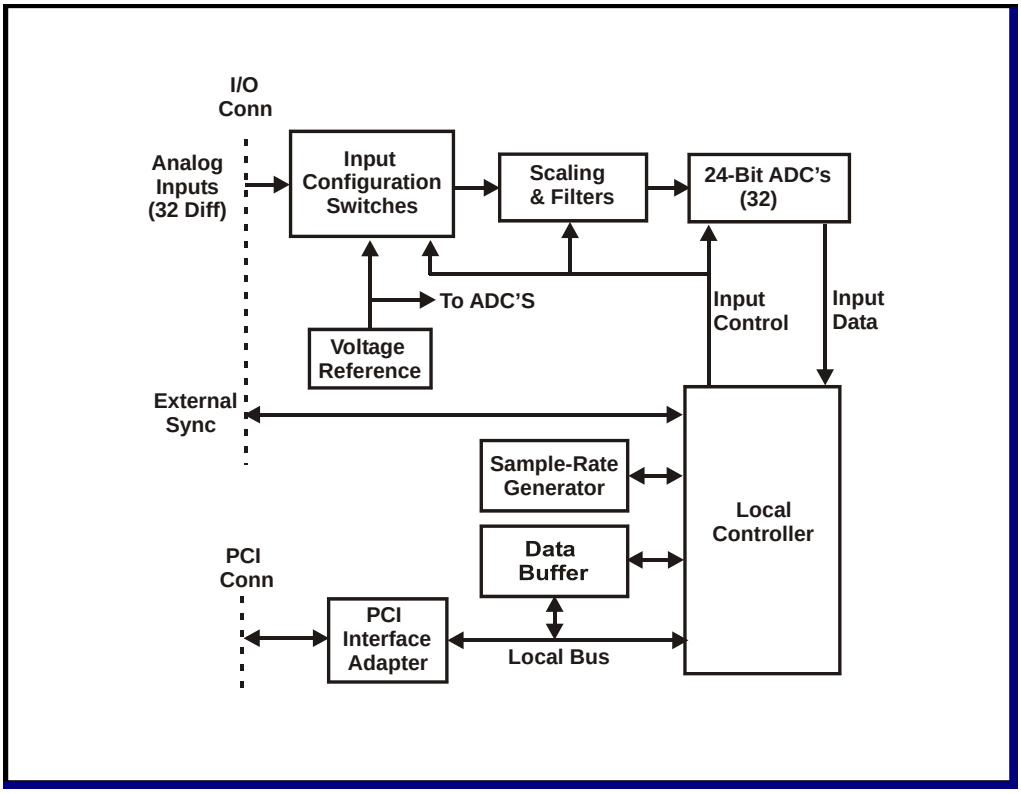

Figure 1.2. Functional Organization

An internal sample-rate clock generator is adjustable from 20 MHz to 55 MHz, and is divided down within the local controller to provide sample rates from 2.0 KSPS to 200 KSPS. Input bandwidth varies from 1000 Hz to 80 kHz, depending upon the selected sample rate, and extends down to DC. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample FIFO data buffer.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host system are adequately discharged to ground.

Before removing the board from the protective shipping envelope, select an empty PCI slot in the host computer and, if a blank panel bracket is located in the slot position, remove the bracket. Then remove the board from the shipping envelope and position the board with the panel bracket oriented toward the expansion panel opening. Align the board's PCI edge-connector with the mating connector on the motherboard, and carefully press the board into position. Verify that the PCI connector has mated completely, and that the panel bracket is seated against the fastener bracket above the panel opening. To complete the installation, secure the panel bracket with an appropriate machine or panhead screw; do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

The system I/O connector is designed to mate with a 100-pin dual-ribbon connector, equivalent to AMP #749621-9. This insulation displacement (IDC) cable connector accepts two 50-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2.2 and in Figure 2.2.2.

Table 2.2.2. System Connector Pin Assignments

ROW-A	
PIN	FUNCTION
1	CLOCK INPUT LO
2	CLOCK INPUT HI
3	SYNC INPUT LO
4	SYNC INPUT HI
5	DIGITAL RETURN
6	DIGITAL RETURN
7	CLOCK OUTPUT LO
8	CLOCK OUTPUT HI
9	SYNC OUTPUT LO
10	SYNC OUTPUT HI
11	INPUT RETURN
12	INPUT RETURN
13	VTEST RETURN
14	VTEST OUTPUT
15	INPUT RETURN
16	INPUT RETURN
17	INPUT CH 00 LO
18	INPUT CH 00 HI
19	INPUT CH 01 LO
20	INPUT CH 01 HI
21	INPUT CH 02 LO
22	INPUT CH 02 HI
23	INPUT CH 03 LO
24	INPUT CH 03 HI
25	INPUT CH 04 LO
26	INPUT CH 04 HI
27	INPUT CH 05 LO
28	INPUT CH 05 HI
29	INPUT CH 06 LO
30	INPUT CH 06 HI
31	INPUT CH 07 LO
32	INPUT CH 07 HI
33	INPUT CH 08 LO
34	INPUT CH 08 HI
35	INPUT CH 09 LO
36	INPUT CH 09 HI
37	INPUT CH 10 LO
38	INPUT CH 10 HI
39	INPUT CH 11 LO
40	INPUT CH 11 HI
41	INPUT CH 12 LO
42	INPUT CH 12 HI
43	INPUT CH 13 LO
44	INPUT CH 13 HI
45	INPUT CH 14 LO
46	INPUT CH 14 HI
47	INPUT CH 15 LO
48	INPUT CH 15 HI
49	INPUT RETURN
50	INPUT RETURN

ROW-B	
PIN	FUNCTION
1	AUX LVDS INP LO
2	AUX LVDS INP HI
3	DIGITAL RETURN
4	DIGITAL RETURN
5	AUX LVDS OUT LO
6	AUX LVDS OUT HI
7	INPUT RETURN
8	INPUT RETURN
9	INPUT CH 16 LO
10	INPUT CH 16 HI
11	INPUT CH 17 LO
12	INPUT CH 17 HI
13	INPUT CH 18 LO
14	INPUT CH 18 HI
15	INPUT RETURN
16	INPUT RETURN
17	INPUT CH 19 LO
18	INPUT CH 19 HI
19	INPUT CH 20 LO
20	INPUT CH 20 HI
21	INPUT CH 21 LO
22	INPUT CH 21 HI
23	INPUT RETURN
24	INPUT RETURN
25	INPUT CH 22 LO
26	INPUT CH 22 HI
27	INPUT CH 23 LO
28	INPUT CH 23 HI
29	INPUT CH 24 LO
30	INPUT CH 24 HI
31	INPUT RETURN
32	INPUT RETURN
33	INPUT CH 25 LO
34	INPUT CH 25 HI
35	INPUT CH 26 LO
36	INPUT CH 26 HI
37	INPUT CH 27 LO
38	INPUT CH 27 HI
39	INPUT RETURN
40	INPUT RETURN
41	INPUT CH 28 LO
42	INPUT CH 28 HI
43	INPUT CH 29 LO
44	INPUT CH 29 HI
45	INPUT CH 30 LO
46	INPUT CH 30 HI
47	INPUT CH 31 LO
48	INPUT CH 31 HI
49	INPUT RETURN
50	INPUT RETURN

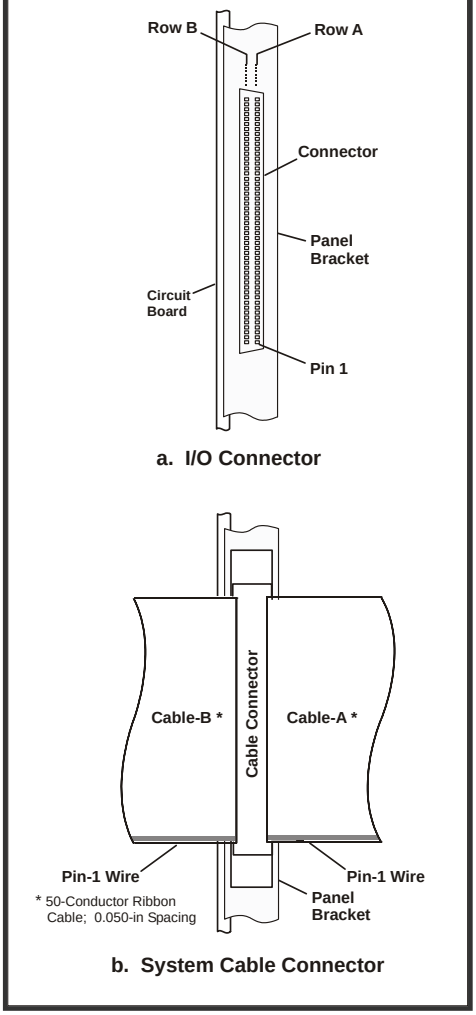

Figure 2.2.2: System I/O Connections

2.3 Analog Input Configuration

The analog inputs are configured as 32 differential input pairs. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs. Although the input configuration is differential, single-ended signal sources can be accommodated as described in Paragraph 2.3.2.

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm** which, for optimum performance, must not exceed the maximum value indicated in the product specification.

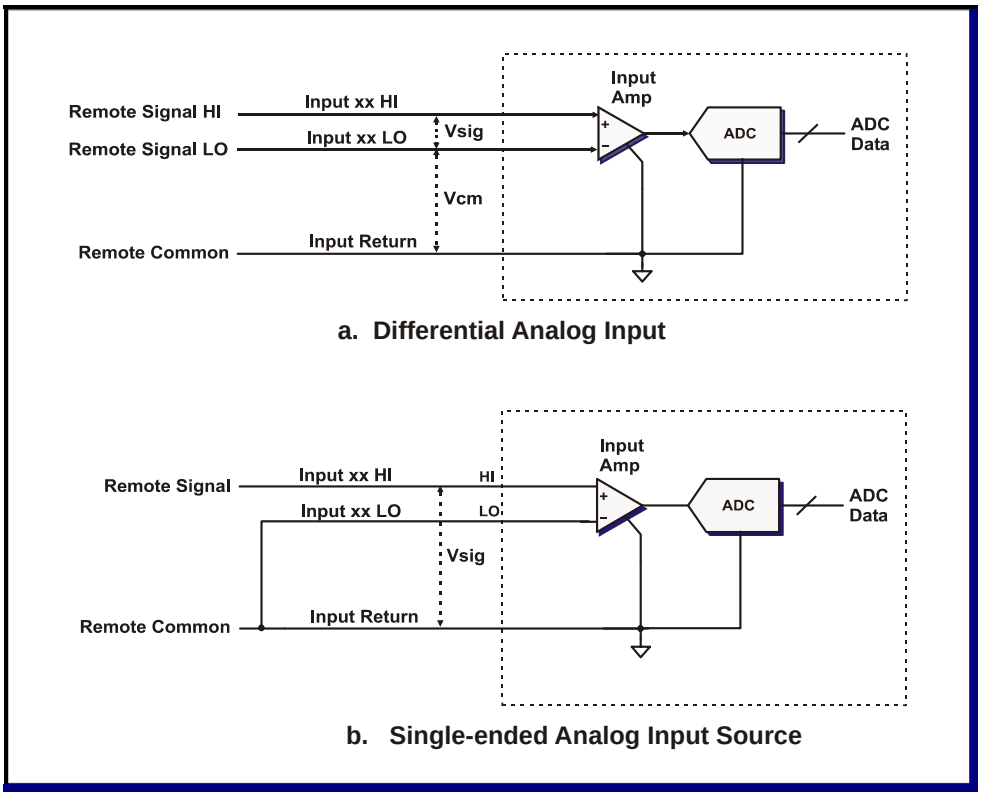

Figure 2.3.1. Input Configurations

2.3.2 Single-Ended Input Sources

Single-ended signal sources can be accommodated as shown in Figure 2.3.1b, with the signal line connected to INP CHAN XX HI, and the associated INP CHAN XX LO input connected to INPUT RETURN at the source. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote signal return and INPUT RETURN, a low impedance between the two returns can cause excessive current to flow, which in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.4.1 Interboard Connections

Figure 2.4.1 illustrates how multiple PCI-24DSI32 boards can be daisy-chained together in an initiator-target sequence to provide common clocking between boards. The CLOCK OUTPUT HI/LO lines from an initiator are connected to the CLOCK INPUT HI/LO lines on a target board, and the SYNC output and input pairs are connected similarly. Each target board can serve as an initiator for another target board, and multiple boards can be daisy-chained together for synchronous operation.

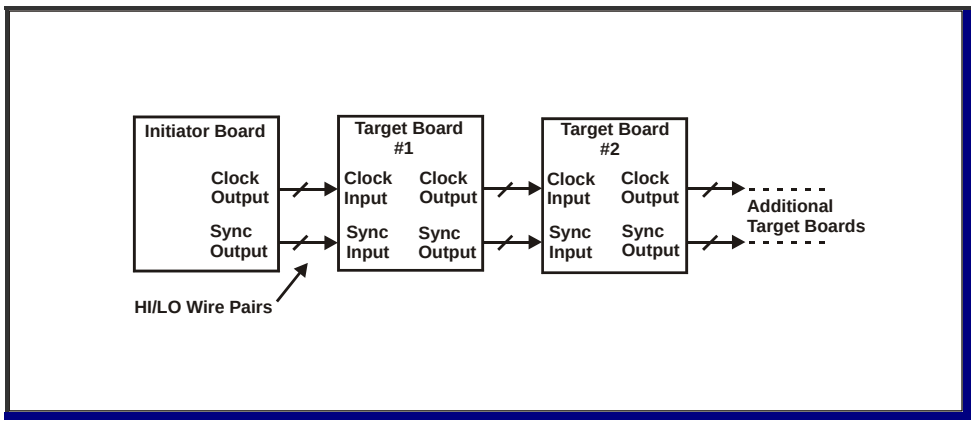

Figure 2.4.1. Multiboard Clock/Sync Connections

By using an external LVDS distribution module, multiple boards can be interconnected in a 'star' configuration to eliminate the clock and sync propagation delay introduced by each board in a daisy chain configuration.

The clock output signal is generated internally on an initiator board, or is a duplicate of the clock input signal on a target board. Similarly, the sync output is the software-generated sync signal on an initiator board, or a duplicate of the sync input signal on a target board.

Note: External clock and sync inputs can be provided from external sources other than an initiator board. External clock and sync sources must be LVDS-compatible.

Because each board provides active differential outputs for the next board in the chain, the number of boards in the chain is limited only if the propagation delay of approximately 10 nanoseconds introduced by each board becomes significant over multiple boards. Cable-length between boards should be less than one meter for general-purpose ribbon cable, while high-quality 100-Ohm cable can extend the length to 10 meters or more.

Application software controls the designation of each board as an initiator or a target, and also selects the channels on each board that will respond to the daisy-chained clock. Although only software-designated channels respond to the daisy-chained clock, all channels on all target boards respond to the sync signal.

2.4.2 Multiboard Synchronization

Boards that are daisy-chained together for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The sequence has a duration of approximately 100 milliseconds, after which all synchronized channels operating from a common clock will sample their inputs simultaneously.

The SYNC I/O line can also be used to reset (clear) the data buffers on target boards.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum adjustment interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Verification and Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This procedure describes the adjustment of the internal reference. For applications in which the system must not be powered down, the adjustment can be performed while the board is installed in an operating system.

2.6.1 Equipment Required

Table 2.6.1 lists the equipment requirements for calibrating the PCI-24DSI32 board. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Adjustment Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with PCI expansion slot	---	---
Cable connector, with test leads. (Not required if calibration test points are made permanently available at a system connection point)	AMP	749621-9

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimmer that is accessible at the top of the board, as shown in Figure 2.6.2.

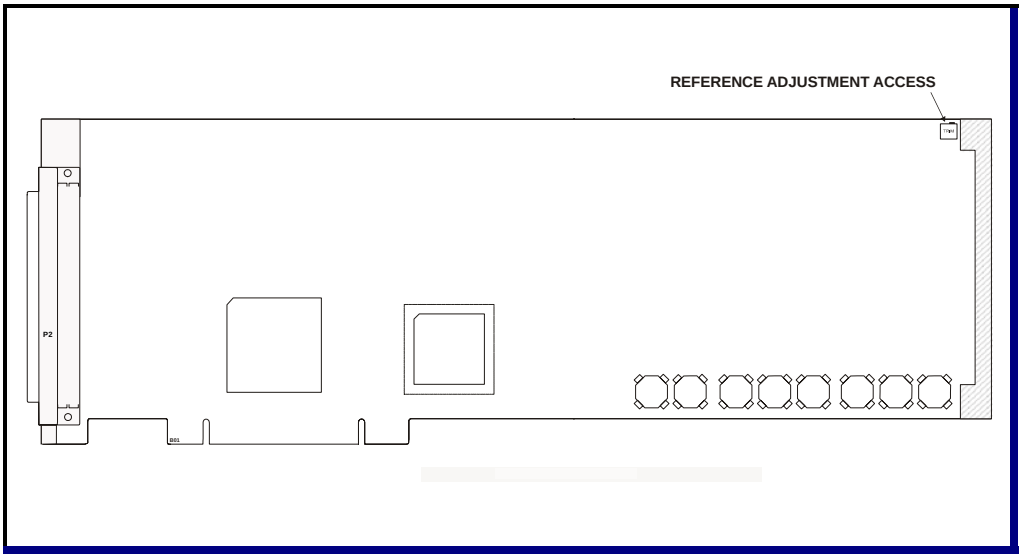

Figure 2.6.2. Reference Adjustment Access

This procedure assumes that the board is installed in an operating system, and that the ±10V input range is selected.

1. Connect the digital multimeter between the VTEST OUTPUT (+) and VTEST RETURN (-) pins in the system I/O connector. Refer to Table 2.2.2 for pin assignments.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding.

3. Select the ±10V input range.

4. Verify that the digital multimeter indication is +9.9000 VDC ±0.0009 VDC. If the indication is not within this range, adjust the REFERENCE ADJUSTMENT trimmer until the digital multimeter indication is within the specified range.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PCI-24DSI32 board is compatible with the PCI Local Bus specification and supports "plug-n-play" autoconfiguration at the time of power-up. That is, the host can obtain the amount of I/O space required by the board, and return the configuration base address into the PCI Configuration Register on this board. The PCI interface is controlled by a PLX™ PCI-9080 PCI adapter. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. Reserved bits in each register are ignored during write operations, and are forced LOW during read operations. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written as LOW.

Table 3.1. Control and Data Registers

LOCAL ADDR	ACCESS MODE	REGISTER	DEFAULT	DESCRIPTION
00	R/W	**Board Control (BCR)**	0000 383Ch *	Board Control Register (BCR)
04	R/W	**Nref PLL Control**	0000 01F4h	PLL reference oscillator control integer. (PLL configuration only)
08	R/W	**Nvco PLL Control (Legacy Nrate)**	0000 01F4h	PLL vco control integer. (Nrate for the legacy rate generator)
0C	RO	**Rate Assignments**	0000 0000h ****	ADC Clock source; Group disables.
10	R/W	**Rate Divisor**	0000 0005h	Sample rate divisor.
14	RO	**(Reserved)**	0000 0000h	---
18	R/W	**PLL Reference Freq**	XXXX XXXXh	PLL reference frequency indicator
1C	RO	(Reserved)	0000 0000h	---
20	R/W	**Buffer Control**	0003 FFFEh **	Input buffer control and status
24	RO	**Board Configuration**	00XX XXXXh	Installed firmware and hardware options
28	RO	**Buffer Size**	0XXX XXXXh	Number of ADC values in the input buffer.
2C	RO	Autocal Values ***	---	---
30	RO (DMA)	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag
34-7C	--	(Reserved)	---	---

* Changes to 0000 783Ch when the input buffer fills.
** Changes to 0103 FFFEh when the buffer fills.
*** Maintenance register. Shown for reference only.
**** May be 0000 0190h in earlier firmware revisions.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and input range selections, and consists of 32 control bits and status flags (Table 3.2). Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.
D01	R/W	AIM1	
D02	R/W	RANGE0	Analog input range selection. Defaults to ±10V range.
D03	R/W	RANGE1	
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults HIGH to Initiator mode.
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.
D07	R/W	*AUTOCAL	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.
D09	R/W	INTERRUPT A1	
D10	R/W	INTERRUPT A2	
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D12	RO	AUTOCAL PASS	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.
D13	RO	CHANNELS READY	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.
D15	R/W	*INITIALIZE	Initializes the board when asserted. Sets all defaults.
D16	R/W	SYNCHRONIZE SCAN	Selects synchronous sampling mode.
D17	R/W	CLEAR BUFFER ON SYNC	When this bit is HIGH, the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.
D18	R/W	RATE GEN EXT CLOCK OUT (Initiator Mode only)	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock. (If Group-00 external clocking is selected, the output is driven by the internal rate generator and the Group-00 divisor).
D19	R/W	SELECT LOW IMAGE FILTER	When this bit is HIGH, the low-frequency image filter is selected. When LOW, the high filter is selected.
D20	R/W	(Reserved)	--
D21	R/W	ARM EXTERNAL TRIGGER	Arms the external burst trigger input. (3.12)
D22	R/W	THRESHOLD FLAG OUT	Routes the threshold flag to the AUX LVDS output.
D23-31	RO	(Reserved)	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Changes to 0000 783Ch when the input buffer fills.

3.3 Configuration and Initialization

3.3.1 Board Configuration

Board configuration is initiated by a PCI bus RESET, and should be required only once after the initial application of power. During board configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	5 seconds

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 5 seconds, and produces the following conditions:

- The Initiator mode is selected, External clock output is Channel-00 sample clock,
- The width of the buffer data field is adjusted to 16 bits,
- The internal rate generator is the ADC clock source,
- Internal rate generator frequency is 32.768 MHz,
- Rate divisor(s) are preset to 5,
- Sample rate is 12.8 KSPS; i.e.: 32.768MHz / (512 *5).
- The analog input buffer is reset to empty; buffer threshold equals 0003 FFFEh,
- Analog inputs are configured for ±10 Volt operation,
- All control registers are initialized; all defaults are invoked,
- The local interrupt request is asserted as an initialization-completed event.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[1..0], the effects of which are summarized in Table 3.4. The analog input selection arranges all input channels in differential configuration during normal operation, or invokes one of two selftest modes.

Table 3.4. Analog Input Function Selection

AIM[..0]	FUNCTION OR MODE
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

3.4.1 Selftest Modes

Two selftest modes provide the ability to verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). The +VREF test produces a positive value equal to 99.00 percent of the selected input range (e.g. +9.900 Volts for the ±10 Volt range) from all input channels, and the ZERO test should produce a value of 0.000 Volts. The accuracy of selftest measurements should correspond to the product accuracy specification.

NOTE: For maximum test accuracy, the internal reference voltage must be allowed to settle completely when the test mode is changed. After selecting either of these test modes, insert the indicated minimum settling delay before acquiring test values:

ZERO test: 100 milliseconds,
+VREF test: 3 seconds.

3.4.2 Input Range Selection

Any one of three input voltage ranges can be selected for all channels. RANGE[1..0] control bits in the BCR select the input range, as shown in Table 3.4.3.

Table 3.4.3. Analog Input Range Selection

RANGE[1..0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±2.5 Volts
2	±5 Volts
3	±10 Volts

3.4.3 Settling Delays and the Channels Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate intervals indicated:

5 Seconds:	Board initialization (3.3),
1 us:	Buffer reset, if not in synchronous-scanning mode (3.5.3.2),
10 us-5 ms:	Buffer reset, if in synchronous-scanning mode (3.5.3.2),
100 ms:	Sample rate change ; i.e.: Nrate, Ndiv, Rate assignments (3.6).
1-100 ms:	ADC synchronization (3.6.5 and 3.10),
1-100 ms:	Synchronous-scan initiation (3.10),

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO data buffer, which has a capacity of 256K (262,144) data values. Data accumulates in the buffer until extracted by the PCI bus from a single register location, indicated as INPUT DATA BUFFER in Table 3.1. Reading an empty buffer returns an indeterminate value.

3.5.2 Data Organization

Each value in the data buffer consists of a 5-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the buffer control register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

SELECTED DATA WIDTH	RESERVED (Zero)	CHANNEL TAG	ZERO-PAD	CHANNEL DATA VALUE
16 Bits	D[31..29]	D[28..24]	D[23..16]	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

3.5.2.1 Channel Tags

If the input channels are not scan-synchronized (Paragraph 3.10), the order in which channel data accumulates in the buffer is not generally predictable. Therefore, a channel tag that identifies each input channel is attached to associated data values in the buffer.

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3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +5.000 Volts for the ±5V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3) contains the threshold value for the buffer status flag, and also provides control bits for clearing the buffer and for disabling the buffer input.

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold (duplicated in the BCR)
D[18]	R/W	DISABLE BUFFER INPUT	Disables ADC inputs to the buffer
D[19]	R/W	CLEAR BUFFER **	Clears (empties) the buffer
D[21..20]	R/W	DATA WIDTH	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23..22]	RO	(Reserved)	---
D[24]	R/W	BUFFER OVERFLOW ***	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW ***	Reports buffer underflow (Read on empty)
D[31..22]	RO	(Reserved)	---

* Changes to 0103 FFFEh when the buffer fills. ** Clears automatically. *** Clear by writing LOW, or by board reset.

NOTE: Since delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Disable' controls.

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer can be used to control the BUFFER THRESHOLD FLAG status bit, which can be selected as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

NOTE: Effective in firmware revision 0502 and subsequent 05XX revisions, the THRESHOLD FLAG OUT control bit is active in the BCR. When this bit is set HIGH, the threshold flag is routed to the AUX LVDS OUT output in the system I/O connector.

3.5.3.2 Buffer Clearing and Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer, and holds the buffer in reset until the internal data pipeline clears, approximately 1.0 microsecond. This bit clears automatically.

Asserting the DISABLE BUFFER INPUT control bit disables inputs to the buffer from the ADC input channels, and halts the accumulation of further input data. Input data already present in the buffer when this bit is asserted remains in the buffer.

Note: The buffer also can be cleared by writing a "one" to the SOFTWARE SYNC control bit in the BCR when the CLEAR BUFFER ON SYNC control bit is HIGH. See "Global Buffer Clear" in Paragraph 3.10.

3.5.4 Buffer Size Register

This read-only register contains the number of analog input values currently stored in the input data buffer.

3.5.5 Buffer Underflow and Overflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared by writing LOW directly, or by a board reset.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Sample rate,
b. Phase, or skew,
c. Channel synchronization.

The effective input bandwidth is determined by the sample rate, while phase and synchronization control the relative timing of sampling between multiple channels. Phase and synchronization are considerations in applications that require consistent relative timing of sampling among multiple channels or multiple boards.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

3.6.1 Sample Rate Control

3.6.1.1 Rate Clock Organization

Sample rates are derived either from an adjustable internal rate generator, or from a single external hardware clock, as shown in Figure 3.6.1.1. Input channels are arranged into four groups (Table 3.6.1.1), three of which can be independently designated as either active or inactive. The sample rate for all channel groups is controlled by the following operations:

a. Assignment to the internal rate generator or to the external clock,
b. Rate generator frequency selection,
c. Rate divisor selection.

The number of channels per group is reduced to four channels for 16-channel boards, or to two channels for 8-Channel boards. This scheme ensures that the board is divided into four equal channel groups, regardless of the number of channels present on a board.

3.6.1.2 Rate Generator Assignment

A 4-bit code RATE SOURCE in the Rate Assignments register selects either the internal rate generator or the external sample rate clock as sample rate source. Group selection codes are arranged in the register as shown in Table 3.6.1.2-1, and use the assignment codes listed in Table 3.6.1.2-2. ***The Group-0 assignment selects the sample rate source for all groups***, while Group 1-3 assignments enable or disable the specific channel groups. Disabled groups do not provide data to the input data buffer.

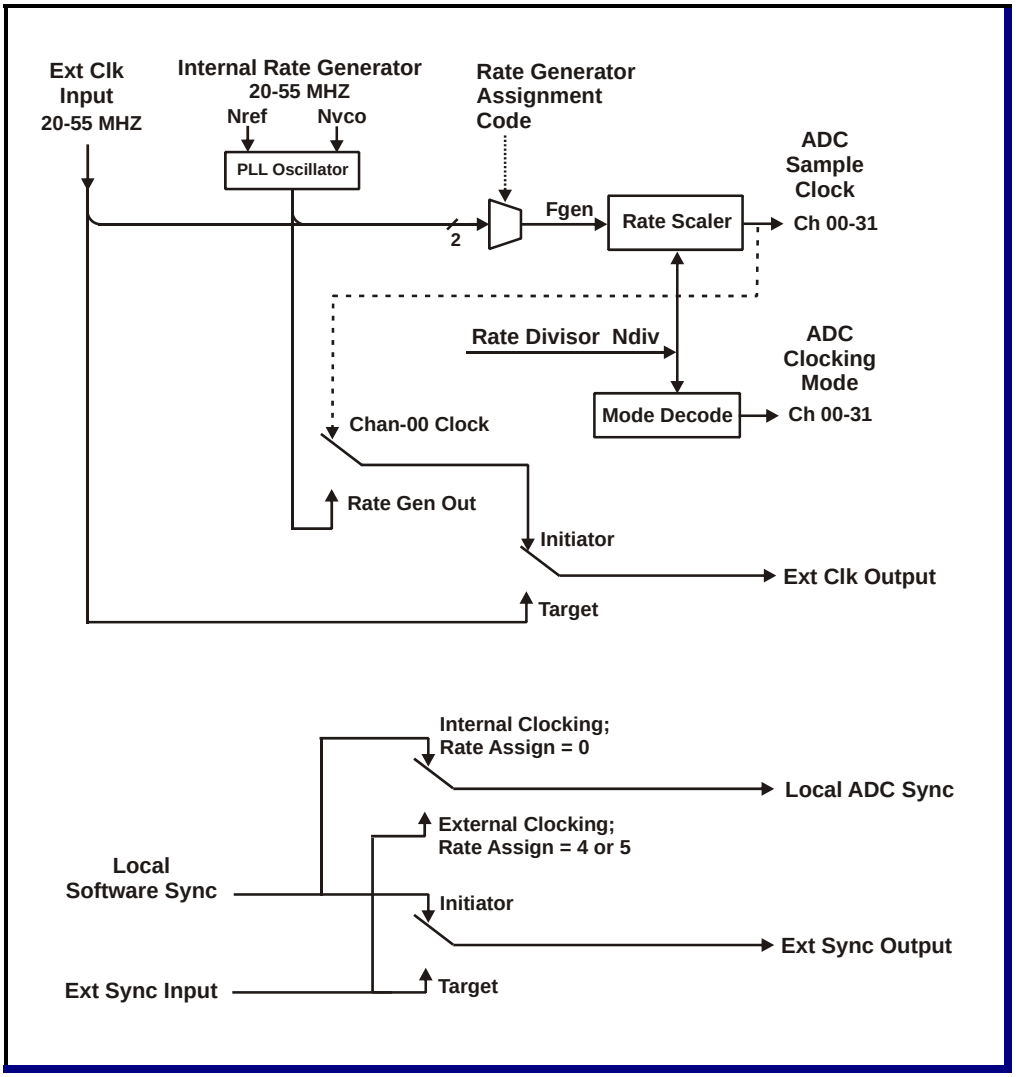

Figure 3.6.1.1. ADC Clock and Sync Organization, 32 Channels

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	32-CHAN BOARD	16-CHAN BOARD	8-CHAN BOARD
0	00-07	00-03	00,01
1	08-15	04-07	02,03
2	16-23	08-11	04,05
3	24-31	12-15	06,07

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	SAMPLE CLOCK SOURCE; GROUP-0 ENABLE/DISABLE	0
D[07..04]	GROUP-1 ENABLE/DISABLE	1
D[11..08]	GROUP-2 ENABLE/DISABLE	2
D[15..12]	GROUP-3 ENABLE/DISABLE	3
D[31..16]	(Reserved)	---

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT *	GROUPS 1-3 ASSIGNMENT
0	Internal Rate Generator	(Unused)
1	(Reserved)	(Unused)
2	(Reserved)	(Unused)
3	(Reserved)	(Unused)
4	External Sample Clock (as rate generator input)	Enabled
5	Direct External Sample Clock (routed directly to ADC)	Enabled
6-7	**Disabled**	**Disabled**
8-15	(Reserved)	(Reserved)

* Applies to all channel groups. Disabling Group-0 disables all groups.

3.6.1.3 Sample Clock Generation

A rate divisor integer **Ndiv** (Table 3.6.1.3) controls a *rate divisor* for the rate generator or external clock input. This integer controls the sample rate for active channels.

Table 3.6.1.3. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0005h**

BIT FIELD:	FUNCTION
D[07..00]	RATE DIVISOR (**Ndiv)**
D[31..08]	(Reserved)

The ADC sample rate **Fsamp** is determined by the rate generator frequency **Fgen** and a rate **DIVISOR** as: (all values in decimal)

$$\mathbf{Fsamp} = \frac{\mathbf{Fgen}}{\mathbf{DIVISOR} * \mathbf{512}}, \qquad \textbf{(3-1)}$$

where **Fsamp** and **Fgen** are in kilohertz, and **DIVISOR** is defined as:

If Ndiv > 0, then DIVISOR = Ndiv,
If Ndiv = 0, then DIVISOR = 0.5, **(3-2)**

where **Ndiv** can have any integer value from zero through 25. **Fgen** has a range of 20 - 55 MHz for the PLL rate generator option, or 25.6 - 51.2 MHz for the legacy option. Refer to Section 3.6.2.

Note: The ADC's operate in one of three different clocking modes, with each mode determined by the required sample rate. In addition to establishing the sample rate division factor, the integer **Ndiv** also controls the ADC clocking mode.

3.6.2 Rate Generator Control

The internal rate generator is a PLL-controlled oscillator locked to a stable reference frequency. Older (Legacy) versions of this product implement a rate generator that could be adjusted with 0.2-percent resolution. The higher-resolution PLL configuration however provides less clock jitter, and consequently produces a more finely detailed spectrum and a lower noise floor. The frequencies of the generator is controlled by the Nref and Nvco control registers listed in Table 3.1. The effect of these registers is determined by the specific PLL or Legacy rate generator option that is present on the board, which is specified as an ordering option.

3.6.2.1 PLL Rate Generator

If the PLL Rate Generator ordering option applies, **Fgen** is generated by an internal phase-locked loop (PLL) oscillator with a frequency range of 20-55 MHz. The frequency **Fgen** of the oscillator is related to a reference frequency **Fref** by integers **Nref** and **Nvco** (Tables 3.6.2.1-1 and 3.6.2.1-2) as:

$$\mathbf{Fgen} = \mathbf{Fref} * \frac{\mathbf{Nvco}}{\mathbf{Nref}}, \qquad \textbf{(3-3)}$$

where **Nvco** and **Nref** each has a maximum range from 30 to 1000, and **Fref** is the frequency of the reference oscillator, which has a standard frequency of **32.768MHz**. Table 3.6.2.1-3 summarizes the sample rate control parameters.

Table 3.6.2.1-1. PLL Nref Register

Offset: 0004h **Default: 0000 01F4h**

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[09..00]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 30-1000.
D[31..27]	R/W	(Reserved)	---

Table 3.6.2.1-2. PLL Nvco Register

Offset: 0008h **Default: 0000 01F4h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[09..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 30-1000.
D[31..27]	R/W	(Reserved)	---

NOTE: Nvco and Nref each has a maximum range from 30 to 1000. For optimum performance, select the *lowest* possible values for Nvco and Nref.

*Because specific applications might require custom values for **Fref**, an approximate measurement of the installed PLL reference oscillator frequency is available in the PLL Reference Freq register listed in Table 3.1. This value is determined at initialization, and equals **Fref** in Hertz with an accuracy of approximately 0.02-percent. It is intended as an indicator only, and is not recommended as a source for the actual **Fref** frequency.*

By combining Equation 3-3 with Equation 3-1 in Section 3.6.1.3:

$$\frac{\textbf{Nvco}}{\textbf{Nref}} = \frac{\textbf{Fsamp * 512 * DIVISOR}}{\textbf{Fref} \text{ (32.768MHz)}} \quad \textbf{(3-4)}$$

Table 3.6.2.1-3. Summary of PLL Sample Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Frequency Range	**Fgen**	20-55 MHz
VCO Factor	**Nvco**	30-1000
Reference Factor	**Nref**	30-1000
Rate Divisor	**Ndiv**	0 - 25
Reference Frequency	**Fref**	Standard value = 32.768MHz

The following example illustrates one of several methods for determining **Nvco** and **Nref**: (Calculating the optimum values for integers **Nvco** and **Nref** can often be simplified by converting all variables, including **Fref**, into products of their prime factors). Other approaches include calculating all possible values of Nvco and Nref, and then sorting the results for the frequency closest to the required frequency.

EXAMPLE: Required sample rate **Fsamp** is **15.360 kHz**. **Fref = 32.768 MHz**:

1. Insert the **Fref** and required **Fsamp** values into Equation 3-3, expressing both in Hertz.

$$\frac{Nvco}{Nref} = \frac{15360 * 512 * DIVISOR}{32768000} .$$

2. Convert **Fref** and **Fsamp** into their prime factors, and simplify the fraction by canceling all factors that are duplicated in the numerator and denominator

$$\frac{Nvco}{Nref} = \frac{(2^{10} * 3 * 5) * (2^{9}) * DIVISOR}{2^{18} * 5^{3}} = \frac{6 * DIVISOR}{25} .$$

3. Select a value for **DIVISOR** that adjusts the value of the fraction to between 0.78 and 1.56 (22MHz to 55MHz) /32.768MHz, with unity being ideal. In this case, use **DIVISOR = 4:**

$$\frac{Nvco}{Nref} = \frac{24}{25}$$

4. Multiply both numerator and denominator by an integer that produces the lowest possible in-range values for **Nvco** and **Nref**, which must be 30 or greater. In this case, multiply by 2:

$$\frac{Nvco}{Nref} = \frac{48}{50} .$$

5. Final Results: **Nvco = 48; Nref = 50; DIVISOR = 4**.

   To confirm the results, first use Equation 3-2 to verify that the rate generator frequency **Fgen** is within the specified range of 20-55 MHz. If **Fgen** is out of range, select another **DIVISOR** value in Step-3:

$$Fgen = Fref * \frac{Nvco}{Nref}$$

$$= 32{,}768{,}000\ Hz * \frac{48}{50} = \underline{31{,}457{,}280\ Hz}.$$

   Finally, use Equation 3-1 to verify the sample rate **Fsamp**:

$$Fsamp = \frac{Fgen}{512 * DIVISOR}$$

$$= \frac{31{,}457{,}280\ Hz}{512 * 4} = \underline{15{,}360\ Hz} .$$

3.6.2.2 Legacy Rate Generator

For boards equipped with the Legacy Rate Generator option, the frequency **Fgen** of an internal rate generator is controlled over a frequency range of 25.6 -51.2 MHz by a variable **Nrate** (Table 3.6.2.2-1) as:

$$\mathbf{Fgen = 25.6 * (1 + Nrate/511),} \qquad \textbf{(3-5)}$$

where **Fgen** is in Megahertz, and **Nrate** has a range from zero through 511.

Table 3.6.2.2-1. Legacy Rate Control Register

Offset: 0008h **Default: 0000 0000h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[16..00]	R/W	RATE CONTROL **(Nrate)**	Frequency control factor; 0-511
D[31..17]	R/W	(Reserved)	---

* Default frequency is 25.6MHz.

Determining the optimum values for **Nrate** and **Ndiv** is usually an iterative process that starts by selecting a maximum value for **DIVISOR** (from **Ndiv**) in Equation 3-1, and then selects successively smaller values of **Ndiv** until valid values for both **Ndiv** and **Nrate** produce a value for **Fsamp** that is as close as possible to the required value.

3.6.3 Direct External Clocking

If the rate assignment selection (Table 3.6.1.2-2) is "Direct External Sample Clock," the signal at the external clock input is routed directly to the ADC's without modification. This configuration eliminates the effect of the **Nrate** control variable, and gives the external clock source direct control of the ADC's.

Although the variable **Nrate** has no effect in this configuration, the clocking mode of the ADC's must be controlled by **Ndiv** as shown in Figure 3.6.1.1. Table 3.6.1.6 shows the relationships between the sample rate **Fsamp**, the external clock frequency, and the required values for **Ndiv**.

Table 3.6.3. Direct External Clocking

Sample Rate Fsamp (KSPS)	External Clock Frequency	Divisor Integer Ndiv
2-50	256 * Fsamp	**2 thru 25**
50-100	128 * Fsamp	**1**
100-200	64 * Fsamp	**0**

3.6.4 Harmonically Locked Channels

Channel groups operating at different frequencies that are exact submultiples of a common frequency perform conversions repetitively relative to a sampling frame, and are *harmonically locked*. An example of this might be four groups operating from the same Fgen source at 25.6 MHz, with Ndiv values of 1, 2, 4 and 8. Using the equation for Fsamp in Paragraph 3.6.1.3, the corresponding sample rates for the four groups would be 50 KSPS, 25 KSPS, 12.5 KSPS and 6.25 KSPS, respectively.

3.6.5 Channel Synchronization

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously while operating from a common clock.

Synchronization is invoked by setting the SOFTWARE SYNC control bit HIGH in the BCR. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition (Paragraph 3.4.4). The CHANNELS READY transition can be selected as a condition for an interrupt request event.

3.6.6 Multiboard Operation

Multiple PCI-24DSI32 boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*. A board is designated as an initiator by setting the INITIATOR control bit HIGH in the BCR, or as a target when the control bit is LOW. *The INITIATOR control bit controls only the source of the external clock and sync outputs, and has no other effect.*

External clock and sync inputs can be provided from LVDS sources other than an initiator board.

3.6.6.1 External Sample Clock

Target boards receive an external clock from the external clock input connection, and duplicate the input clock at the external clock output connection (Figure 3.6.1.1). The external clock input is designated as the clocking source by writing either the "External Sample Clock" or "Direct External Sample Clock" assignment code to the target boards' Rate Assignments register described in Paragraph 3.6.1.2. For calculation of target board sample rates, the external sample clock corresponds to the rate generator frequency **Fgen** described in Section 3.6.1 if "External Sample Clock" is selected, or provides the ADC sample clock directly if "Direct External Sample Clock" is selected.

An ***initiator*** provides an external clock output from either of two sources. If the RATE GEN EXT CLOCK OUT control bit in the BCR is LOW (default), the external clock output is identical to the Group 00 ADC sample clock, which is the internal rate generator output divided by the rate divisor. If the control bit is HIGH, the rate generator unmodified output provides the external clock.

NOTE: The INITIATOR control bit controls only the sources of the external clock and sync output signals, and has no other effect.

Multiple boards can all be configured as initiators and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the LVDS source driver, an LVDS distribution module usually is required in this configuration.

3.6.6.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board.

The SOFTWARE SYNC control bit in the BCR can be used also to clear the buffers on the initiator and target boards simultaneously, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR.

3.7 Autocalibration

Autocalibration is an embedded utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are determined during autocalibration, and are applied to each channel in real-time during data acquisition. The correction values are retained until either: (a) power is removed, (b) a PCI reset occurs, or (c) autocalibration is invoked again. Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration is indicated by the AUTOCAL flag clearing automatically to the LOW state. Clearing of the AUTOCAL control bit is selectable as an interrupt request event.

An autocalibration sequence has a typical duration from 4 to 9 seconds, depending upon the selected sample rate and number of active channels. Read or write access from the PCI bus during autocalibration may disrupt the calibration process, and should be avoided. Either a suitable delay or the "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful.

To ensure full conformance to the product specification, autocalibration should always be invoked after:

(a). Power has been applied to the board,

(b). A PCI reset event has occurred,

(b). The input range, clock source or sampling rate has been altered,

(c). A scan-synchronization sequence has been performed (Section 3.10.

Autocalibration can be invoked at any time, but should not occur while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. For optimum performance, a warmup delay of 15 minutes is recommended.

3.8 Interrupt Control

In order for the board to generate a PCI interrupt on INTA#, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described below in Paragraph 3.8.2.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	(Reserved)
6	(Reserved)
7	(Reserved)

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX™ PCI-9080 reference manual..

3.9 DMA Operation

DMA transfers from the analog input buffer are supported in either of two DMA channels with the board operating as bus master. Table 3.9.1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***exceeds the selected buffer threshold*** *(Table 3.5.3).*

The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The number of values read from the buffer equals the threshold value *plus one*,
(c) The buffer is cleared,
(d) The board is reset,
(e) Autocalibration is executed.

The first occurrence of any of these events terminates the DMA request.

3.10 Scan Synchronization

Although the data sequence for any specific channel in the data buffer represents the actual sampling sequence for that channel, the ordering of multiple channels in the buffer can vary due to the asynchronous nature of the sample clock relative to the board's master clock. These variations in channel order can occur even though all channels are synchronized to a common sample clock.

Variations in the ordering of multiple channels can be eliminated by synchronizing the acquisition of each scan to the board's master clock. This ***scan-synchronization*** can be effective only if all active channels are operating from a common clock source.

Note: References to *channel synchronization* in this manual pertain to the situation in which the sampling of all input channels occurs simultaneously. *Scan-synchronization* refers to the synchronization of discrete data scans to the master clock, to ensure a consistent ordering of data channels in the data buffer.

For synchronized scans, the channel sequence for each scan in the buffer is ordered from lowest to highest. All samples in each scan represent the same sample event, and are arranged beginning with the lowest active channel and proceeding upward through the highest active channel. Table 3.10.1 illustrates examples of channel sequences in both synchronized and nonsynchronized scans in which eight channels are active. Scan synchronization is invoked by setting the SYNCHRONIZE SCAN control bit HIGH in the BCR.

Table 3.10.1. Channel Order (Active channels 00-07)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	34567012	01234567
Tn+1	56701234	01234567
Tn+2	01234567	01234567
Tn+3	45670123	01234567
Tn+4	12345670	01234567

To invoke the scan-synchronized mode, set the SYNCHRONIZE SCAN control bit HIGH in the BCR, and wait for the CHANNELS READY flag (3.4.4) in the BCR to undergo a LOW-to-HIGH transition. While the CHANNELS READY flag is LOW, the following sequence is executed by the local controller:

1. The Group-0 sample clock (Section 3.6.1) is distributed to all input channels,
2. All ADC's are channel-synchronized (Section 3.6.2),
3. All channels are scan-synchronized.

The buffer clears to empty, and the first two scans are discarded to ensure full synchronization. Subsequent samples are scan-synchronized as described above. The Channels-Ready flag can be used to generate an interrupt at the end of the process.

Notice that all enabled input channels receive the sample clock selected for Group-0 *while operating in the scan-synchronized mode*, and the sample clock settings for Group-1 through Group-3 are ignored. Disabled groups remain disabled.

Use the following sequence to scan-synchronize multiple boards (Paragraph 3.6.3)

Synchronize ADC's:

1. On all boards: Set SYNCHRONOUS SCAN;
   Wait for Channels Ready LOW-to-HIGH on all boards (LOW 1-100ms).
   (All ADC's are synchronized, but sample-skewed between boards)
2. On Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on all boards (LOW 1-100ms).
   (All ADC's are scan synchronized; but the data buffers are skewed)

Global Buffer Clear:

3. On all boards: Set the CLEAR BUFFER ON SYNC bit,
4. On Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on the initiator. (LOW 10us to 5ms),
   (All ADC's and buffers are scan-synchronized)
5. On all boards: Clear the CLEAR BUFFER ON SYNC bit.

For optimum DC performance, execute autocalibration on all boards after synchronizing the ADC's on all boards, and follow the procedure with a 'global clear' operation.

NOTE: If autocalibration is executed while scan-synchronized, repeat the global buffer clear sequence (Steps 3 through 5). To simplify this operation, the CLEAR BUFFER ON SYNC control bit can be allowed to remain HIGH while scan-synchronized.

3.11 Board Configuration Register

The read-only board configuration register (Table 3.11.1) contains the existing firmware revision, and a status field that indicates the availability of optional features.

Table 3.11.1. Board Configuration Register

Offset: 0000 0024h **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16	High if the board contains only 16 input channels.
D17	High if the board contains only 8 input channels.
D18-D31	(Reserved)

3.12 External Independent Burst Triggering

Since the delta-sigma conversion process is essentially continuous, an acquisition 'burst' is initiated by clearing the input buffer when a burst trigger occurs, and allowing subsequent 'burst' data to accumulate in the buffer. The External Independent Burst Triggering feature allows a burst to be initiated externally through the AUX I/O pins in the system I/O connector, regardless of the selected rate assignment (Paragraph 3.6.1.2).

This feature is available with firmware revision 502h (Table 3.11.1) and subsequent 5XXh revisions.

The External Burst Triggering feature is implemented as follows:

When ARM EXTERNAL TRIGGER is set HIGH in the BCR, the buffer is cleared and held in this state until an external trigger occurs at the AUX INPUT HI/LO pins in the system I/O connector. The trigger is edge-detected, and must be asserted HIGH for a minimum of 100ns in order to be acknowledged. When the trigger occurs:

1. The ARM EXTERNAL TRIGGER bit is cleared LOW in the BCR, and:
2. The buffer is enabled, and subsequent data accumulates in the buffer, beginning with the first complete data scan after the trigger occurs.

To support daisy-chain operation of multiple boards, the AUX OUTPUT follows the AUX INPUT, with no clocking delays introduced.

****

The AUX inputs, outputs and associated digital ground (DGND) pins are located in the system I/O connector as:

I/O Pin B1: AUX INPUT LO
I/O Pin B2: AUX INPUT HI
I/O Pin B3: DGND
I/O Pin B4: DGND
I/O Pin B5: AUX OUTPUT LO
I/O Pin B6: AUX OUTPUT HI.

3.13 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance is suspended. Abrupt changes include:

- A change in voltage range or sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PCI-24DSI32 board contains sixteen dual delta-sigma 24-Bit A/D converters and all supporting functions necessary for adding analog I/O capability to a PCI expansion system. A PCI interface adapter (Figure 4.1) provides the interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

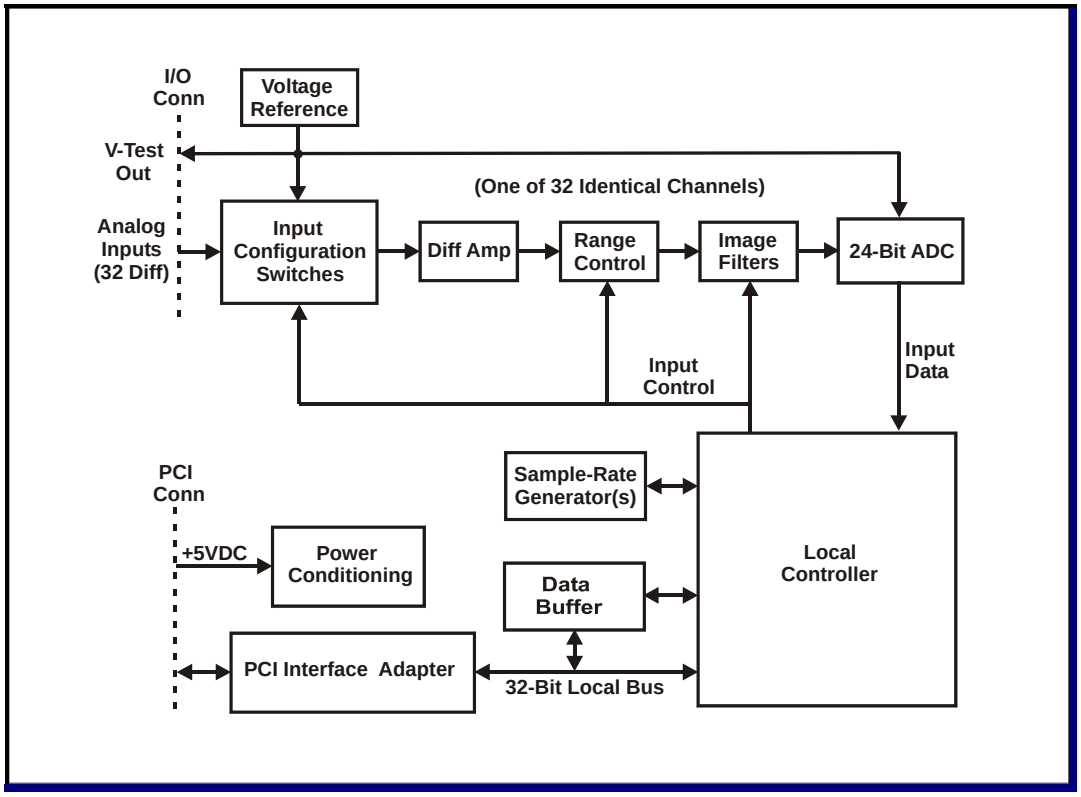

Figure 4.1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibration of each input channel is adjusted with correction values that are determined during autocalibration.

4.2 Analog Inputs

The 32 analog input channels are arranged in four channel groups, with each group containing one-fourth of the channels present on the board. Group 0 through Group 3 can be designated as either active or inactive, with only active groups sending input data to the data buffer. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a differential amplifier which removes any common mode voltage that might be present. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or positive full-scale reference voltage.

A range control attenuator adjusts the maximum level of the signal to the full-scale input range of 2.0 VRMS required by the ADC. High frequency noise and digital filter images are attenuated by a 2-pole Butterworth lowpass filter, the cutoff frequency of which can be selected as either of two fixed frequencies.

The final conditioned, scaled and filtered input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then attaches a 5-bit channel tag to the data word, applies offset and gain correction factors, and finally transfers the corrected data to the input data buffer.

Antialias filtering is provided by each ADC in the form of a lowpass digital filter with a sharp cutoff frequency at approximately 40-50 percent of the sampling frequency. The digital filter has no filtering effect at multiples of the sampling clock, which is a multiple (x32-128) of the sampling frequency. To prevent extraneous signal frequency components within these "filter images" from appearing in the passband, the hardware image filters shown in Figure 4.1 can be configured to provide filtering within the digital filter images.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The offset error of each channel is determined first, by selecting a zero input reference level and storing the values reported from all channels. A precision internal voltage reference then is used to calculate the gain error, and both offset and gain correction values are stored in static RAM for retrieval during data acquisition.

The internal voltage reference is adjusted to equal 99.000 percent of the selected input voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

4.4 Sampling Clocks

An internal sample rate generator provides a frequency range of 20-55 MHz, which is divided down by a software-specified integer to provide sample rates from 2.0 KSPS to 200 KSPS. Three addition rate generators are available as a manufacturing option, with each generator independently adjustable and assignable to any or all channel groups.

An external clock output can be assigned as the output of the rate generator, or as the ADC sample clock. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive and retransmit the external clock are *clock targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Control

Regulated supply voltages of +5 Volts, +6 Volts and ±15 Volts are required by the analog networks. Multiple DC/DC converters in the power conditioner use +5V input power from the PCI bus to produce preregulated DC voltages that subsequently are postregulated with linear regulators to the required supply voltages. Linear regulators ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

LOCAL ADDR	ACCESS MODE	REGISTER	DEFAULT	DESCRIPTION
00	R/W	**Board Control (BCR)**	0000 383Ch *	Board Control Register (BCR)
04	R/W	**Nref PLL Control**	0000 01F4h	PLL reference oscillator control integer. (PLL configuration only)
08	R/W	**Nvco PLL Control (Legacy Nrate)**	0000 01F4h	PLL vco control integer. (Nrate for the legacy rate generator)
0C	RO	**Rate Assignments**	0000 0000h ****	ADC Clock source; Group disables.
10	R/W	**Rate Divisor**	0000 0005h	Sample rate divisor.
14	RO	**(Reserved)**	0000 0000h	---
18	R/W	**PLL Reference Freq**	XXXX XXXXh	PLL reference frequency indicator
1C	RO	(Reserved)	0000 0000h	---
20	R/W	**Buffer Control**	0003 FFFEh **	Input buffer control and status
24	RO	**Board Configuration**	00XX XXXXh	Installed firmware and hardware options
28	RO	**Buffer Size**	0XXX XXXXh	Number of ADC values in the input buffer.
2C	RO	Autocal Values ***	---	---
30	RO (DMA)	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag
34-7C	--	(Reserved)	---	---

* Changes to 0000 783Ch when the input buffer fills.
** Changes to 0103 FFFEh when the buffer fills.
*** Maintenance register. Shown for reference only.
**** May be 0000 0190h in earlier firmware revisions.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.
D01	R/W	AIM1	
D02	R/W	RANGE0	Analog input range selection. Defaults to ±10V range.
D03	R/W	RANGE1	
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults HIGH to Initiator mode.
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.
D07	R/W	*AUTOCAL	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.
D09	R/W	INTERRUPT A1	
D10	R/W	INTERRUPT A2	
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D12	RO	AUTOCAL PASS	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.
D13	RO	CHANNELS READY	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.
D15	R/W	*INITIALIZE	Initializes the board when asserted. Sets all defaults.
D16	R/W	SYNCHRONIZE SCAN	Selects synchronous sampling mode.
D17	R/W	CLEAR BUFFER ON SYNC	When this bit is HIGH, the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.
D18	R/W	RATE GEN EXT CLOCK OUT (Initiator Mode only)	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock. (If Group-00 external clocking is selected, the output is driven by the internal rate generator and the Group-00 divisor).
D19	R/W	SELECT LOW IMAGE FILTER	When this bit is HIGH, the low-frequency image filter is selected. When LOW, the high filter is selected.
D20	R/W	(Reserved)	--
D21	R/W	ARM EXTERNAL TRIGGER	Arms the external burst trigger input. (3.12)
D22	R/W	THRESHOLD FLAG OUT	Routes the threshold flag to the AUX LVDS output.
D23-31	RO	(Reserved)	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Changes to 0000 783Ch when the input buffer fills.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
Rate generator clocks are initialized	250 ms

Table 3.4. Analog Input Function Selection

AIM[..0]	FUNCTION OR MODE
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.4.3. Analog Input Range Selection

RANGE[1..0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±2.5 Volts
2	±5 Volts
3	±10 Volts

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

SELECTED DATA WIDTH	RESERVED (Zero)	CHANNEL TAG	ZERO-PAD	CHANNEL DATA VALUE
16 Bits	D[31..29]	D[28..24]	D[23..16]	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold (duplicated in the BCR)
D[18]	R/W	DISABLE BUFFER INPUT	Disables ADC inputs to the buffer
D[19]	R/W	CLEAR BUFFER **	Clears (empties) the buffer
D[21..20]	R/W	DATA WIDTH	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23..22]	RO	(Reserved)	---
D[24]	R/W	BUFFER OVERFLOW ***	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW ***	Reports buffer underflow (Read on empty)
D[31..22]	RO	(Reserved)	---

* Changes to 0103 FFFEh when the buffer fills. ** Clears automatically. *** Clear by writing LOW, or by board reset.

Table 3.6.1.1. Channel Groups

	INPUT CHANNELS		
CHANNEL GROUP	**32-CHANNEL BOARD**	**16-CHANNEL BOARD**	**8-CHANNEL BOARD**
0	00-07	00-03	00,01
1	08-15	04-07	02,03
2	16-23	08-11	04,05
3	24-31	12-15	06,07

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	SAMPLE CLOCK SOURCE; GROUP-0 ENABLE/DISABLE	0
D[07..04]	GROUP-1 ENABLE/DISABLE	1
D[11..08]	GROUP-2 ENABLE/DISABLE	2
D[15..12]	GROUP-3 ENABLE/DISABLE	3
D[31..16]	(Reserved)	---

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT *	GROUPS 1-3 ASSIGNMENT
0	Internal Rate Generator	(Unused)
1	(Reserved)	(Unused)
2	(Reserved)	(Unused)
3	(Reserved)	(Unused)
4	External Sample Clock (as rate generator input)	Enabled
5	Direct External Sample Clock (routed directly to ADC)	Enabled
6-7	**Disabled**	**Disabled**
8-15	(Reserved)	(Reserved)

* Applies to all channel groups. Disabling Group-0 disables all groups.

Table 3.6.1.3. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0005h**

BIT FIELD:	FUNCTION
D[07..00]	RATE DIVISOR (**Ndiv)**
D[31..08]	(Reserved)

Table 3.6.2.1-1. PLL Nref Register

Offset: 0004h **Default: 0000 01F4h**

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[09..00]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 30-1000.
D[31..27]	R/W	(Reserved)	---

Table 3.6.2.1-2. PLL Nvco Register

Offset: 0008h **Default: 0000 01F4h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[09..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 30-1000.
D[31..27]	R/W	(Reserved)	---

Table 3.6.2.1-3. Summary of PLL Sample Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Frequency Range	**Fgen**	20-55 MHz
VCO Factor	**Nvco**	30-1000
Reference Factor	**Nref**	30-1000
Rate Divisor	**Ndiv**	0 - 25
Reference Frequency	**Fref**	Standard value = 32.768MHz

Table 3.6.2.2-1. Legacy Rate Control Register

Offset: 0008h **Default: 0000 0000h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[16..00]	R/W	RATE CONTROL **(Nrate)**	Frequency control factor; 0-511
D[31..17]	R/W	(Reserved)	---

* Default frequency is 25.6MHz.

Table 3.6.3. Direct External Clocking

Sample Rate Fsamp (KSPS)	External Clock Frequency	Divisor Integer Ndiv
2-50	256 * Fsamp	**2 thru 25**
50-100	128 * Fsamp	**1**
100-200	64 * Fsamp	**0**

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	(Reserved)
6	(Reserved)
7	(Reserved)

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.10.1. Channel Order (Active channels 00-07)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	34567012	01234567
Tn+1	56701234	01234567
Tn+2	01234567	01234567
Tn+3	45670123	01234567
Tn+4	12345670	01234567

Table 3.11.1. Board Configuration Register

Offset: 0000 0024h **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16	High if the board contains only 16 input channels.
D17	High if the board contains only 8 input channels.
D18-D31	(Reserved)

Record of Revisions:

122207: Tables 3.1 and 3.6.1.2-1: Revised Assignment Register default value to all-zero.
Paragraph 3.5.3.1: Added note pertaining to the Threshold Flag Out control bit.
Paragraph 3.13: New paragraph.

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