General Standards Corporation

High Performance Bus Interface Solutions

Rev: 052914

PMC66-18AI32SSC1M

32-CHANNEL DIFFERENTIAL 18-Bit or 16-Bit, SIMULTANEOUS SAMPLING, PMC ANALOG INPUT BOARD

With 1.0MSPS Sample Rate per Channel, and 66MHz PCI Support

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC66-18AI32SSC1M board is a single-width PCI mezzanine card (PMC) that provides high-speed simultaneous 18-bit or 16-bit analog input capability for PMC applications. 32 differential analog input channels can be digitized simultaneously at rates up to 1,000,000 conversions per second per channel, with software-controlled voltage ranges of ±10V or ±5V. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

Autocalibration determines offset and gain correction values for each input channel, and the corrections are applied subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

Power requirements consist of +5 VDC from the PCI bus in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional air cooling. Specific details of physical characteristics and power requirements are contained in the PMC66-18AI32SSC1M product specification. Figure 1.1-1 shows the physical configuration of the board and the arrangement of major components.

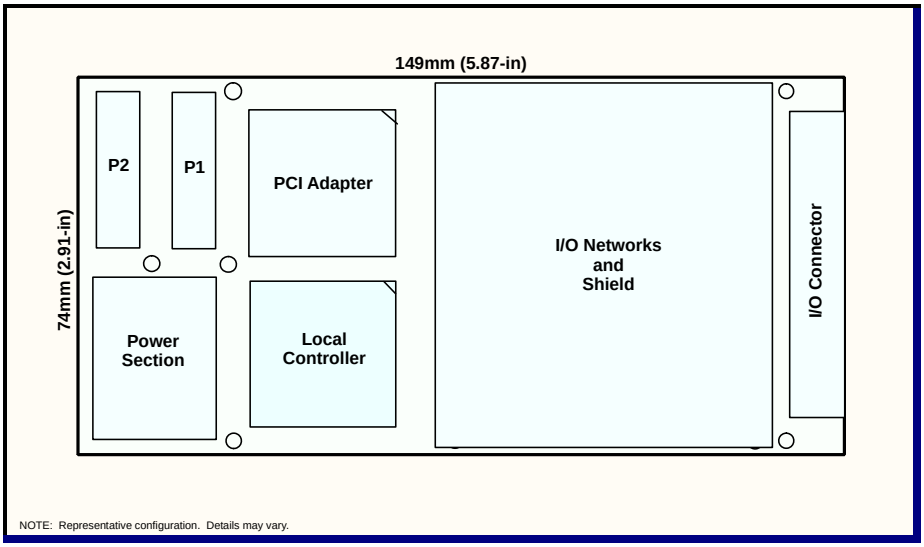

Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. System input and output connections are made through a high-density front-panel I/O connector. An auxiliary connector on Side-2 of the board provides bidirectional external sync and clock ports for internal multisite synchronization.

1.2 Functional Overview

The PMC66-18AI32SSC1M analog input board samples and digitizes up to 32 input channels simultaneously at rates up to 1,000,000 samples per second for each channel, with conversion resolution available as either 18 bits or 16 bits. Each input channel contains a dedicated successive-approximation (SAR) ADC, the sampled data from which is error-corrected and routed to the PCI bus through a 1-MByte FIFO buffer. The 32-Bit local data path supports full D32 local-bus data packing for 16-Bit data. Throughput performance is further enhanced with 66MHz PCI support. All operational parameters are software configurable.

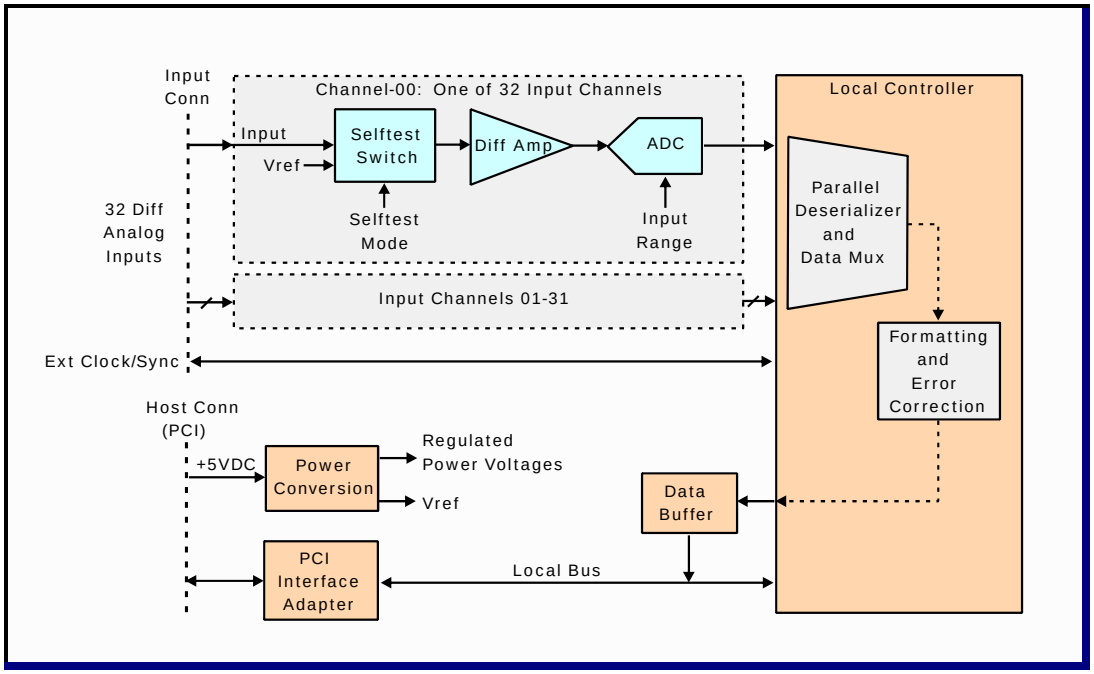

Figure 1.2-1. Functional Organization

Inputs can be sampled in groups of 2, 4, 8, 16, or 32 channels; or any contiguous channel group can be designated for acquisition. The sample clock can be generated from (a) an internal rate generator, (b) by software or (c) by external hardware. Input ranges are software-selectable as ±10V or ±5V.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and applies the corrections subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the three mezzanine connectors P1, P2 and P4 facing the mating connectors J1, J2 and J4 on the host board (Figure 2.2-1). Then carefully press the board into position on the host. Verify that the mezzanine connectors have mated completely and that the board is seated firmly against the host board. Attach the board to the host with 2.5 x 6.5mm panhead screws. Pass the screws through the host board into the corresponding mounting holes in the standoffs and front-panel bezel. Tighten the screws carefully to complete the installation. Do not overtighten.

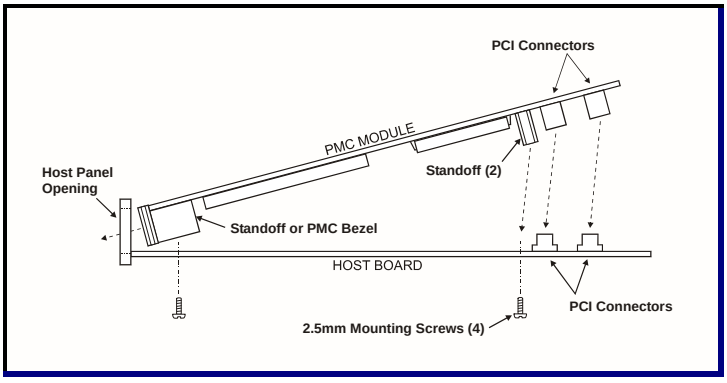

Figure 2.2-1. Mechanical Installation

2.2.2 Input/Output Cable Connections

System I/O connections are made through the 80-Pin front-panel system I/O connector (Figure 2.2-2) with the pin assignments listed in Table 2.2-1.

Auxiliary Sync I/O connections are made through a low-profile 6-Pin, single-row connector located on the back of the board (Side-2), with the pin assignments shown in Table 2.2-2. The auxiliary sync I/O connector is designed to mate with a Molex cable connector Model 51146-0600.

Table 2.2-1. System I/O Connector Pin Functions

Row A			Row-B	
Pin	Signal		Pin	Signal
1	INP00 LO		1	INP17 LO
2	INP00 HI		2	INP17 HI
3	INP01 LO		3	INP18 LO
4	INP01 HI		4	INP18 HI
5	INP02 LO		5	INP19 LO
6	INP02 HI		6	INP19 HI
7	INP03 LO		7	INP20 LO
8	INP03 HI		8	INP20 HI
9	INP04 LO		9	INP21 LO
10	INP04 HI		10	INP21 HI
11	INP05 LO		11	INPUT RTN
12	INP05 HI		12	INPUT RTN
13	INPUT RTN		13	INP22 LO
14	INPUT RTN		14	INP22 HI
15	INP06 LO		15	INP23 LO
16	INP06 HI		16	INP23 HI
17	INP07 LO		17	INP24 LO
18	INP07 HI		18	INP24 HI
19	INP08 LO		19	INP25 LO
20	INP08 HI		20	INP25 HI
21	INP09 LO		21	INP26 LO
22	INP09 HI		22	INP26 HI
23	INP10 LO		23	INPUT RTN
24	INP10 HI		24	INPUT RTN
25	INP11 LO		25	INP27 LO
26	INP11 HI		26	INP27 HI
27	INPUT RTN		27	INP28 LO
28	INPUT RTN		28	INP28 HI
29	INP12 LO		29	INP29 LO
30	INP12 HI		30	INP29 HI
31	INP13 LO		31	INP30 LO
32	INP13 HI		32	INP30 HI
33	INP14 LO		33	INP31 LO
34	INP14 HI		34	INP31 HI
35	INP15 LO		35	INPUT RTN
36	INP15 HI		36	INPUT RTN
37	INP16 LO		37	DIG RTN
38	INP16 HI		38	CLOCK I/O
39	INPUT RTN		39	DIG RTN
40	INPUT RTN		40	SYNC I/O

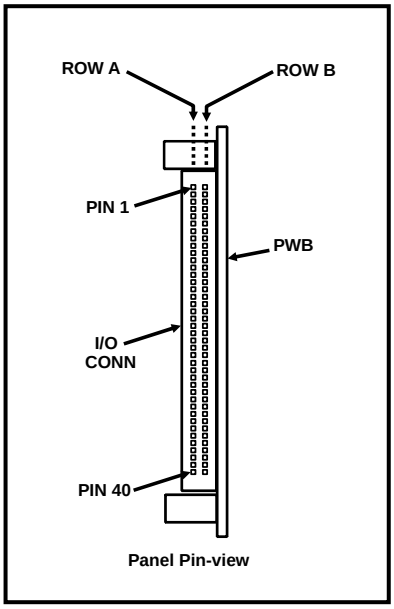

Figure 2.2-2. System I/O Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG,** or equivalent.

Table 2.2-2. Auxiliary Sync I/O Connections

Signal	P1 Pin
DIG RTN	1
AUX CLOCK	2
DIG RTN	3
AUX SYNC	4
DIG RTN	5
(Reserved)	6

.

2.3 System Configuration

2.3.1 Analog Inputs

The 32 analog input channels can be configured for either differential or single-ended operation. This configuration is determined by external wiring as shown in Figure 2.3-1, and is not affected by application software.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

This operating mode also offers the highest rejection of the common mode noise, which is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode (Figure 2.3-1a), the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point which must ensure that the sum of the signal level **(Vsig)** and the common mode voltage **(Vcm)** remain within the range specified for the board. Ground current through the INPUT RTN pins must be limited in order to avoid damage to the cable or the input board.

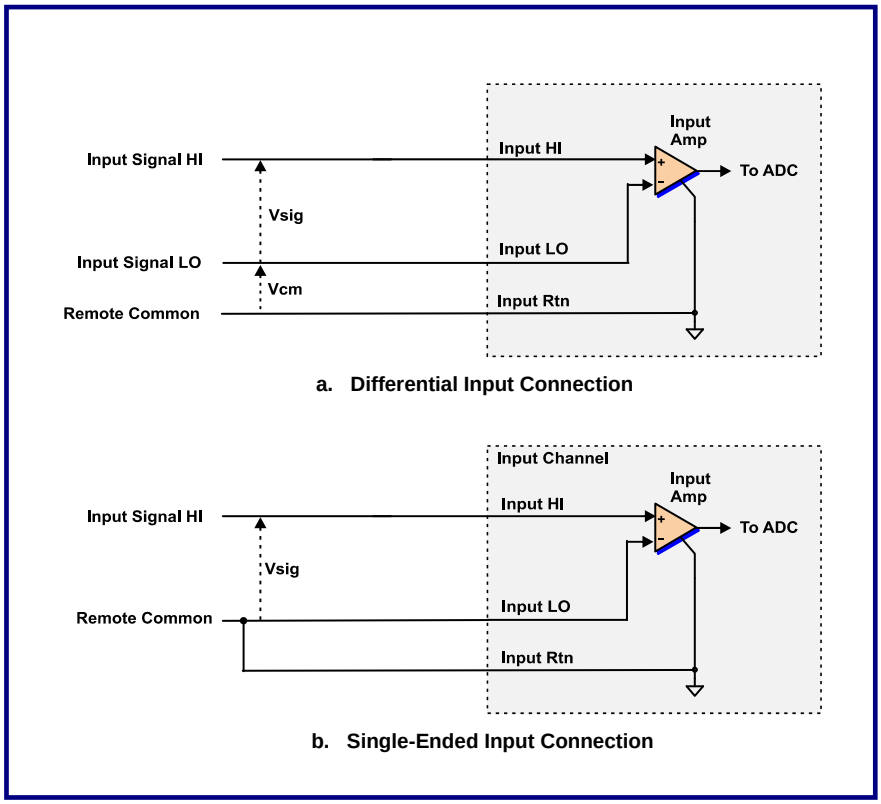

Figure 2.3-1. Analog Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1b) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. A single-ended configuration usually is more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or could generate potentially destructive ground current.

For applications in which multiple signal sources share a single ground reference or return, the differential configuration is recommended, with all "LO" inputs connected together at the common remote return.

2.3.2 External Clock and Sync I/O

The CLOCK I/O and SYNC I/O pins in the I/O connector are bidirectional TTL signals that provide external control of analog input sampling and burst triggering. These signals are referenced to the DIG RTN pin, which is connected internally to PCI digital ground.

When configured as inputs by selection of the target mode, these pins accept clock and triggering signals from any external TTL source, including those originating on another PMC66-18AI32SSC1M. For boards configured as initiators, the clock and sync pins become outputs that can be used to control external devices, including other PMC66-18AI32SSC1M boards. Loading of initiator outputs should not exceed 10 milliamps. In the default state after power-up or initialization, both pins are configured as inputs. Clock and sync pins default to inputs (targets), and are pulled up internally to +3.3V through 4.7K-Ohms.

NOTE: The logic polarities of the clock and sync I/O pins can be inverted by application software.

2.3.2.1 External ADC Clocking

When the CLOCK I/O pin is configured as an input, all active input channels are sampled on the falling edge of a TTL input signal on this pin. Both the HIGH and LOW states of the clock input must have minimum durations of 100ns.

When configured as an initiator, the CLOCK I/O pin becomes a normally HIGH output that falls for 120-180ns at each occurrence of the internal ADC sample clock.

2.3.2.2 External Burst Triggering

When the SYNC I/O pin is configured as an input, a high-to-low TTL transition on this pin can be used to trigger an internal acquisition burst. Both HIGH and LOW sync input states must have durations of at least 100ns.

When configured as an initiator, the SYNC I/O pin becomes a normally HIGH output that falls for 120-180ns at the initiation of each internal triggered burst.

2.3.3 Auxiliary External Clock and Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking to external events. These TTL connections are available as AUX-CLOCK and AUX-SYNC (Table2.2-2), and are accessible through a low-profile 6-Pin connector on the back of the board (Side-2).

The AUX I/O pins can be programmed to be asserted either HIGH or LOW, and can be configured individually as inputs or outputs. Active AUX *outputs* produce an output pulse for each internal ADC sample clock or burst trigger. Source and sink load capacity of each output is 8 milliamps. Further details pertaining to these I/O functions are tabulated in Table 3.9-1.

2.3.4 Multiboard Synchronization

If multiple boards are to be synchronized together, the CLOCK I/O and/or the SYNC I/O pins from one board, the ***initiator***, are connected to the corresponding pins of one or more ***target*** boards (Figure 2.3-2). The controlling software determines specific clocking and burst triggering functions. The maximum number of targets depends upon both static loading and cable characteristics, and can vary from four to as many as eight.

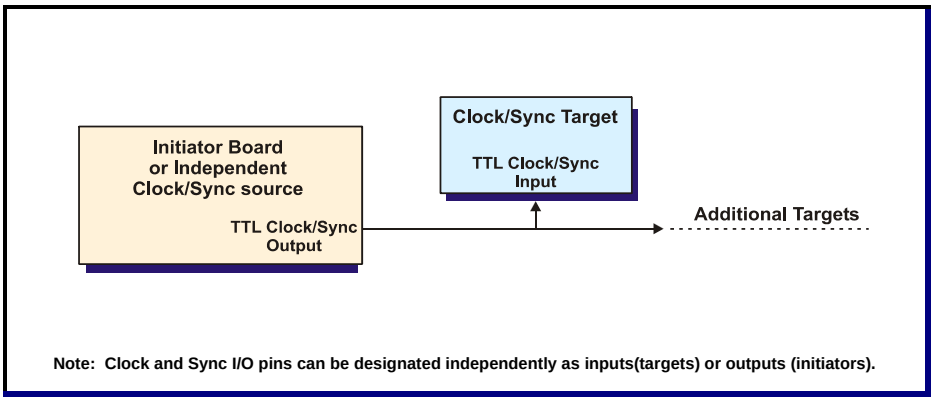

Figure 2.3-2. Multiboard Synchronization

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog input channels are software-calibrated to a single internal voltage reference by an embedded autocalibration firmware utility. The procedure presented here describes the verification and adjustment of the internal reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC site	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to two 0.02-inch square test posts.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the single reference voltage that ensures conformance to the product specification. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1.

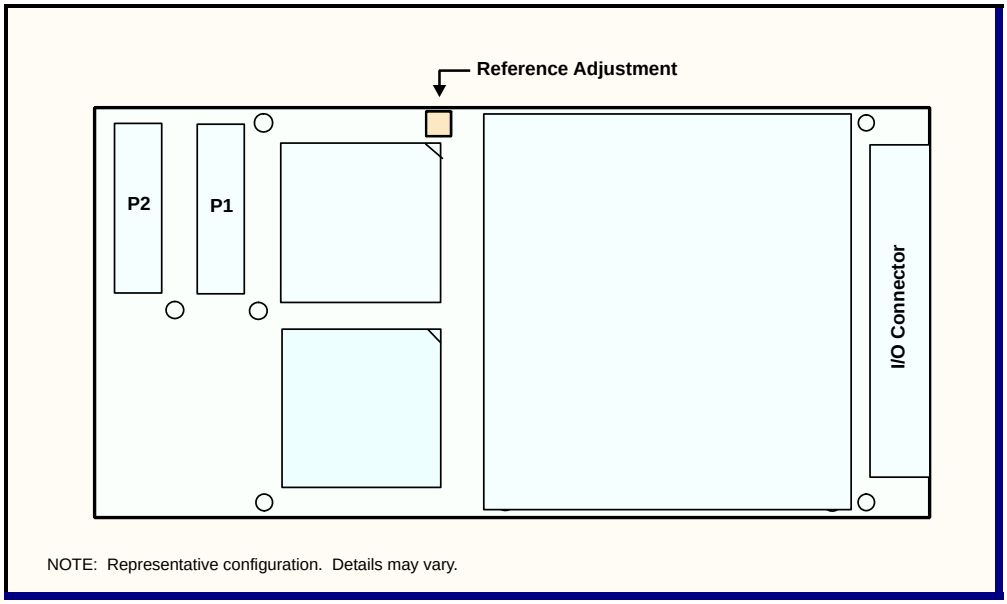

Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the board to be adjusted is installed on an operational host:

1. Connect the digital multimeter between VCAL (+) Pin-3, and REF RTN (-) Pin-4 in the J3 test connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding.
3. Select the highest input range; ±10V or ±2.5V.
4. Verify that the digital multimeter indication is +9.9900 VDC ±0.0008 VDC for the ±10V range, or +2.4975 VDC ±0.0004 VDC for the ±2.5V range. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer accordingly.
5. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-18AI32SSC1M is compatible with the IEEE PCI Local Bus specification, Revision 2.3. A PLX™ PCI-9056 adapter operating in J-mode controls the PCI interface, and supports both 33MHz and 66MHz PCI clock frequencies, as well as the D32 PCI bus width. Configuration-space registers are initialized internally to support the location of the board on any 64 long-word boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All local data transfers are long-word D32. Specific operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer. The board identifies itself over the PCI bus with device, vendor and subsystem identification codes that are available on the General Standards web site.

Table 3.1-1. Control and Data Registers

Offset (Hex) [1]	Register	Access Mode [2]	Default	Primary Function
0000	BOARD CONTROL (BCR)	R/W	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	R/W	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	XXXX XXXXh	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	R/W	0001 02D0h	Rate-A generator freq selection
0014	RATE-B GENERATOR	R/W	0000 2000h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer
001C	BURST SIZE	R/W	0000 0001h	Number of sample clocks in a triggered burst.
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	ACTIVE CHANNEL ASSIGNMENT	R/W	0000 0100h	Specific first and last active channels.
0028	BOARD CONFIGURATION	RO	000X XXXXh	Firmware revision and option straps.
002C	Autocal Values [3]	R/W	0000 080Xh	Autocal value readback.
0030	Auxiliary R/W Register [3]	R/W	0000 0000h	Auxiliary register. For internal use only.
0034	AUXILIARY SYNC I/O CONTROL	R/W	0000 0000h	Controls auxiliary sync I/O port
0038	SCAN MARKER UPPER WORD	R/W	0000 0000h	Packed-data scan marker D[31..16].
003C	SCAN MARKER LOWER WORD	R/W	0000 0000h	Packed-data scan marker D[15..0].
0040	Test Utility Register [3]	R/W	0000 0000h	Maintenance utility register.
0044	PRETRIGGER COUNTER LOW	RO	0000 0000h	Pretrigger counter lower 32 bits D00-D31.
0048	PRETRIGGER COUNTER HIGH	RO	0000 0000h	Bits D00-D15 are 'Pretrigger Counter' high bits D32-D47.
004C-0050	(Reserved)	RO	0000 0000h	---
0054	EXTERNAL CLOCK DIVISOR	R/W	0000 0000h	External clock frequency divisor (3.15)
0058-007C	(Reserved)	RO	0000 0000h	---

[1] Offsets from the PCI base address for local addressing.

[2] R/W = Read/Write; RO = Read-Only.

[3] Maintenance register; Shown for reference only

3.2 Board Control Register (BCR)

The Board Control Register (BCR) controls primary board functions, including the analog input mode and voltage range. Table 3.2-1 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

Bit	Mode	Designation	Def	Description	Ref
D00-D02	R/W	AIM[2..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	(Reserved)	0	---	---
D04-D05	R/W	RANGE[1..0]	2h	Analog input range. Defaults to ±10V range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.	3.5.1.3
D07	R/W	(Reserved)	0h	---	---
D08	R/W	BACKGROUND CALIBRATION	0h	Selects background (continuous) autocal. Superseded by AUTOCAL. Maximum sample rate = 750SPS	3.14
D09-D10	R/W	(Reserved)	0h	---	---
D11	R/W	DISABLE SCAN MARKER	0	Disables the scan marker in data packing mode.	3.11
D12	R/W	*INPUT SYNC	0	Produces a single ADC clock when selected in the Scan and Sync Control Register, or a single burst trigger when selected with the Burst On Sync control field.	3.4.3 3.12.1
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal completion confirms a successful calibration.	
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.11
D19-D31	RO	(Reserved)	0	---	---

* Clears automatically when the associated operation is completed.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This 200-300millisecond process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Board configuration terminates with the PCI interrupt disabled.

3.3.2 Initialization

Internal control logic can be initialized without reconfiguration of the PCI registers by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all defaults are invoked (Table 3.2-1),
- Analog input voltage range is ±10 Volts (Tables 3.2-1, 3.4-1),
- All available channels are active (Table 3.4-2),
- Input sample clocking is disabled (Table 3.4-2),
- Rate generator Rate-A is adjusted for a 50 kHz sample rate, and is disabled (Table 3.4-4).
- Analog input data coding format is offset binary; Data packing is disabled (Table 3.2-1),
- Data reporting resolution is 16 Bits (Table 3.5-3),
- Data packing is disabled (Table 3.11-1),
- The analog input buffer is reset to empty (Table 3.5-3),

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Parameters

3.4.1 Input Voltage Range

BCR control field RANGE[] (Table 3.4-1) selects the analog input voltage range.

Table 3.4-1. Analog Voltage Range Selection

	Analog Input Range Set *	
Range Select[1:0]	**High Range Set**	**Low Range Set**
0	(Reserved)	(Reserved)
1	±5 Volts	±1.25 Volts
2	±10 Volts	±2.5 Volts
3	±10 Volts	±2.5 Volts

* See Table 3.10-1 for input range options.

3.4.2 Active Channel Selection

NOTE: The Scan and Sync control register (Table 3.4-2) controls the selection of active channels, as well as the configuration of internal timing signals.

3.4.2.1 Predetermined Channel Group

The analog inputs can be sampled in groups of 2, 4, 8, 16 or 32 active channels, or any single channel can be selected for digitizing. The number of active channels is selected by the ACTIVE CHANNELS[] field in the scan and sync control register. Each active channel group commences with Channel-00, and proceeds upward through successive channels to the selected number of channels.

For Single-Channel sampling (ACTIVE CHANNELS[] = 0), the channel to be digitized is selected by the SINGLE-CHANNEL SELECT control field.

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

Bit	Mode	Designation	Def	Description
D00-D02	R/W	ACTIVE CHANNELS	5h	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 32 channels (00-31); Default value 6 => (Reserved) 7 => Channel group assignment (See Section 3.4.2.2) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	SAMPLE CLOCK SOURCE	0h	Selects the analog input sample clocking source and I/O mode: 0 => External Clock input line (Selects Clock TARGET mode) 1 => Internal Rate-A generator output 2 => Internal Rate-B generator output 3 => BCR Input Sync control bit.
D05	R/W	ENABLE CLOCKING	0	Enables the selected ADC clocking process
D06	R/W	ENA EXT CLK DIVISION	0	Enables internal frequency division of an external clock source (3.15)
D07	RO	BURST BUSY	0	Indicates that a triggered burst is in progress.
D08-D09	R/W	BURST ON SYNC	0h	Selects bursting trigger source and I/O mode (Section 3.12) 0 => Bursting disabled 1 => Rate-B generator 2 => External Sync-I/O input (Selects Sync TARGET mode) 3 => BCR Input Sync control bit.
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	INVERT CLOCK AND SYNC I/O	0	Inverts the logic polarities of external clock and sync I/O input and output signals to assert HIGH.
D12-17	R/W	SINGLE-CHANNEL SELECT	0h	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	ENABLE PRETRIGGERING	0	Enables the pretriggering mode and the 'Latched Trigger' status flag.
D19	R/W	LATCHED TRIGGER	0	Records a trigger event when pretriggering is enabled. Cleared by direct write, by clearing the buffer, or by disabling pretriggering.
D20-D31	RO	(Reserved)	0	Inactive

3.4.2.2 User-Defined Channel Group

If "Channel group assignment" is selected in the ACTIVE CHANNELS field in the Scan and Sync control register (Table 3.4-2), the first and last active channels are defined by the Active Channels Assignment control register shown in Table 3.4-3. The group of active channels is *contiguous*, beginning with the channel designated by the FIRST CHANNEL SELECT field, and proceeding upward through consecutive channels to and including the channel designated by LAST CHANNEL SELECT. The LAST CHANNEL SELECT field must be equal to or greater than the FIRST CHANNEL SELECT field.

When selection of active channels is user-defined, the context of the "Channel-00" tag in the data buffer (Table 3.5-1) changes to the "First-Channel" tag. For example, if FIRST CHANNEL SELECT = 05, then D16 in the buffer will be HIGH for Channel-05 data, and LOW otherwise. This context change applies also to the scan marker if data packing is enabled (Section 3.11).

NOTE: The Active Channel Assignment register is monitored for invalid values, and is adjusted automatically to correct assignment errors. The first channel must not be higher than the selected last channel, and the selected last channel must not exceed the highest available channel number.

Table 3.4-3. User-Defined Active Channel Assignment

Offset: 0000 0024h **Default: 0000 0100h**

Data Bit	Mode	Designation	Default	Description
D00-D07	R/W	FIRST CHANNEL SELECT	0	First (lowest-numbered) active channel
D08-D15	R/W	LAST CHANNEL SELECT	1	Last (highest-numbered) active channel
D16-D31	RO	(Reserved)	0	Inactive. Returns all-zero.

3.4.3 Timing Organization

Figure 3.4-1 illustrates the manner in which ADC timing signals are organized within the board. The input sample clock selector is controlled by the Scan and Sync control register, which provides direct software control of clocking and sync operations. The bidirectional external clock I/O pin provides external control of ADC clocking.

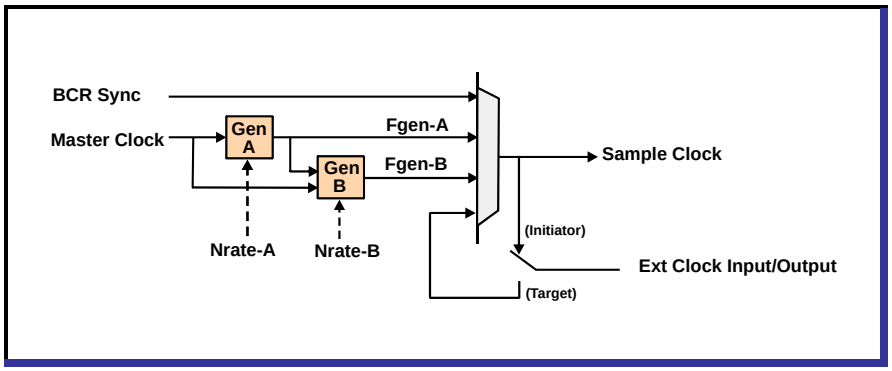

Figure 3.4-1. Sample Clock Organization

Two internal rate generators operate directly from the master clock frequency, or can be cascaded. A sample clock can be generated by (a) an internal rate generator, (b) the INPUT SYNC control bit in the BCR, or (c) an external clock source. Each sample clock produces a sample of all active input channels.

NOTES: The logic polarities of the external clock and sync I/O pins can be inverted by setting the INVERT CLOCK AND SYNC I/O control bit HIGH in the Scan and Sync control register (Paragraph 2.3.2 and Table 3.4-2). This inversion does not affect the Auxiliary Clock and Sync logic polarities selected in Table 3.9-1.

3.4.4 Sample Rate Control

All active channels are sampled, or clocked, simultaneously from the source selected by the SAMPLE CLOCK SOURCE control field in the Scan and Sync control register (Table 3.4-2).

NOTE: ADC sampling (clocking), is disabled while the ENABLE CLOCKING control bit is LOW, or is enabled when this bit is set HIGH.

3.4.4.1 Sample Rate Generators

Each of two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate control register. The two rate control registers are organized as shown in Table 3.4-4. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. D16 defaults to the HIGH (disable) state in the Rate-A control register.

Table 3.4-4. Rate Generator Control Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 02D0h (Rate-A), 0000 2000h (Rate-B)**

Data Bit	Mode	Designation	Default	Description
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

3.4.4.2 Rate Generator Frequency Control

Each rate generator is controlled by a *divisor* **Nrate** that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of **Fclk**, the output frequency **Fgen** of each generator is determined as:

Fgen (Hz) = Fclk (Hz) / Nrate,

where **Nrate** is the decimal equivalent of D00-D15 in the rate generator register (Table 3.4-5). **Fgen** is the sampling frequency, and equals the rate at which all active channels are sampled. **Fclk** has a standard value of 36 MHz, but may have other values depending upon custom ordering options.

The maximum sampling frequency **Fgen-max** is 1000 kHz.

Table 3.4-5. Rate Generator Frequency Selection

Nrate (RATE[15..0])		**Fgen (36 MHz Master Clock)**
(Dec)	**(Hex)**	**(Hz)**
36	24	1,000,000
37	25	972,973
---	---	Fgen (Hz) = 36,000,000 / Nrate

* ±0.005 percent.

3.4.4.3 Generator Cascading

To obtain very low sampling or burst-triggering rates, the Rate-B generator can be configured with the RATE-B CLOCK SOURCE control field to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

Fgen-B (Hz) = Fclk / (Nrate-A * Nrate-B) ,

which can produce sample rates as low as 0.009 Hz with **Fclk** = 36 MHz.

3.4.5 External Clock and Sync I/O

Multiple boards can be interconnected externally to produce synchronous analog input sampling and burst triggering. Figure 2.3-2 illustrates the interconnections required. One of the boards is designated as the *Initiator*, and the remaining boards are designated as *targets*.

A board that is enabled for external sync I/O is designated as a ***clock target*** by selecting 'External Clock Input Line' in the SAMPLE CLOCK SOURCE control field of the Scan and Sync control register. An external clock input signal can originate either from an initiator board, or from an independent TTL source. Any other value for this field designates the board as an ***clock initiator***.

A ***clock initiator*** generates an output clock pulse in conjunction with each internal ADC sample clock, and each of the target boards responds to the clock pulse by acquiring a single sample of all of its designated active channels.

External ***burst triggering*** I/O is implemented in the same manner as external clocking I/O, but the trigger source is selected through the BURST ON SYNC control field in the Scan and Sync control register, and the SYNC I/O pin provides the external trigger interface connection.

NOTES: To avoid contention on the SYNC I/O line, all initiator/target designations should be assigned before enabling external sync I/O operation. No more than one board can be designated as an initiator.

For optimum autocalibration effectiveness at rates above 50 KSPS, adjust the Rate-A Generator register to the same value on all boards.

Refer to Section 3.15 for an alternative function for the external clock input.

Refer to Paragraph 3.9 for alternative external clock and sync provisions.

3.5 Analog Data Control

3.5.1 Input Data Organization

Processed conversion data from the analog-to-digital converters (ADC's) flows into the analog input FIFO data buffer, and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

3.5.1.1 Input Data Buffer

Nonpacked analog input data is right-justified to the LSB, and occupies bit positions D00 through D15 for 16-Bit data, or D00 through D17 for 18-Bit data (Table 3.5-1). D31 is the Channel-00 tag, which is asserted when the data field contains Channel-00 data. The Channel-00 tag is not available for packed data.

The intermediate bit field is all-zero unless two's complement coding is selected, in which case the reserved bits become the sign extension. When selection of active channels is user-defined (3.4.2.2), the context of the "Channel-00 tag" in the data buffer (Table 3.5-1) becomes the "First-Channel tag."

An empty buffer returns an indeterminate value. Refer to Paragraph 3-11 for the configuration of packed data, and for the effect of data packing on buffer contents.

Table 3.5-1. Input Data Buffer; Nonpacked Data

Offset: 0008h **Default: N/A**

Native Data Width	Selected Data Width	Channel-00 Tag	Reserved * (Zero)	Channel Data Value
18 Bits	18 Bits	D[31]	D[30..18]	D[17..0]
	16 Bits	D[31]	D[30..16]	D[15..0]
16 Bits	---	D[31]	D[30..16]	D[15..0]

All fields are read-only; Write-data is ignored. *** Sign-extension in two's complement coding mode *for 18-Bit data only*.**

NOTE: The two's complement sign extension extends through D30 *for 18-Bit data only.* 16-Bit data, including two's complement data, is confined to single-word boundaries.

3.5.1.2 Data Width Selection

In the native 16-Bit configuration, the input ADC's are inherently 16-Bit devices and all data is reported in a 16-bit wide format. The 16-Bit reporting width has the significant advantage of supporting data packing (3.11), which essentially doubles the local data throughput.

For the native 18-Bit configuration, the ADC's are 18-Bit devices, and data can be reported in either 16-Bit or 18-Bit format. The 16-Bit data format in the native 18-Bit configuration supports data packing, as well as retaining much of the lower noise advantage provided by the 18-Bit ADC's. The 18-Bit data format is selected by setting the SELECT 18 BIT DATA control bit HIGH in the Input Data Buffer Control Register (Table 3.5-3). 16-Bit data is selected by the default LOW state of this control bit, which is ignored in the native 16-Bit configuration.

3.5.1.3 Data Coding Format

Analog input data is arranged in a right-justified data field with the coding conventions shown in Table 3.5-2. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

Table 3.5-2. Input Data Coding

	Digital Value (Hex)			
	Offset Binary		Two's Complement	
Analog Input Level	**18-Bit Data**	**16-Bit Data**	**18-Bit Data**	**16-Bit Data**
Positive Full Scale minus 1 LSB	0003 FFFF	0000 FFFF	0001 FFFF	0000 7FFF
Zero (Midscale)	0002 0000	0000 8000	0000 0000	0000 0000
Zero minus 1 LSB	0001 FFFF	0000 7FFF	0003 FFFF	0000 FFFF
Negative Full Scale	0000 0000	0000 0000	0002 0000	0000 8000

3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-3 controls and monitors the flow of data through the analog input data buffer. Asserting the CLEAR BUFFER control bit HIGH clears, or empties, the buffer. The Threshold Flag is HIGH when the number of values in the input data buffer ***exceeds the input threshold value*** defined by bits D00-D17, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.7) can be programmed to occur on either the rising or falling edge of the threshold flag.

The Buffer Size register shown in Table 3.5-4 contains the number of locations occupied in the buffer, and is updated continuously. ***If data packing is enabled and scan marking is disabled (3.11), the number of samples present in the buffer is twice the value contained in the Buffer Size register.***

Buffer underflow and overflow flags in the BCR indicate that the buffer has been read while empty or written to when full. Each of these situations is indicative of data loss. Once set HIGH, each flag remains HIGH until cleared, either by directly clearing the bit LOW or by clearing the buffer or initializing the board.

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

Data Bit	Mode	Designation	Def	Description
D00-D17	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D20	R/W	SELECT 18 BIT DATA	0	Selects the 18-Bit data width when HIGH, or 16-Bit width when LOW. Ignored in the native 16-Bit configuration
D21-D31	RO	(Inactive)	0	---

*Clears automatically within 200ns of being set

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

Data Bit	Mode	Designation	Def	Description
D00-D18	RO	BUFFER SIZE	00000h	Number of locations occupied in the input buffer
D19-D31	RO	(Inactive)	0	---

3.5.3 Analog Input Function Modes

BCR control field AIM[] selects the analog input signal source, and provides selftest modes for monitoring the integrity of the analog input networks. Table 3.5-5 summarizes the input function modes.

3.5.3.1 System Analog Inputs

With the default value of 'Zero' selected for the AIM[] field in the BCR, all ADC channels are connected to the system analog inputs from the system I/O connector.

Table 3.5-5. Analog Input Function Selection

AIM[2:0]	Function or Mode
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

3.5.3.2 Selftest Modes

In the selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and the averaged values of multiple samples should be used for critical measurements.

The ZERO selftest applies a Zero reference signal to all input channels, and should produce a nominal midscale reading of 0000 8000h for 16-Bit data, or 0002 0000h for 18-bit data.

For the +VREF test, a precision reference voltage is applied to all inputs. The +VREF reference voltage equals 99.900% of the positive fullscale value (nominally 0000 FFDFh for 16-Bit data, or 0003 FF7Dh for 18-Bit data).

3.6 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup or a PCIbus reset,
- Input range change,
- Sample rate change, if greater than 50 kHz.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR, and the control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of approximately 1.0 second. Completion of the operation can be detected either by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.7) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

A small error can be introduced when the input range is changed, or when a large change occurs in the sample rate. Performing autocalibration with the required sample rate selected eliminates this error. During autocalibration, no control settings are altered and external analog input signals are ignored.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

NOTE: The autocalibration utility uses the contents of the Rate-A generator control register to establish the ADC sample rate to be used during test-signal acquisition. For optimal calibration effectiveness when clocking the inputs from a source other than the Rate-A generator, adjust the Rate-A generator control register to approximately the value that would produce the expected sample rate (Section 3.4.4).

3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.7.1)
b. The *PCI interrupt* must be enabled (Section 3.7.2).

A local interrupt request will not generate a PCI bus interrupt unless the PCI interrupt has been enabled as outlined in Paragraph 3.7.2.

3.7.1 Local Interrupt Request

The Interrupt Control Register shown in Table 3.7-1 controls the single local interrupt request line. Two simultaneous source conditions (IRQ 0 and1) are available for the request, with multiple conditions available for each source. IRQ 0 and 1 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for either of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if a selected interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *Local Interrupt Input Enable* control bits HIGH in the *Runtime Interrupt Control/Status Register* described in Section 6 of the PLX^{TM} PCI-9056 reference manual.

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

Data Bit	Mode	Designation	Def	Value	Interrupt Event
D00-02	R/W	IRQ0 A0,1,2	0	0	Initialization completed.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4	Triggered burst initiated (BURST BUSY => HI)
				5	Triggered burst completed (BURST BUSY => LO)
				6-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	Input buffer overflow or underflow
				4-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

* HIGH after reset.

3.8 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master, in either DMA Channel 00 or Channel 01. Set bit D[02] in the PCI Command register HIGH to select the bus mastering mode. Also, clear D[15] LOW in the PCI-9056 DMA Mode register to select *slow-terminate* operation. Refer to the PCI-9056 reference manual for a detailed description of DMA configuration registers.

3.8.1 Block Mode

Table 3.8-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	(Note 2)
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

3.8.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.8-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

When operating in demand mode, DMA data transfer from the input buffer is requested continuously by the local controller as long as the buffer contains data.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained in the buffer until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

3.9 Auxiliary External Clock and Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking and burst triggering to external events. These bidirectional TTL connections are available as AUX CLOCK and AUX SYNC (Table 2.2-2), and when active *as inputs*, replace the corresponding external CLOCK I/O and SYNC I/O inputs in the system I/O connector. The AUX I/O signals are accessible through a 6-Pin connector on the back (Side-2) of the board.

AUX clock and sync signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.9-1. When an AUX signal is designated as an ***input***, the signal replaces the corresponding CLOCK I/O or SYNC IO input from the system connector. In order for the input to be acknowledged, ***target mode*** must be selected in the corresponding clock or sync control field in the Scan and Sync control register (Table 3.4-2). The AUX I/O pins are pulled up internally to +3.3VDC through 4.7K.

Active AUX ***outputs*** produce an output pulse for each internal ADC sample clock or burst trigger, and are active in both target and initiator clock and sync modes.

AUX *inputs* are edge-detected as LOW-to-HIGH transitions if the INVERT INPUTS control bit is LOW, or as HIGH-to-LOW transitions if the bit is HIGH. Minimum HIGH and LOW level durations are 100ns if the NOISE SUPPRESSION control bit is LOW, or 1.5us if the bit is HIGH. AUX *output pulses* are positive (i.e.: baseline level is LOW) if the INVERT OUTPUTS control bit is LOW, or negative (baseline HIGH) if the control bit is HIGH. Output pulse width is typically 130ns if the NOISE SUPPRESSION control bit is LOW, or 2.0us if the bit is HIGH.

To increase the reliability of external triggering in high-noise environments, selectable noise suppression increases the debounce or detection interval for active inputs, and increases the pulse width of active outputs.

Table 3.9-1. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 1.5us, and output pulse width is 2.0us.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as the AUX CLOCK I/O control mode.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10-1) contains the existing firmware revision, and a status field that indicates the configuration of optional features.

Table 3.10-1. Board Configuration Register

Offset: 0000 0028h **Default: 000X XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12-D14	(Reserved status flags or revision field).
D15	Product Identification flag: High indicates PMC66-18AI32SSC1M
D16-D17	Channel Availability: 0 => 32 Channels 1 => 16 Channels 2 => 8 Channels 3 => 4 Channels
D18	Master Clock Frequency: 0 => 36 MHz 1 => (Reserved)
D19	Input Range Set: 0 => High Range Set: ±10V, ±5V. 1 => Low Range Set: ±2.5V, ±1.25V.
D20	High for native 18-Bit board; Low for 16-Bit board.
D21-D31	(Reserved)

3.11 Data Packing (16-Bit Data only)

For 16-Bit native data, or if 16-Bit data is selected for a board configured in the 18-Bit native format, data packing enables the entire 32-Bit local bus to be used to convey data to the PCI bus. Setting the ENABLE DATA PACKING control bit high in the BCR selects the data packing mode, in which two consecutive 16-bit data values are packed into a single 32-Bit local data longword. In the data packing mode, a 32-bit scan marker code is inserted directly before each Channel-00 data value in the buffer (or immediately before the 'first channel' if the active channels are user-defined (3.4.2.2). ***The scan marker can be disabled by setting the DISABLE SCAN MARKER control bit HIGH in the BCR.***

Table 3.11-1. 16-Bit Data Packing

	Buffer Data Field					
	ENABLE DATA PACKING = 0 DISABLE SCAN MARKER = X		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 0		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 1	
Buffer Lword Order	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**
00	8000h	Chan 00 Data	Upper Marker	Lower Marker	Chan 01 Data	Chan 00 Data
01	0000h	Chan 01 Data	Chan 01 Data	Chan 00 Data	Chan 03 Data	Chan 02 Data
02	0000h	Chan 02 Data	Chan 03 Data	Chan 02 Data	Chan 05 Data	Chan 04 Data
03	0000h	Chan 03 Data	Chan 05 Data	Chan 04 Data	Chan 07 Data	Chan 06 Data
---	---	---	---	---	---	---

The scan marker code is defined by the 'Scan Marker Upper Word' and 'Scan Marker Lower Word' registers listed in Table 3.1-1, and is inserted immediately before the first value in each data scan as shown in Table 3.11-1. The lower 16 bits in each register contains one word of the code. The upper 16 bits of these registers are ignored, and should be written as all-zero.

Some applications may require the scan marker code to be absolutely unique and not appear randomly in the data. To support this requirement, an all-zero marker code (0000 0000h) causes every all-zero data value (0000h) to be forced to a unit code (0001h) when data packing is enabled. This arrangement supports the uniqueness requirement without affecting the differential nonlinearity of the data itself.

NOTE: If the number of active channels is odd-numbered while data packing is enabled, an all-zero data value is inserted directly after the last active channel value. Like all other all-zero data values, the inserted value is forced to a unit code if an all-zero marker is in effect and scan marking is enabled.

3.12 Triggered Bursts

The BURST ON SYNC control field in the Scan and Sync control register (Table 3.4-2) controls the triggering mode for acquisition bursts. Bursting is disabled if this field is zero. For all nonzero values, a sync event, *or trigger*, initiates a **burst** of internal sample clocks, each of which produces a sample of all active channels.

NOTE: The logic polarities of the external clock and sync I/O pins can be inverted by setting the INVERT CLOCK AND SYNC I/O control bit HIGH in the Scan and Sync control register (Paragraph 2.3.2 and Table 3.4-2). This inversion does not affect the Auxiliary Sync logic polarities selected in Table 3.9-1.

3.12.1 Burst Size and Trigger Source

The number of sample clocks issued during a burst is controlled by the 20-bit **Burst Size control register** listed in Table 3.1-1, which has a range from 1 to 1,048,575 sample clocks. For Burst-Size values of one or greater, the number of sample clocks in a burst equals the value in the register. For example, if a burst size of 10 is selected while 16 channels are active, then each burst will contain 160 sample values. Selection of the burst trigger source is summarized in Table 3.12-1. A Burst-Size of zero produces a burst that extends continuously until stopped, either by disabling the internal clock or by clearing the BURST ON SYNC control field.

The Sync I/O pin in the system I/O connector can operate as an input or output trigger pin. The trigger output can serve as a burst trigger for target boards in which the BURST ON SYNC control field selects the external Sync I/O pin as a trigger source.

NOTE: During a triggered burst the BURST BUSY status flag in the Scan and Sync control register goes HIGH at the trigger event, and returns LOW at the end of the burst. Either edge of the BURST BUSY flag is selectable as an interrupt event (Table 3.7-1).

Table 3.12-1. Burst Trigger Source

Scan and Sync Register BURST ON SYNC	Burst Trigger Source	Sync I/O Pin
0	Bursting disabled.	Input (Disabled)
1	Rate-B generator.	Trigger Output
2	External Sync I/O input pin (or AUX input)	Trigger Input (Target mode)
3	INPUT SYNC control bit in the BCR.	Trigger Output

3.12.2 Sample Clock Source

When operating in the triggered-burst mode, the sample-clock source is selected by the SAMPLE CLOCK SOURCE field in the Scan and Sync control register.

The following sequence illustrates the setup for a typical burst operation, and assumes that ADC clocking is disabled:

1. Select the input range, sample-clock source and burst size, with clocking disabled,
2. Use Table 3.12-1 to select the burst trigger source (enables burst triggering),
3. Load and enable the associated rate generators, if required,
4. Clear the input buffer,
5. Enable ADC sampling by setting the ENABLE CLOCKING control bit HIGH in the Scan and Sync control register.

NOTE: ADC sampling, or clocking, is disabled while the ENABLE CLOCKING control bit in the Scan and Sync control register is in the default LOW state. Sampling commences when this bit is set HIGH.

3.12.3 Pretriggering (Firmware Revision-004 and higher)

If the ENABLE PRETRIGGERING control bit is set HIGH in the Scan and Sync control register, data is acquired before a trigger occurs, and the 48-bit Pretrigger Counter (Table 3.1-1) accumulates the number of Longword values stored in the buffer before the trigger. The pretrigger counter is cleared either by clearing the data buffer or by initialization. The LATCHED TRIGGER status flag is set by a trigger event, and is cleared either (a) directly, (b) by clearing the buffer, or (c) by deasserting the ENABLE PRETRIGGERING control bit.

When a trigger occurs, the Pretrigger Counter stops incrementing and retains the total number of longword values stored in the buffer after the buffer was last cleared, and before the trigger occurred. The pretrigger count includes scan markers if scan markers are enabled (3.11). The trigger condition is sampled with each ADC sample, and a detected trigger event indicates that the *previous sample* was the last pretrigger sample.

The pretrigger counter is double-buffered in order to avoid ambiguous states when its value is changing. However, since two bus transactions are required to read the entire 48-Bit pretrigger counter, reading the counter before the LATCHED TRIGGER flag is asserted is not recommended. After the buffer is cleared, acquisition commences on a scan boundary, with the lowest active channel appearing first in the buffer.

At the end of a triggered burst:

- The Pretrigger Counter contains the number of pretrigger Lword values stored after the data buffer was last cleared.
- The LATCHED TRIGGER flag remains asserted.
- The specified number of posttrigger samples has been acquired.
- Acquisition ceases and subsequent triggers are ignored until the sequence is reinitialized.

Clearing the buffer clears the LATCHED TRIGGER flag and pretrigger counter, and reinitializes the burst sequence by commencing accumulation of pretrigger data.

Due to delays in the ADC conversion process and to internal pipelining of input data, a delay occurs between the instant that a sample occurs and the appearance of associated data in the data buffer. To compensate for this effect, posting of the LATCHED TRIGGER flag is delayed until the last associated pretrigger data value enters the buffer.

Note: Operation of the pretriggering function has not been verified while running background autocalibration (3.14). Contact GSC if pretriggering is required during background autocalibration.

3.13 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance is suspended. Abrupt changes include:

- A change in voltage range or sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

3.14 Background Calibration (Firmware Revision-003 and higher)

At lower sample rates, the periodic interruption of data acquisition to perform autocalibration can be avoided by implementing Background Calibration. Background calibration maintains calibration continuously during data acquisition, and is invoked by setting the BACKGROUND CALIBRATION control bit HIGH in the BCR. When operating in this mode, calibration is performed continuously by switching the inputs of all channels continuously between the system inputs and the internal selftest signals. The settling times involved in this activity impose a limit of approximately 750SPS (samples per second) on the maximum practical effective sample rate. At sample rates above this limit, calibration errors and effective input noise will increase. However, in some applications involving low sample rates, the advantages of maintaining calibration during extended uninterrupted data acquisition can be significant.

NOTES; During Background Calibration:

(1) The effective sample rate is *one-half* the rate determined in Section 3.4. For example, if the sample rate source is the Rate-A generator, then the *effective* sample rate is:

Effective Fgen (Hz) = Fclk (Hz) / (2 * Nrate),

(2) The maximum practical effective sample rate is approximately 750SPS (Frate-A = 1.5kHz).

The settling time for calibration in this mode is approximately 2400 sample clocks, as measured from the initial selection of background calibration. This interval corresponds to 12 seconds for full 18-Bit calibration with a sample rate of 200SPS, four seconds at 600SPS, etc.

If autocalibration (3.6) is selected while operating in the background calibration mode, a normal autocalibration sequence will occur, followed by the resumption of background calibration.

3.15 External Clock Division (Firmware Revision-010 and higher)

By default, the external clock input can be used to directly clock the analog inputs, with each input pulse initiating a single conversion of all active channels (See Paragraph 3.4.5). However, to support high frequency external clocking sources, the frequency of the external clock input can be divided internally to the required sample rate.

If the ENA EXT CLK DIVISION control bit is set HIGH in the Scan and Sync control register (Table 3.4-2), the external clock input is routed through a 20-Bit divider and the divided frequency is used as the input sample clock. The external clock input frequency is divided by the value contained in the External Clock Divisor register listed in Table 3.1-1.

NOTE: To implement external clock division, the original selection requirements for the external clock are unchanged in the Scan and Sync control register, and the SAMPLE CLOCK SOURCE field must be zero. For example; from the default state after initialization, write the value 0000_0065h to the Scan and Sync control register.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of 32 differential analog input channels contains a dedicated 18-Bit or 16-Bit ADC, a selftest input switching network, and a differential input amplifier (Figure 4.1-1). A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller. +5 VDC power from the PCIbus is converted into regulated power voltages for the internal analog networks.

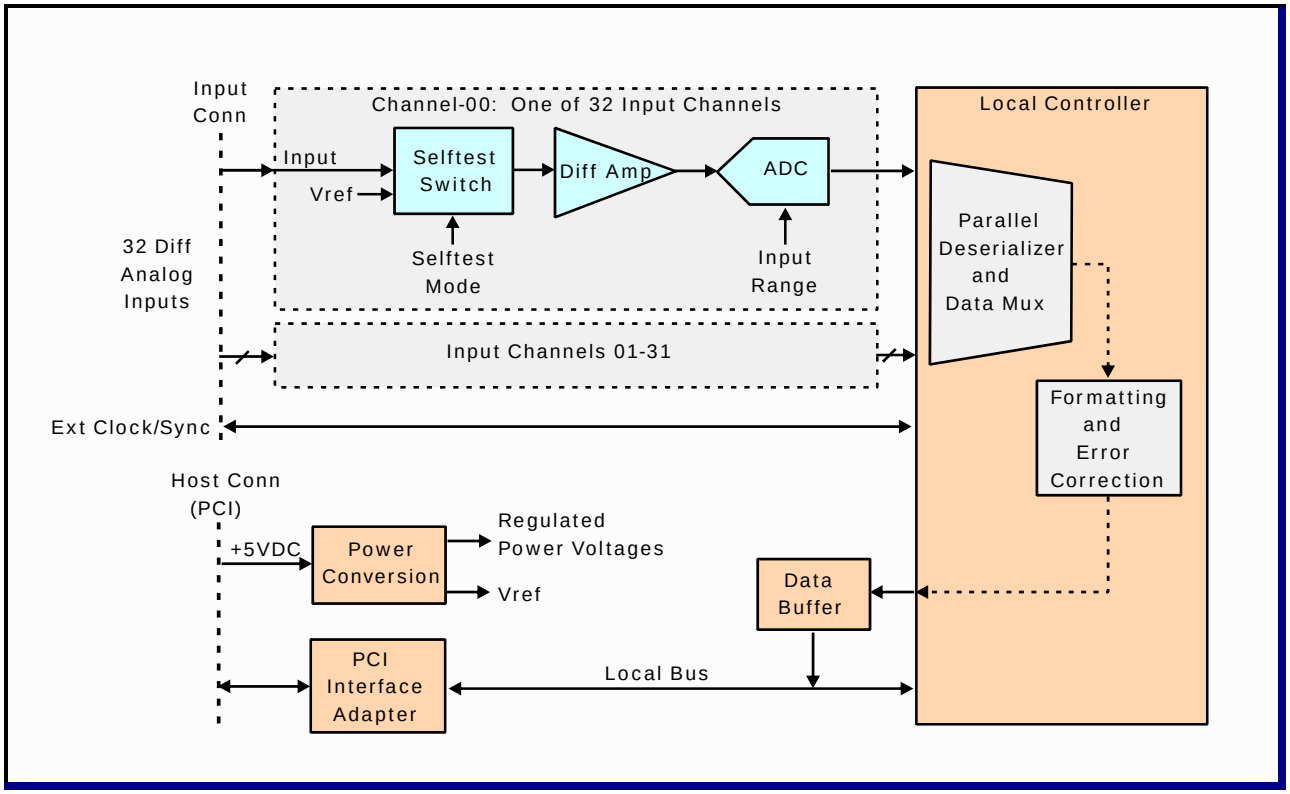

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input channels, and the input differential amplifier is biased to accept bipolar input ranges. The input range is controlled by adjusting the ADC reference voltage. Each input sample is corrected for gain and offset errors with calibration values determined during autocalibration. A 1-Megabyte FIFO buffer accumulates analog input data for subsequent retrieval by a PMC host.

Analog input sampling on multiple target boards can be synchronized to a single software-designated initiator board. An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, the ADC's receive system analog input signals from the input connector. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC. The input network in each channel provides the necessary offset parameters to support bipolar input ranges.

Serial data from all ADCs are deserialized simultaneously and then multiplexed into a parallel data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies the gain and offset correction values that are obtained during autocalibration. The corrected data is then formatted and loaded into the analog input data buffer.

The inputs can be acquired either continuously or in discrete bursts. Burst triggers can be obtained from various sources, including an external Sync input I/O pin or a 16-Bit divider driven by the internal master clock. The number of samples in a burst is controlled by a 20-Bit Burst Size register.

4.3 Rate Generators

The local controller contains two independent rate generators, each of which divides a master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a sample-clock or burst-trigger source for the analog inputs, and the generators can be cascaded to produce very long sampling or burst intervals.

4.4 Data Buffer

A 1M-Byte FIFO buffer accumulates analog input data for subsequent retrieval by the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by a threshold flag that can be used to generate an interrupt request when the number of values in the buffer moves above or below a selected count. Local data packing is supported for 16-bit data, and DMA transfers can be implemented in both block and demand modes.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the application software.

An internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample as it is acquired during acquisition, and are retained until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated supply voltages of ±5 VDC and ±15 VDC are required for internal analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

APPENDIX A

Local Control Register Quick Reference

APPENDIX A
Local Control Register Quick Reference

This appendix consolidates the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

Offset (Hex) [1]	Register	Access Mode [2]	Default	Primary Function
0000	BOARD CONTROL (BCR)	R/W	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	R/W	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	XXXX XXXXh	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	R/W	0001 02D0h	Rate-A generator freq selection
0014	RATE-B GENERATOR	R/W	0000 2000h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer
001C	BURST SIZE	R/W	0000 0001h	Number of sample clocks in a triggered burst.
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	ACTIVE CHANNEL ASSIGNMENT	R/W	0000 0100h	Specific first and last active channels.
0028	BOARD CONFIGURATION	RO	000X XXXXh	Firmware revision and option straps.
002C	Autocal Values [3]	R/W	0000 080Xh	Autocal value readback.
0030	Auxiliary R/W Register [3]	R/W	0000 0000h	Auxiliary register. For internal use only.
0034	AUXILIARY SYNC I/O CONTROL	R/W	0000 0000h	Controls auxiliary sync I/O port
0038	SCAN MARKER UPPER WORD	R/W	0000 0000h	Packed-data scan marker D[31..16].
003C	SCAN MARKER LOWER WORD	R/W	0000 0000h	Packed-data scan marker D[15..0].
0040	Test Utility Register [3]	R/W	0000 0000h	Maintenance utility register.
0044	PRETRIGGER COUNTER LOW	RO	0000 0000h	Pretrigger counter lower 32 bits D00-D31.
0048	PRETRIGGER COUNTER HIGH	RO	0000 0000h	Bits D00-D15 are 'Pretrigger Counter' high bits D32-D47.
004C-0050	(Reserved)	RO	0000 0000h	---
0054	EXTERNAL CLOCK DIVISOR	R/W	0000 0000h	External clock frequency divisor (3.15)
0058-007C	(Reserved)	RO	0000 0000h	---

[1] Offsets from the PCI base address for local addressing.

[2] R/W = Read/Write; RO = Read-Only.

[3] Maintenance register; Shown for reference only

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

Bit	Mode	Designation	Def	Description	Ref
D00-D02	R/W	AIM[2..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	(Reserved)	0	---	---
D04-D05	R/W	RANGE[1..0]	2h	Analog input range. Defaults to ±10V range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.	3.5.1.3
D07	R/W	(Reserved)	0h	---	---
D08	R/W	BACKGROUND CALIBRATION	0h	Selects background (continuous) autocal. Superseded by AUTOCAL. Maximum sample rate = 750SPS	3.14
D09-D10	R/W	(Reserved)	0h	---	---
D11	R/W	DISABLE SCAN MARKER	0	Disables the scan marker in data packing mode.	3.11
D12	R/W	*INPUT SYNC	0	Produces a single ADC clock when selected in the Scan and Sync Control Register, or a single burst trigger when selected with the Burst On Sync control field.	3.4.3 3.12.1
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal completion confirms a successful calibration.	
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.11
D19-D31	RO	(Reserved)	0	---	---

* Clears automatically when the associated operation is completed.

Table 3.4-1. Analog Voltage Range Selection (BCR field)

	Analog Input Range Set *	
Range Select[1:0]	**High Range Set**	**Low Range Set**
0	(Reserved)	(Reserved)
1	±5 Volts	±1.25 Volts
2	±10 Volts	±2.5 Volts
3	±10 Volts	±2.5 Volts

* See Table 3.10-1 for input range options.

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

Bit	Mode	Designation	Def	Description
D00-D02	R/W	ACTIVE CHANNELS	5h	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 32 channels (00-31); Default value 6 => (Reserved) 7 => Channel group assignment (See Section 3.4.2.2) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	SAMPLE CLOCK SOURCE	0h	Selects the analog input sample clocking source and I/O mode: 0 => External Clock input line (Selects Clock TARGET mode) 1 => Internal Rate-A generator output 2 => Internal Rate-B generator output 3 => BCR Input Sync control bit.
D05	R/W	ENABLE CLOCKING	0	Enables the selected ADC clocking process
D06	R/W	ENA EXT CLK DIVISION	0	Enables internal frequency division of an external clock source (3.15)
D07	RO	BURST BUSY	0	Indicates that a triggered burst is in progress.
D08-D09	R/W	BURST ON SYNC	0h	Selects bursting trigger source and I/O mode (Section 3.12) 0 => Bursting disabled 1 => Rate-B generator 2 => External Sync-I/O input (Selects Sync TARGET mode) 3 => BCR Input Sync control bit.
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	INVERT CLOCK AND SYNC I/O	0	Inverts the logic polarities of external clock and sync I/O input and output signals to assert HIGH.
D12-17	R/W	SINGLE-CHANNEL SELECT	0h	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	ENABLE PRETRIGGERING	0	Enables the pretriggering mode and the 'Latched Trigger' status flag.
D19	R/W	LATCHED TRIGGER	0	Records a trigger event when pretriggering is enabled. Cleared by direct write, by clearing the buffer, or by disabling pretriggering.
D20-D31	RO	(Reserved)	0	Inactive

Table 3.4-3. Active Channel Assignment

Offset: 0000 0024h **Default: 0000 0100h**

Data Bit	Mode	Designation	Default	Description
D00-D07	R/W	FIRST CHANNEL SELECT	0	First (lowest-numbered) active channel
D08-D15	R/W	LAST CHANNEL SELECT	1	Last (highest-numbered) active channel
D16-D31	RO	(Reserved)	0	Inactive. Returns all-zero.

Table 3.4-4. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 02D0h (Rate-A), 0000 2000h (Rate-B)**

Data Bit	Mode	Designation	Default	Description
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

Table 3.4-5. Rate Generator Frequency Selection

Nrate (RATE[15..0])		Fgen (36 MHz Master Clock)
(Dec)	(Hex)	(Hz)
36	24	1,000,000
37	25	972,973
---	---	Fgen (Hz) = 36,000,000 / Nrate

* ±0.005 percent.

Table 3.5-1. Input Data Buffer; Nonpacked Data

Offset: 0008h **Default: N/A**

Native Data Width	Selected Data Width	Channel-00 Tag	Reserved * (Zero)	Channel Data Value
18 Bits	18 Bits	D[31]	D[30..18]	D[17..0]
	16 Bits	D[31]	D[30..16]	D[15..0]
16 Bits	---	D[31]	D[30..16]	D[15..0]

All fields are read-only; Write-data is ignored. *** Sign-extension in two's complement coding mode *for 18-Bit data only*.**

Table 3.5-2. Input Data Coding

	Digital Value (Hex)			
	Offset Binary		Two's Complement	
Analog Input Level	18-Bit Data	16-Bit Data	18-Bit Data	16-Bit Data
Positive Full Scale minus 1 LSB	0003 FFFF	0000 FFFF	0001 FFFF	0000 7FFF
Zero (Midscale)	0002 0000	0000 8000	0000 0000	0000 0000
Zero minus 1 LSB	0001 FFFF	0000 7FFF	0003 FFFF	0000 FFFF
Negative Full Scale	0000 0000	0000 0000	0002 0000	0000 8000

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

Data Bit	Mode	Designation	Def	Description
D00-D17	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D20	R/W	SELECT 18 BIT DATA	0	Selects the 18-Bit data width when HIGH, or 16-Bit width when LOW. Ignored in the native 16-Bit configuration
D21-D31	RO	(Inactive)	0	---

*Clears automatically within 200ns of being set

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

Data Bit	Mode	Designation	Def	Description
D00-D18	RO	BUFFER SIZE	00000h	Number of locations occupied in the input buffer
D19-D31	RO	(Inactive)	0	---

Table 3.5-5. Analog Input Function Selection (BCR field)

AIM[2:0]	Function or Mode
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

Data Bit	Mode	Designation	Def	Value	Interrupt Event
D00-02	R/W	IRQ0 A0,1,2	0	0	Initialization completed.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4	Triggered burst initiated (BURST BUSY => HI)
				5	Triggered burst completed (BURST BUSY => LO)
				6-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	Input buffer overflow or underflow
				4-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	(Note 2)
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

Table 3.9-1. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 1.5us, and output pulse width is 2.0us.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as the AUX CLOCK I/O control mode.

Table 3.10-1. Board Configuration Register

Offset: 0000 0028h **Default: 000X XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12-D14	(Reserved status flags or revision field).
D15	Product Identification flag: High indicates PMC66-18AI32SSC1M
D16-D17	Channel Availability: 0 => 32 Channels 1 => 16 Channels 2 => 8 Channels 3 => 4 Channels
D18	Master Clock Frequency: 0 => 36 MHz 1 => (Reserved)
D19	Input Range Set: 0 => High Range Set: ±10V, ±5V. 1 => Low Range Set: ±2.5V, ±1.25V.
D20	High for native 18-Bit board; Low for 16-Bit board.
D21-D31	(Reserved)

Table 3.11-1. Data Packing

	Buffer Data Field					
	ENABLE DATA PACKING = 0 DISABLE SCAN MARKER = X		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 0		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 1	
Buffer Lword Order	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**
00	8000h	Chan 00 Data	Upper Marker	Lower Marker	Chan 01 Data	Chan 00 Data
01	0000h	Chan 01 Data	Chan 01 Data	Chan 00 Data	Chan 03 Data	Chan 02 Data
02	0000h	Chan 02 Data	Chan 03 Data	Chan 02 Data	Chan 05 Data	Chan 04 Data
03	0000h	Chan 03 Data	Chan 05 Data	Chan 04 Data	Chan 07 Data	Chan 06 Data
---	---	---	---	---	---	---

Table 3.12-1. Burst Trigger Source

Scan and Sync Register BURST ON SYNC	Burst Trigger Source	Sync I/O Pin
0	Bursting disabled.	Input (Disabled)
1	Rate-B generator.	Trigger Output
2	External Sync I/O input pin (or AUX input)	Trigger Input (Target mode)
3	INPUT SYNC control bit in the BCR.	Trigger Output

APPENDIX B

Migration From CCPMC66-16AI32SSA

Appendix B

Migration From CCPMC-16AI32SSA

Operation of the PMC66-18AI32SSC1M is similar to that of the CCPMC66-16AI32SSA. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 provides a brief comparison of CCPMC66-16AI32SSA and PMC66-18AI32SSC1M features.

Table B.1. CCPMC66-16AI32SSA, PMC66-18AI32SSC1M Features Comparison

Feature	CCPMC66-16AI32SSA	PMC66-18AI32SSC1M
Number of Input Channels	**32**	**32**
Native Input Configuration	**Differential**	**Differential**
Input Ranges	**±2.5V, ±1.25V and ±0.625V**	**±10V and ±5V**
Input Impedance	**Intermediate (70K-150K-Ohms)**	**High (1-2 Megohms)**
Form Factor	**Conduction-cooled PMC with P4 I/O**	**Air-cooled PMC with front-panel I/O**
Local Clock	**40 MHz**	**36 MHz**
Native Resolution	16 Bits	18 or 16 Bits
Data Buffer	1M-Byte FIFO	1M-Byte FIFO
Buffer Data Field	32 Active bits	32 Active bits
PCI Interface	PCI 2.3; D32; 33MHz/66MHz	PCI 2.3; D32; 33MHz/66MHz

B.2. Migration Issues

Section 2.0. Installation and Maintenance:

I/O pin assignments have changed.

Paragraph 3.1. Control and Data Registers:

Local addressing has been extended from 16 Lwords to 64 Lwords.

Table 3.1-1. Control and Data Registers:

The BCR and Rate-A/B Generator control register default values have changed.

Table 3.2-1: Board Control Register:

Redundant-function control bit D07, ENABLE EXTERNAL SYNC, is now a reserved bit.
Unused AUTONOMOUS DEMAND MODE control bit D19, is now a reserved bit.
The default value has changed.
Background calibration controls have been added.

Paragraph 3.4-1. Input Voltage Range:

Input voltage ranges have been revised to ±10V and ±5V.

B.2. Migration Issues (Continued)

Table 3.4-2: Clock and Sync Control Register:

Reserved bit D05 has been redesignated as ENABLE CLOCKING.
Reserved bit D11 has been redesignated as INVERT CLOCK AND SYNC.

Paragraph 3.4.4.2. Rate Generator Frequency Control:

The default master clock frequency has changed from 40 MHz to 36 MHz.

Paragraph 3.5.1. Input Data Organization:

The buffer data format has been modified to support 18-Bit data..

Paragraph 3.8.2. Demand Mode (DMA):

The now-obsolete threshold-driven demand mode DMA has been eliminated.

Table 3.10-1. Board Configuration Register:

The board configuration register has been modified to conform to applicable production options.

Paragraph 3.14. Background Calibration:

New feature permits continuous autocalibration at lower sample rates.

Paragraph 3.15. External Clock Division (FW-010 and higher):

New feature permits internal division of an external clock frequency as a sample clock.

Production Revision History:

07-18-2008:	Paragraph 1.1:	Updated general description.
09-15-2008,	Table 3.2-1:	Background calibration controls D08, D09.
01-15-2009:	Table 3.7-1:	Background calibration sample rate limit interrupt event.
	Paragraph 3.14:	Background calibration description.
03-11-2009:	Tables 3.4-1, 3.10-1:	Low-range input option.
03-25-2009:	Tables 3.1-1, 3.4-1:	Added pretrigger counter and controls.
	Paragraph 3.12.3:	Added pretriggering description.
05-17-2009:	Table 3.2-1:	Deleted status flag BCR D09.
	Table 3.7-1:	Deleted IRQ0-6 interrupt event.
	Paragraph 3.14:	Removed reference to status flag BCR D09.
	Table 2.5.2:	Added ±2.5V range.
06-05-2009:	Table 3.1-1:	Corrected typos.
03-25-2010:	Paragraph 3.12.3:	Clarified 'Latched Trigger' flag at end of burst.
04-26-2012:	Tables 3.1.1, 3.4-2:	Added Ext Clk Division controls.
	Paragraph 3.15:	Added new feature; "External clock Divisor" (FW-010 and higher).
04-26-2012:	Tables 3.1.1, 3.4-2:	Added Ext Clk Division controls.
07-10-2012:	Figure 2.3-1:	Updated illustration.
10-31-2013:	Paragraph 2.3.2.2:	Clarified minimum input pulse widths.
	Paragraph 3.14:	Updated the effective firmware revision.
05-29-2014:	Paragraph 2.5.2:	Revised connector reference.

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