General Standards Corporation

High Performance Bus Interface Solutions

Rev: 040412

cPCI6U64-20AOF16C500KR

20-Bit Sixteen-Output 500KSPS
Precision Wideband cPCI Analog Output Board

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

The CPCI6U64-20AOF16C500KR is a precision 20-Bit analog output Compact PCI 6U module that provides sixteen simultaneously clocked output channels (Figures 1-1 and 1-2). The outputs can be clocked synchronously or independently at rates up to 500 KSPS per channel, and are supported by a 256K-Sample FIFO data buffer. Both continuous and burst clocking modes are supported, and the output ranges are software-selectable as ±6V and ±3V, or optionally as ±10V and ±5V. Clocking and triggering rates can be derived from internal rate generators, or from external clock and trigger sources to support the synchronous operation of multiple boards.

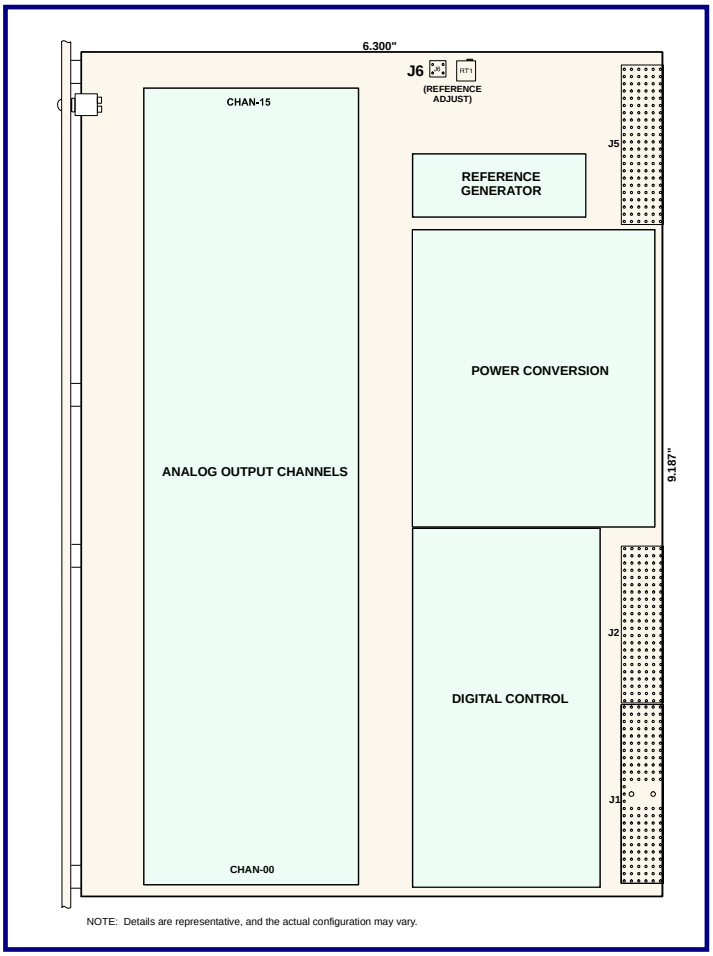

Figure 1-1. Physical Configuration

The analog outputs implement an R-2R DAC in each channel, which minimizes latency and has no minimum clocking rate. The outputs can be factory-configured for either single-ended or 3-wire differential operation.

On-demand autocalibration determines and applies error correction for all analog output channels. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

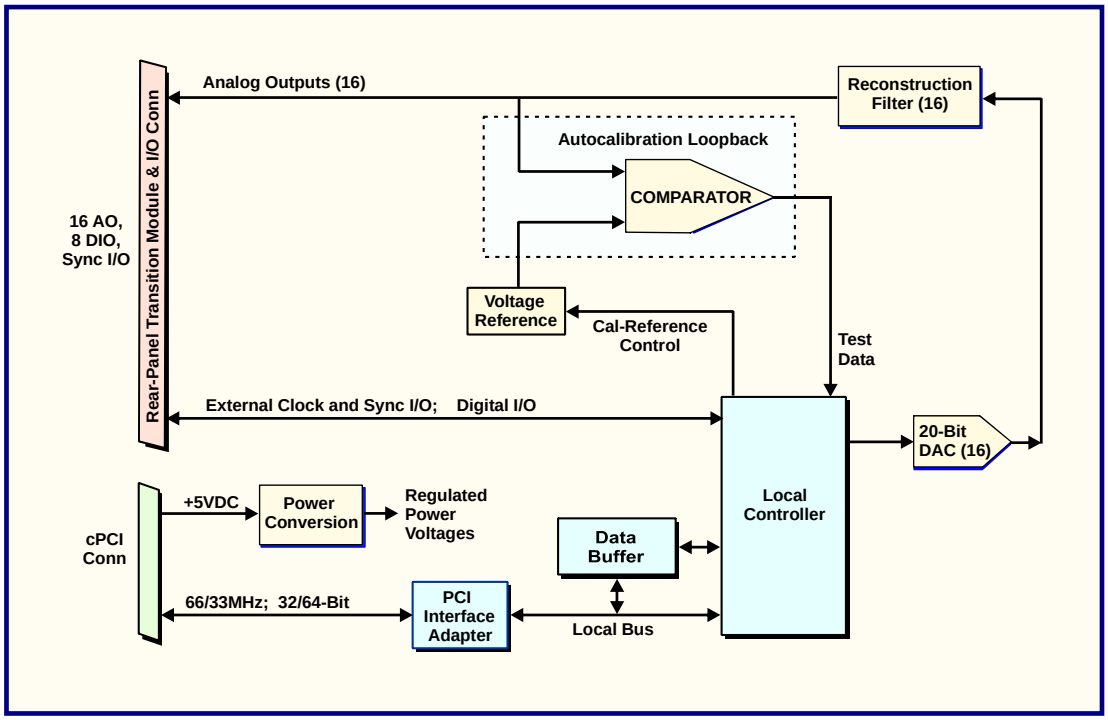

Figure 1-2. Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the rear panel through a transition module. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable electrical or mechanical features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the module should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the module from the conductive shipping envelope, ensure that the work surface, the installer and the host equipment have been properly discharged to ground.

Before removing the board from the protective shipping envelope, select an empty 6U expansion slot in the host computer and, if a blank panel is located in the slot position, remove the panel. Then remove the board from the shipping container and insert the board into the allocated expansion slot, carefully pressing the board firmly to seat the rear-panel connectors. Secure the panel latches to complete the installation.

2.2.2 Input/Output Cable Connections

System input/output connections are made at the rear panel of companion rear transition module cPCI6U64-20AOF16C500KTM, through FP-P1, P2 and P3, as shown in Figure 2.2-1. Unused pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, unused inputs should be grounded to the input return to minimize the injection of noise into the board.

System cable signal pin assignments are listed in Tables 2.2-1 and 2.2-2. Refer to the product specification for information pertaining to system input/output cable mating connector part numbers. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connectors (50-Pin D-Sub)

	RP-P1		RP-P2
Pin	Function	Pin	Function
1	OUT CH 00 HI [1]	1	OUT CH 10 HI [1]
34	OUT CH 00 LO [1]	34	OUT CH 10 LO [1]
18	OUT RTN	18	OUT RTN
2	OUT RTN	2	OUT RTN
35	OUT CH 01 HI	35	OUT CH 11 HI
19	OUT CH 01 LO	19	OUT CH 11 LO
3	OUT RTN	3	OUT RTN
36	OUT RTN	36	OUT RTN
20	OUT CH 02 HI	20	OUT CH 12 HI
4	OUT CH 02 LO	4	OUT CH 12 LO
37	OUT RTN	37	OUT RTN
21	OUT RTN	21	OUT RTN
5	OUT CH 03 HI	5	OUT CH 13 HI
38	OUT CH 03 LO	38	OUT CH 13 LO
22	OUT RTN	22	OUT RTN
6	OUT RTN	6	OUT RTN
39	OUT CH 04 HI	39	OUT CH 14 HI
23	OUT CH 04 LO	23	OUT CH 14 LO
7	OUT RTN	7	OUT RTN
40	OUT RTN	40	OUT RTN
24	OUT CH 05 HI	24	OUT CH 15 HI
8	OUT CH 05 LO	8	OUT CH 15 LO
41	OUT RTN	41	OUT RTN
25	OUT RTN	25	OUT RTN
9	OUT CH 06 HI	9	OUT RTN
42	OUT CH 06 LO	42	OUT RTN
26	OUT RTN	26	OUT RTN
10	OUT RTN	10	OUT RTN
43	OUT CH 07 HI	43	OUT RTN
27	OUT CH 07 LO	27	OUT RTN
11	OUT RTN	11	OUT RTN
44	OUT RTN	44	OUT RTN
28	OUT CH 08 HI	28	OUT RTN
12	OUT CH 08 LO	12	OUT RTN
45	OUT RTN	45	OUT RTN
29	OUT RTN	29	OUT RTN
13	OUT CH 09 HI	13	OUT RTN
46	OUT CH 09 LO	46	OUT_RTN
30	OUT RTN	30	OUT RTN
14	REM GND SENSE [2]	14	OUT RTN
47	OUT RTN	47	OUT RTN
31	DIGITAL GND	31	DIGITAL GND
15	DIO 00	15	DIO 04
48	DIGITAL GND	48	DIGITAL GND
32	DIO 01	32	DIO 05
16	DIGITAL GND	16	DIGITAL GND
49	DIO 02	49	DIO 06
33	DIGITAL GND	33	DIGITAL GND
17	DIO 03	17	DIO 07
50	DIGITAL GND	50	DIGITAL GND

[1] In single-ended mode, 'HI' indicates signal, and 'LO' indicates no-connect.

[2] Active for single-ended configurations only.

Table 2.2-2. Sync I/O Connector RP-P3 (15-Pin D-Sub)

Pin	Signal
1	EXT SYNC INPUT HI
9	EXT SYNC INPUT LO
2	DIGITAL GND
10	DIGITAL GND
3	EXT CLK INPUT HI
11	EXT CLK INPUT LO
4	DIGITAL GND
12	DIGITAL GND
5	EXT SYNC OUT HI
13	EXT SYNC OUT LO
6	DIGITAL GND
14	DIGITAL GND
7	EXT CLK OUT HI
15	EXT CLK OUT LO
8	DIGITAL GND

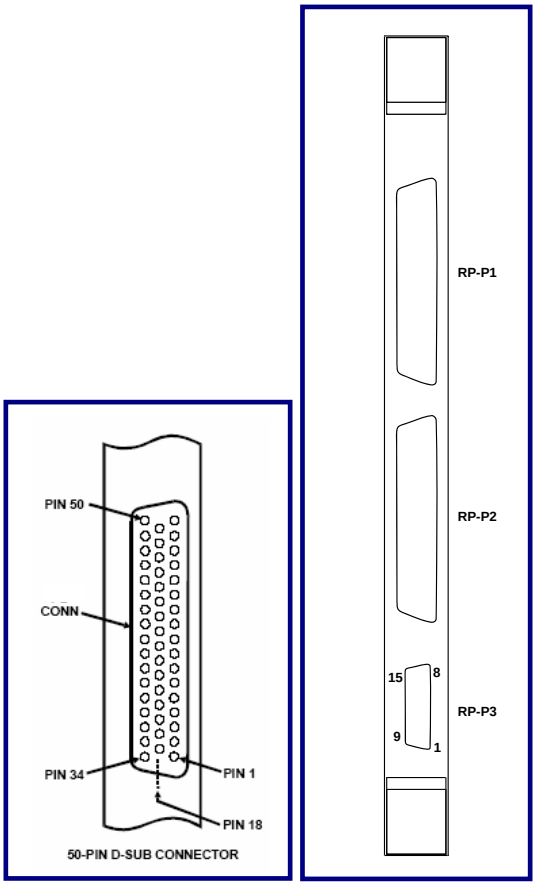

Figure 2.2-1. System I/O Connectors

2.3 System Configuration

2.3.1 Analog Outputs

2.3.1.1 Output Configurations

The sixteen analog output channels can be factored-configured either as 3-wire balanced differential outputs or as single-ended outputs.

Balanced differential outputs (Figure 2.3-1a) provide the highest immunity to system noise and interference, and are recommended for systems in which the loads will accept differential inputs. Each of the HI and LO outputs carries one-half of the output signal, with the two halves operating as complementary signals of equal amplitude and opposite polarity. Since radiated interference usually affects both output lines essentially equally, the coupled interference appears as a common mode signal which will be rejected in a differential load.

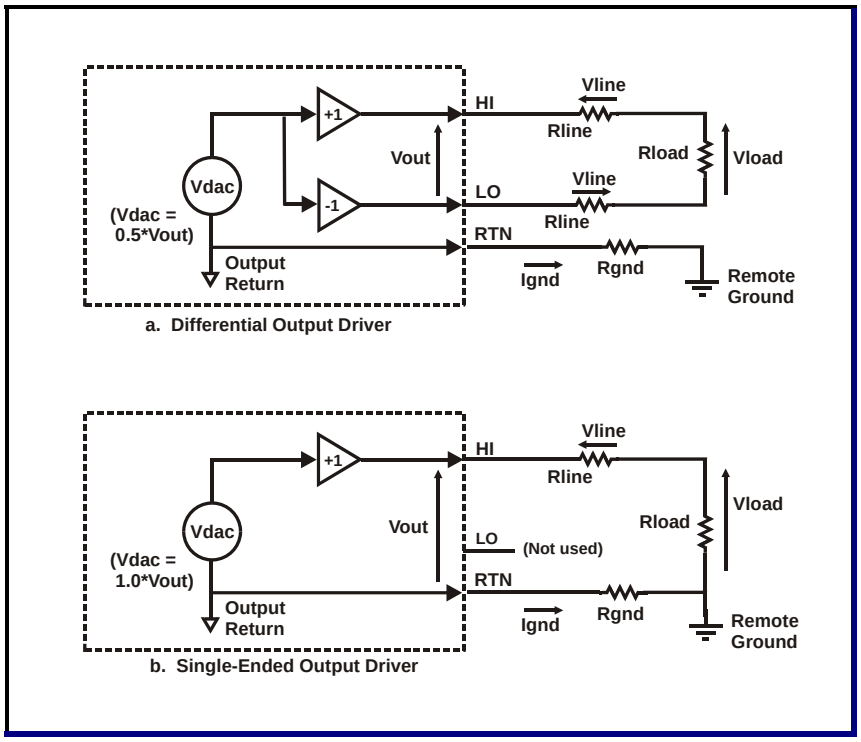

Figure 2.3-1. Output Configurations

For applications requiring single-ended outputs (Figure 2.3-1b), the output signal from each channel appears on the associated 'HI' output pin, and is generated with reference to the output return pin. The 'LO' pin may contain an indeterminate high-impedance signal, and can be either left disconnected or grounded, In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other

NOTE: For single-ended outputs, the REM GND SENSE line can be connected to the remote ground to minimize the effect of voltage drops in the return lines.

2.3.1.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate or heavy loads. Figure 2.3-2 shows the effect of load current on the voltage drop in copper wire of various sizes. A 4.0 milliamp load for example, inserts a voltage drop of more than 0.25 millivolt *per foot* in #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors with milliamp loads, especially in a 20-bit system, in which 1 LSB represents only 19 microvolts on a ±10 Volt range.

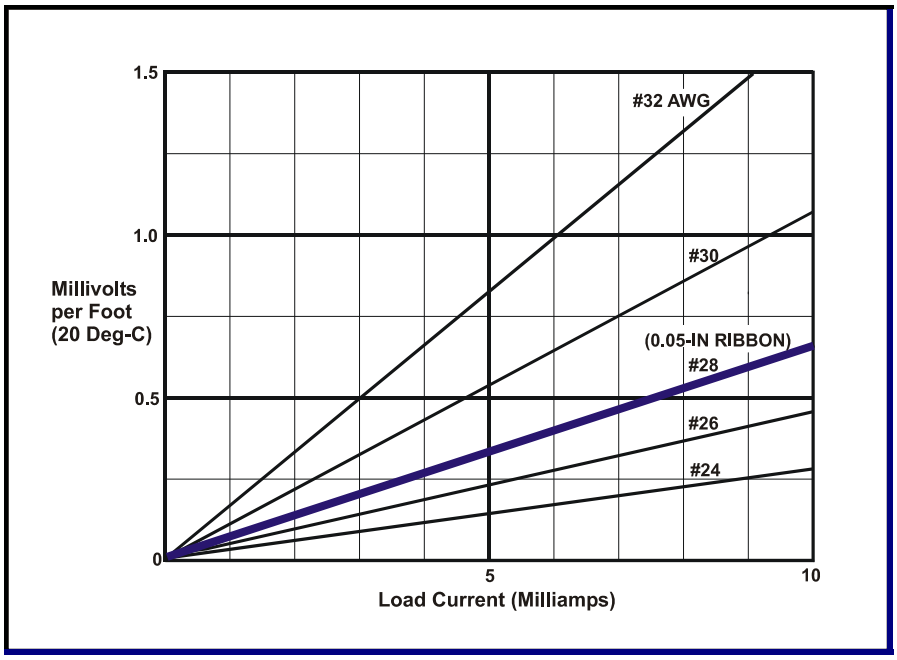

Figure 2.3-2. Line Loss versus Load Current

2.3.2 Multiboard Synchronization

If multiple boards are to be synchronized together, the input and output clock and/or sync (trigger) lines can be interconnected between boards in either a 'multidrop' configuration (Figure 2.3-3), or in a daisy-chained sequence (Figure 2.3-4). The multidrop arrangement eliminates the approximately 100ns delay incurred when passing through each board in a daisy-chain sequence, but limits the number of target boards to one LVDS load unless an LVDS buffer is implemented, or approximately four boards if TTL levels will be used. The number of target boards in a daisy-chain sequence is limited essentially only by the number of slots available in a backplane and the maximum acceptable total delay through the targets. Selection of LVDS or TTL logic levels is controlled by the associated application software.

The board that initiates the clock and trigger (sync) signals is software-designated as the **initiator**, and the clock and sync (trigger) receivers are designated as **targets**. For optimum reliability, the initiator and all targets all should reside in the same backplane. ***LVDS signaling can extend the I/O signals beyond a single backplane, but is limited to the daisy-chain configuration.***

NOTE: The terms 'Trigger' and 'Sync' are used essentially interchangeably throughout this document. 'Trigger" usually refers to an event that initiates a triggered burst, while 'Sync' refers to the logic signal itself.

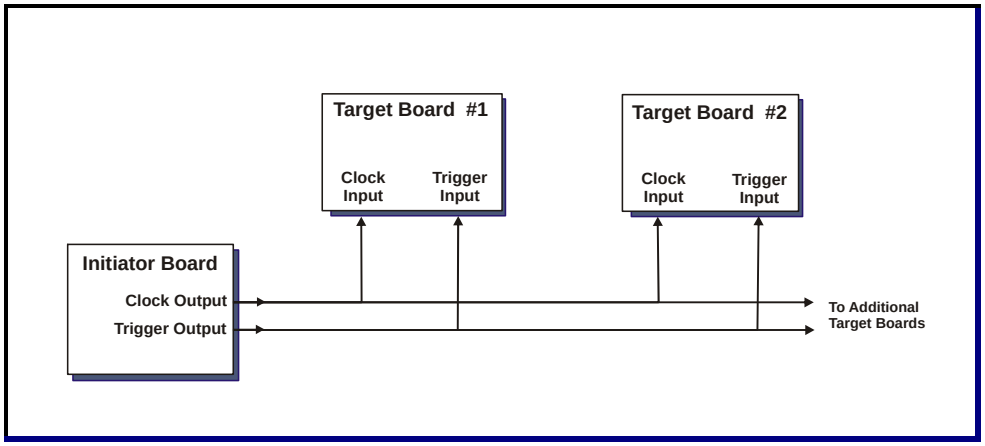

Figure 2.3-3. Multiboard Multidrop Synchronization

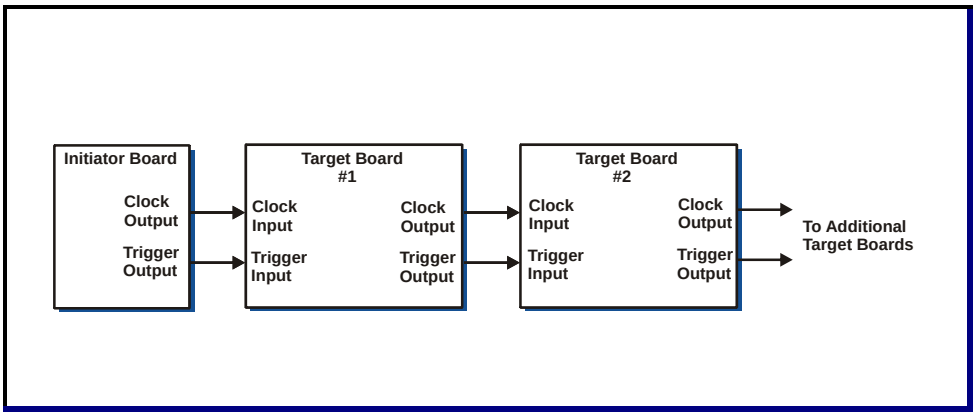

Figure 2.3-4. Multiboard Daisy-Chain Synchronization

2.3.3 External Sync I/O

An initiator (Paragraph 2.3.2) can be replaced with an external source of synchronization signals if the following conventions are observed:

- Input loading is 100 Ohms for LVDS inputs, or less than 0.2ma for TTL inputs. Maximum output loading is 75 Ohms for LVDS outputs, or 10mA for TTL outputs.
- Clocks and sync are edge-detected and are asserted LOW (i.e.: falling edge).
- Minimum input pulse width is 90ns.
- Minimum output pulse width is 110ns.

External devices can be synchronized to an initiator board by recognizing a clock or trigger event as either a TTL or LVDS pulse with a minimum width of 150ns.

2.4 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the range references. The optimum verification interval will vary with upon the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog channels are calibrated to a single internal voltage reference by an embedded autocalibration utility. The procedure presented here describes the verification and adjustment of the range references.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter, 5-1/2 digit, 0.002% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host system with available 6U cPCI slot	(Existing host)	---
Companion rear transition module cPCI6U64-20AOF16C500KTM	GSC	cPCI6U64-20AOF16C500KTM
Test cable; suitable for connecting the digital multimeter to the J6 test connector (Figure 1-1).	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of a single internal reference voltage. Adjustment of the reference, if necessary, is performed with a single trimmer that is located adjacent to the reference test connector J6, as shown in Figure 1-1.

This procedure assumes that the board under test is installed in an operational 6U cPCI host.

1. Connect the digital multimeter between Pins 1(+) and 2(-) in the J6 test connector.
2. If power has been removed from the board, apply power now. Wait at least 15 minutes after power is applied before proceeding.
3. Select the highest output range.
4. For the installed output range listed in the Assembly Configuration register, verify that the voltage displayed by the multimeter conforms to the indicated Vcal Reference value listed in Table 2.5-2. If the reference does not conform to the value listed in the table, adjust the reference trimmer to obtain a nominal in-range value.
5. Reference verification and adjustment are completed. Remove all test connections.

Table 2.5-2. Reference Voltage

Output Range	Vcal Reference
±6V	+5.9400DC ±0.0006VDC
±10V	+9.9000VDC ±0.0008VDC

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The CPCI6U64-20AOF16C500KR is compatible with the PCI Local Bus specification Revision 2.3. A PLX™ PCI-9656 adapter controls the PCI interface, and supports 33/66MHz and 32/64-Bit transfers on the bus. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the cPCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All local data transfers are long-word D32. DMA access is supported for data transfers to the analog output data buffer. To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero), and maintenance registers should not be modified.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2208 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	0000 0X0Xh	Digital I/O port data.	3.12
0008-002C	(Reserved)	RO	0000 0000h	---	---
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register, Interrupts	3.15
0034	ASSEMBLY CONFIGURATION	RO	0XXX XXXXh	Options and firmware revision.	3.16
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1400h	Buffered Analog Outputs Control	3.4
0040	OUTPUT BUFFER THRESHOLD	RW	0003 FFFEh	Output buffer status flag threshold.	3.5.5
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.5.5
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.5
004C	RATE GENERATOR A	RW	0000 0200h	Rate-A generator divider; 24 bits.	3.11
0050	RATE GENERATOR B	RW	0000 3000h	Rate-B generator divider; 24 bits.	3.11
0054	OUTPUT CONFIGURATION	RW	0001 FFFFh	Analog output configuration.	3.4
0056-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

3.2 Board Control Register (BCR)

Most common board functions such as initialization and autocalibration are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Read-only status flags indicate the states of specific operational functions.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2208 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	RW	(Reserved)	0	---	---
D05	RW	DIFFERENTIAL SYNC IO	0	Selects LVDS external sync I/O levels when HIGH.	3.9
D06	RW	ENABLE REMOTE GND SENSE	0	Enables correction for remote ground potential (single-ended outputs only)	3.4.5
D07-D17	RW	(Reserved)	0	---	---
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.7
D19	RW	FRONT PANEL LED	1	Illuminates the front-panel LED when HIGH.	3.14
D20	RW	OUTPUT SW CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.7
D21	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog outputs.	3.11
D22	R/W	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for analog outputs.	3.11
D23	R/W	OUTPUT SW TRIGGER [2,3]	0	Output Burst S/W Trigger. See also Table 3.4-2.	3.8.2
D24	RW	ENABLE OUTPUT FILTERS	0	Activates the lowpass filters in all output channels.	3.4.6
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.5.3
D26-D27	RO	(Reserved)	0	---	---
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.13
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.13
D30	RO	(Reserved)	0	---	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a cPCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to cPCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked. (Paragraph 3.3.2).
- All analog output channels are active. (3.4.1).
- The highest available analog output range is selected. (3.4.2).
- Clock and trigger sources are internal. (3.7.1, 3.8.2),
- The analog output buffer is reset to empty. (3.5.5),
- Data coding is offset binary. (3.5.3).
- The Digital I/O port is configured as eight input lines. (3.12).
- The Front Panel LED indicator is ON. (3.14).
- Rate-A generator is adjusted to 96.000 kHz, and is disabled. (3.11).
- Rate-B generator is adjusted to 4 kHz, and is disabled. (3.11).
- Analog outputs are at midrange (zero).

3.4 Output Configuration

The 16 analog output channels are accessed through a dedicated 256 K-Sample analog output buffer. Once the outputs have been configured through the Output Configuration register (Table 3.4-1), output operations are controlled through the BCR and the Buffered Operations register (Table 3.4-2).

3.4.1 Channel Selection

An output channel is selected as *active* by setting the corresponding OUTPUT_XX selection bit HIGH in the Output Configuration register. A channel is deselected to the *inactive* state by clearing the corresponding selection bit.

An active *channel group* consists of a single set of output values for all active channels. Only active output channels receive data from the output buffer. A channel that is deselected to the inactive state retains the last value that was received while the channel was still active. During initialization, all channels are designated as active and are set to an approximately zero output level.

3.4.2 Voltage Range Selection

An output voltage range of ±6V or ±3V (or optionally ±10V or ±5V) is selected by the OUTPUT HIGH RANGE control field in the Output Configuration register. The highest available output range is selected by default, and all ***outputs initialize to midrange (zero)***.

For maximum accuracy, autocalibration should be performed after a new output range is selected.

Table 3.4-1. Output Configuration Register

Offset: 0054h **Default: 0001 FFFFh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	RW	OUTPUT 00	1	Analog Output Active Channel selection mask.	3.4.1
D01	RW	OUTPUT 01	1	HIGH to enable.	
D02	RW	OUTPUT 02	1		
D03	RW	OUTPUT 03	1		
D04	RW	OUTPUT 04	1		
D05	RW	OUTPUT 05	1		
D06	RW	OUTPUT 06	1		
D07	RW	OUTPUT 07	1		
D08	RW	OUTPUT 08	1		
D09	RW	OUTPUT 09	1		
D10	RW	OUTPUT 10	1		
D11	RW	OUTPUT 11	1		
D12	RW	OUTPUT 12	1		
D13	RW	OUTPUT 13	1		
D14	RW	OUTPUT 14	1		
D15	RW	OUTPUT 15	1		
D16	RW	OUTPUT HIGH RANGE	1	Analog Output Range: Installed Range = ±6V, ±3V: 0 => ±3V 1 => ±6V. Installed Range = ±10V, ±5V: 0 => ±5V 1 => ±10V	3.4.2
D17	RW	CLOCK AND TRIGGER OUT	0	Enables the Analog Output Clock and Trigger external outputs,	3.7.1 3.8.2
D18-D19	RW	CLOCK SOURCE	0	Analog Output clock source: 0 => Rate-A Generator. 1 => Rate-B Generator. 2 => Analog Output External Clock input 3 => (Reserved).	3.7.1
D20-D21	RW	TRIGGER SOURCE	0	Analog Output trigger source: 0 => Rate-B Generator. 1 => Rate-A Generator.. 2 => Analog Output External Trigger input 3 => (Reserved).	3.8.2
D22	RW	(Reserved)	0	---	---
D23	RW	INVERT EXT SYNC	0	Inverts the logic polarities of the external clock and trigger inputs and outputs.	3.7.1.1
D24-D31	RO	(Reserved)	0000h	---	---

Table 3.4-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000 1400h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	R/W	(Reserved)	0h	---	---
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.7
D06	RO	OUTPUT CLOCK READY	0	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.7
D07	R/W	OUTPUT SW CLOCK [1,3]	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.7
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.5.6
D09	R/W	LOAD REQUEST [1]	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.6.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.6.3
D11	R/W	CLEAR OUTPUT BUFFER [1]	0	Resets the output buffer to empty.	3.5.5
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.5.5
D13	RO	OUTPUT BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.5.5
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.5.5
D16	R/W	AO BUFFER OVERFLOW [2]	0	Set HIGH when data is written to a full buffer.	3.5.5
D17	R/W	FRAME OVERFLOW [2]	0	Set HIGH when data is written to a closed buffer.	3.6.3
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.8.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.8.2
D20	R/W	OUTPUT SW TRIGGER [1,3]	0	Produces a single output trigger event when asserted. Clears LOW automatically when the triggered burst is completed. Independent of triggering mode. Duplicated in the BCR.	3.8.2
D21-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

1. Clears LOW automatically when operation is completed.
2. Remains HIGH until cleared by a direct write as LOW, or by initialization.
3. Duplicated elsewhere.

3.4.3 Clock and Trigger Sources

The clock and trigger source fields determine the origins of the analog output clock and trigger functions, and are described later in Sections 3.7.1 and 3.8.2, respectively.

3.4.4 Hardware Configuration

The analog outputs are factory-configured for either 3-wire balanced-differential operation or as single-ended outputs, as indicated in the Assembly Configuration Register. System wiring must be compatible with the hardware configuration (Section 2.3.1.1).

3.4.5 Remote Ground Sensing

Setting the ENABLE REMOTE GND SENSE control bit HIGH in the BCR enables the REM GND SENSE input line in the system I/O connector (Paragraph 2.3.1.1).

3.4.6 Output Filters Control

The lowpass reconstruction output filters are selected by setting the ENABLE OUTPUT FILTERS control bit HIGH in the BCR.

3.5 Output Buffer

Analog output data from the cPCI bus flows into the 256 K-sample analog output FIFO data buffer (Table 3.5-1). From the buffer, the data passes to the analog output DAC channels.

NOTE: The output buffer capacity of 256 K-Samples is distributed among all active output channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 256K / Number of active channels.

Table 3.5-1. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only; Returns all-zero)**

BIT	MODE [1]	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D18	WO	DATA 01 - DATA 18	Intermediate data bits
D19	WO	DATA 19	Most significant data bit
D20	WO	EOF FLAG	End-of-frame (EOF) flag.
D21-D31	WO	---	(Inactive)

1. "WO" indicates write-only access. Read-access returns an all-zero value.

3.5.1 Data Frame

A *data frame* consists of an integral number of channel groups. For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated with an *end-of-frame* (EOF) flag. The EOF designation is applied by setting the EOF flag HIGH when loading the last channel value into the buffer. Thereafter, the EOF flag follows the last channel value through the buffer.

3.5.2 Output Data Format

Analog output data values are written in a 32-bit Lword-serial sequence to the Analog Output Buffer. Bits D19..0 represent the output data value. Bit D20 indicates the last value in a data frame, and is the end-of-frame (EOF) flag. The output buffer appears to the cPCI bus as a single 32-Bit register, and a read-access to this register returns an all-zero value.

3.5.3 Output Data Coding

Analog output data is arranged as 20 active right-justified data bits with the coding conventions shown in Figure 3.5-1. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

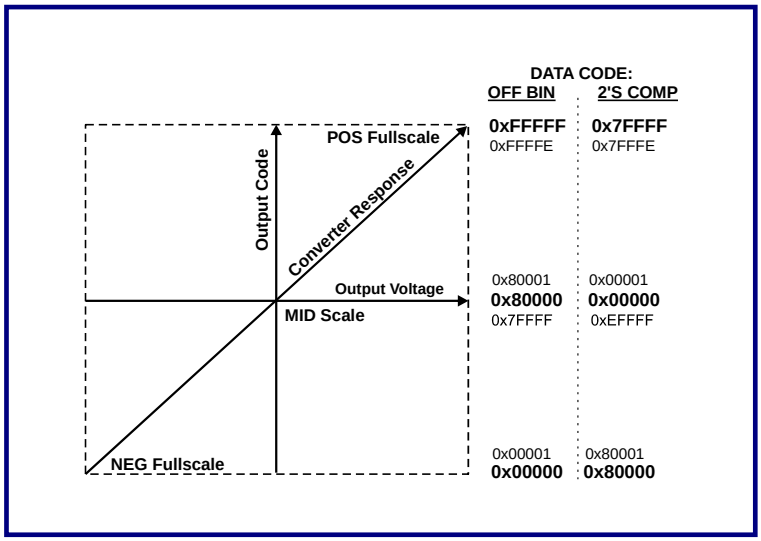

Figure 3.5-1. Analog Data Coding; 20 Bit Data

3.5.4 Buffer Loading

Channel data values are loaded into the output buffer in ascending order of the selected active channels. The channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Figure 3.5-2 illustrates a loading example that implements two output channels, with 100 values per channel. Each channel group in this example consists of active channels 0 and 5.

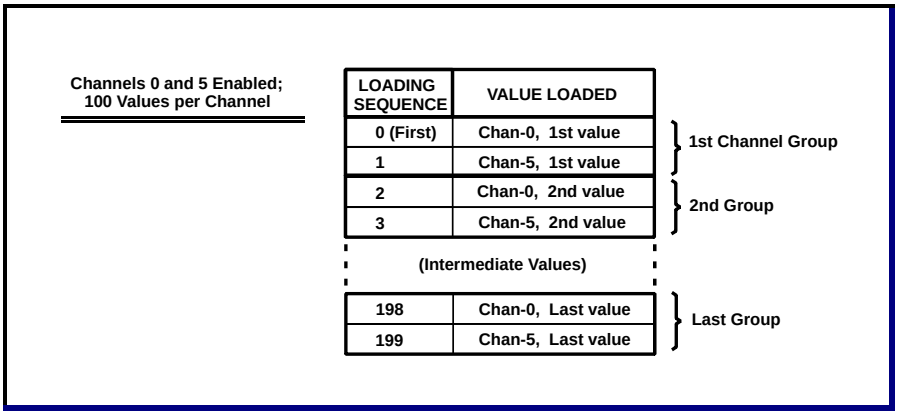

Figure 3.5-2. Typical Buffer Loading Sequence

NOTE: Data can be loaded from the cPCI bus to the output buffer only if the buffer is open; that is, not circular (3.5-7).

3.5.5 Output Buffer Control

The Buffered Output Operations register (Table 3.4-2) controls and monitors the flow of data through the analog output data buffer. Asserting the CLEAR OUTPUT BUFFER control bit HIGH clears, or empties, the buffer.

The AO BUFFER OVERFLOW flag is set HIGH if data is written to a full buffer, and the FRAME OVERFLOW flag indicates that an attempt was made to write data to a closed buffer. Both flags indicate data loss. Each of these flags, once set, remains HIGH until written LOW directly from the bus, or by initialization .

The AO BUFFER EMPTY flag indicates that the buffer contains no output data. The AO BUFFER FULL flag is asserted when the buffer is full. Data written to a full output buffer is discarded.

The Output Buffer Size register shown in Table 3.5-2 contains the number of output data values present in the buffer, and is updated continuously.

Table 3.5-2. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of data values in the output buffer
D19-D31	RO	(Inactive)	0	---

The Output Buffer Threshold register (Table 3.5-3) specifies the buffer size value ***above which*** the OUTPUT BUFFER THRESHOLD flag is asserted HIGH. This status flag is duplicated in the Buffered Output Operations register.

Table 3.5-3. Output Buffer Threshold Register

Offset: 0040h **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	(Reserved)	0	---
D20	RO	OUTPUT BUFFER THRESHOLD	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D21-D31	RO	(Reserved)	0	---

3.5.6 Open Buffer

If the CIRCULAR BUFFER control bit is LOW in the Buffered Output Operations register, the output buffer operates in the ***open*** mode. Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing, and will empty itself unless it is replenished from the cPCI bus. This mode of operation permits the continuous flow of data from the cPCI bus to the analog outputs.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.5-3 illustrates the movement of a single data frame through an open buffer.

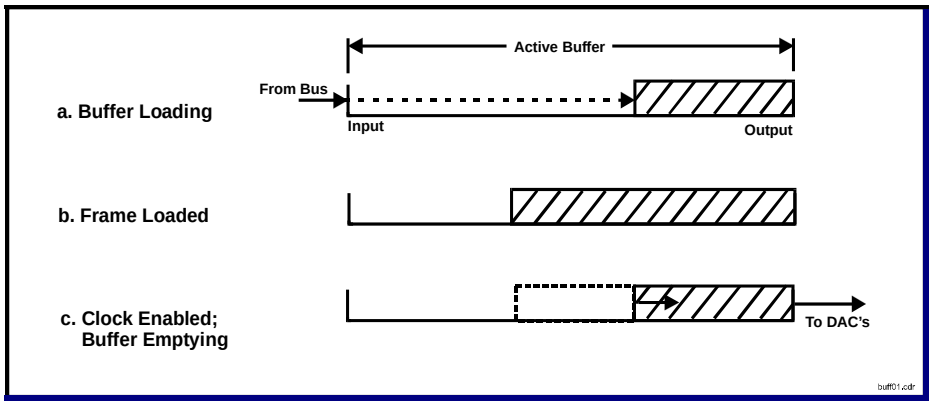

Figure 3.5-3. Open Buffer Data Flow

3.5.7 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the cPCI bus.

In Figure 3.5-4 a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

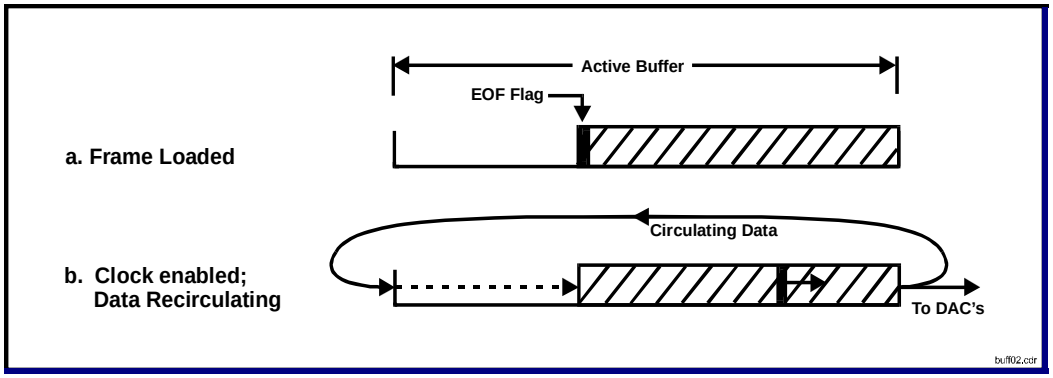

Figure 3.5-4. Circular Buffer Data Flow

An end-of-frame (EOF) flag identifies the end-point, or last value in a data frame, and is set HIGH when the last value is loaded. Multiple contiguous burst functions, or frames, can reside in the buffer simultaneously.

NOTE: Disable output clocking before loading the buffer for circular operation.

3.6 Function Generation

3.6.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous clocking and for circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly.

If triggered-burst clocking is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform is retained in the buffer and can be reproduced repeatedly by subsequent triggers.

3.6.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst clocking is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions are flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions are retained in the buffer, and the series of functions is repeated indefinitely. .

3.6.3 Function Sequencing (Concatenation)

A new function (data frame) can be concatenated to the end of an existing function in a circular buffer while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and simultaneously is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes automatically and the new function seamlessly begins circulating in the buffer and producing an output.

Introduction of a new function commences by setting the LOAD REQUEST flag HIGH in the buffered output operations register, and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag attached to the final value. When the last value in the original function is clocked from the buffer, the accompanying EOF flag closes the buffer, and clears both the LOAD READY flag and the LOAD REQUEST control bit. *Notice that the loading of the new function into the buffer must be completed before the existing function terminates.*

In Figure 3.5-5, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

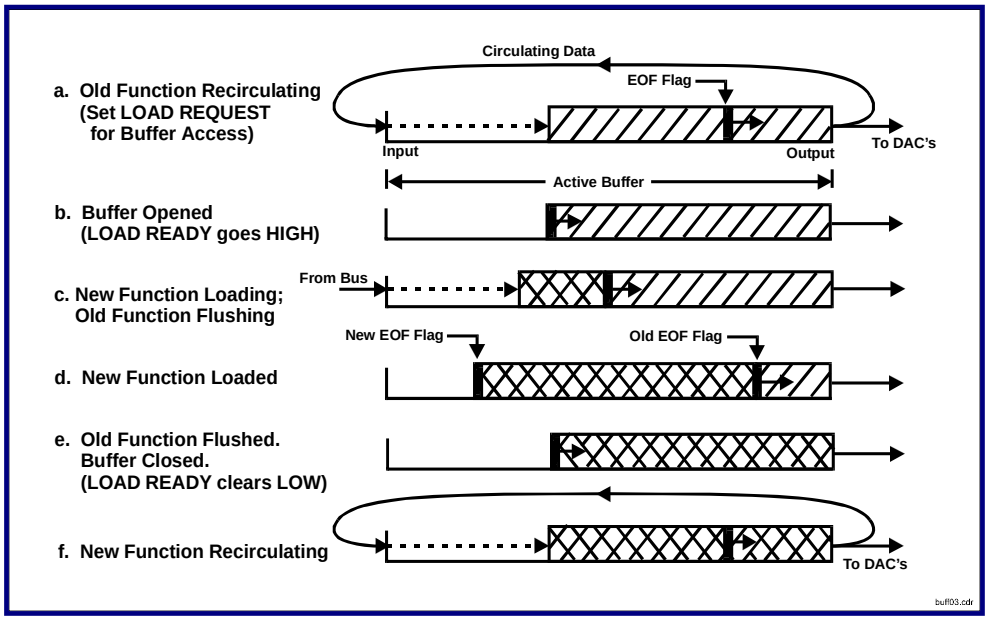

Figure 3.5-5. Function Sequencing (Concatenation)

After loading the new function, allow the LOAD REQUEST control bit to be cleared automatically. This bit should not be cleared from the cPCI bus.

NOTE: If the loading of a new function extends beyond the LOAD-READY interval, the FRAME OVERFLOW flag is set HIGH in the Buffer Operations register, indicating data loss. Once set, this flag remains HIGH until written LOW directly from the bus, or by initialization

3.7 Output Clocking

Each occurrence of the output clock updates either one or all of the active output channels, depending on whether sequential or simultaneous clocking is selected in the BCR.

Output clocking is enabled by setting the ENABLE OUTPUT CLOCKING control bit HIGH in the Buffered Output Operations register and enabling the associated clock source. The OUTPUT CLOCK READY status bit indicates that an output clock will be accepted. This status bit is LOW during reset operations or autocalibration.

3.7.1 Clock Source

The source of the analog output clock is controlled by the CLOCK SOURCE control field in the Output Configuration register, and the default source is the internal Rate-A generator. A software clock can be applied at any time by setting the OUTPUT SW CLOCK control bit HIGH in either the Buffered Output Operations register or the BCR. This bit overrides the existing CLOCK SOURCE selection, and clears automatically.

If the CLOCK AND TRIGGER OUT control bit is set HIGH in the Output Configuration register, the EXT CLK OUT and EXT SYNC OUT pins in the I/O connector each generates an output pulse when the corresponding internal clock or trigger occurs. If this bit is LOW (default), the EXT CLK OUT and EXT SYNC OUT pins produce no output.

3.7.1.1 External Clock

The external clock source at the CLOCK INPUT system I/O connector input can have any frequency up to the maximum value specified for the output clocking rate. When the external clock source is selected, output clocking occurs on a HIGH-to-LOW transition of the external analog output clock.

NOTE: Logic polarities of all external clock and trigger inputs and outputs are inverted if the INVERT EXT SYNC control bit is HIGH in the Output Configuration register.

3.7.1.2 Internal Clocking Rate Generator

The internal Rate-A generator provides an output clocking rate that is adjustable as described in Paragraph 3.11. The Rate-A generator is enabled by setting the ENABLE RATE-A GENERATOR control bit HIGH in the BCR.

3.7.2 Simultaneous Clocking

Simultaneous clocking is selected by setting the SIMULTANEOUS OUTPUTS control bit HIGH in the BCR. If simultaneous clocking is selected, the analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the output clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective clocking rate for each channel equals the output clocking rate.

3.7.3 Sequential Operation

Sequential clocking is selected when the SIMULTANEOUS OUTPUTS control bit in the board control register is LOW. At each clock occurrence in sequential operation, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately. Channel values are read from the buffer beginning with the lowest-numbered active channel in a channel group, and proceeding upward through the highest-numbered active channel. When operating in this mode, the effective clocking rate for each channel equals the output clocking rate *divided by the number of active channels*.

3.8 Clocking Mode

3.8.1 Continuous Clocking

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is LOW (default), the *continuous clocking* mode is selected and data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that an output clock is present. EOF flags are ignored when operating in this mode.

3.8.2 Data Bursts

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is HIGH, burst operation is selected. During a *triggered output burs*t, data is transferred continuously from the output buffer to the analog outputs until either the ***buffer goes empty, or an end-of-frame (EOF) flag is encountered***. In the triggered-burst clocking mode, an internal or external output trigger initiates the transfer of data from the output buffer to the output channels. The BURST READY status flag indicates that a burst trigger will be accepted, and is LOW during each burst.

The source of the output trigger is controlled by the TRIGGER SOURCE control field in the Output Configuration register, and the default source is the internal Rate-B generator. A software trigger can be applied at any time by setting the OUTPUT S/W TRIGGER control bit HIGH in either the Buffer Operations register or the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically. The OUTPUT SW TRIGGER bit goes HIGH during the software-triggered burst, and clears automatically when the burst is completed.

If the CLOCK AND TRIGGER OUT control bit is set HIGH in the output configuration register, the EXT SYNC OUT signal in the I/O connector produces an output pulse when the corresponding internal trigger occurs. If this bit is LOW (default), EXT SYNC OUT produces no output.

NOTE: Logic polarities of all external clock and trigger inputs and outputs are inverted if the INVERT EXT SYNC control bit is HIGH in the Output Configuration register.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (3.5-2). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected clocking rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

NOTE: The terms 'Trigger' and 'Sync' are used essentially interchangeably throughout this document. 'Trigger" usually refers to an event that initiates a triggered burst, while 'Sync' refers to the logic signal itself.

3.8.3 Internal Trigger Rate Generator

The internal Rate-B generator provides an internal trigger that is adjustable as described in Paragraph 3.11. The Rate-B generator is enabled by setting the ENABLE RATE-B GENERATOR control bit HIGH in the BCR.

3.9 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering (Common burst trigger)
c. Synchronous clocking (Common DAC clock)
d. Synchronous clocking and burst triggering (Common trigger and DAC clock).

As many as four boards can be synchronized together when connected in the Multidrop configuration (Figure 2.3-3) or any number can be synchronized together in the Daisy-Chain configuration (Figure 2.3-4).

The DIFFERENTIAL SYNC IO control bit in the BCR selects the clock and sync logic levels as either LVDS (HIGH) or TTL (LOW).

NOTE: For multiboard synchronization, an analog output clock or trigger initiator must have the CLOCK AND TRIGGER OUT control bit asserted. Likewise, all targets that drive other targets in a daisy-chain multiboard configuration must have this bit asserted.

3.10 Buffer DMA Operation

DMA transfers to the analog output FIFO buffer are supported in either block-mode or demand-mode, with the board operating as bus master. Bit 02 in the cPCI Command register must be set HIGH to select the bus mastering mode. Refer to the PCI-9656 reference manual for a detailed description of the associated DMA configuration registers.

3.10.1 Block Mode

Table 3.10-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 01, in which a cPCI interrupt is generated when the transfer has been completed.

Table 3.10-1. Typical Buffer DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A0h	DMA Transfer Byte Count	Number of bytes in transfer	*
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

For typical applications, the DMA Command/Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

3.10.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.10-2 shows a *typical* PCI register configuration for DMA Channel 01 demand mode operation.

Table 3.10-2. Typical Buffer DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32)	0002 1943h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

3.11 Rate Generators

Two rate generators supply independent frequencies for output clocking and burst control (Table 3.11-1). By default, the Rate-A Generator generates an internal clock for the analog outputs and the Rate-B generator controls output burst triggering.

Each generator is enabled by the associated ENABLE RATE-A/B GENERATOR control bit in the BCR. The generators are disabled when these bits are LOW.

Table 3.11-1. Rate Generator Registers (Rate-A,B)

Offset: 004Ch (Rate-A), 0050h (Rate-B) **Default: 0000 0200 (Rate-A), 0000 3000h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

The frequency **Fgen** (Table 3.11-2) of each generator is calculated as:

Fgen = Fclk / Ndiv,

where **Fclk** is the master clock frequency for the board, and **Ndiv** is the value written to the Rate-A/B Generator register. **Fgen** and **Fclk** are both expressed in the same frequency units. **Fclk** is assumed here to be **49.152 MHz,** but custom frequencies are available. If the master clock is provided with a custom frequency, **Fclk** equals the custom frequency. For an external clock or trigger input frequency, **Fclk** equals the external frequency, ***Fgen should not exceed the maximum clocking rate listed in the product specification.***

Table 3.11-2. Typical Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (49.152 MHz Master Clock) [1]
(Dec)	(Hex)	(Hz)
98	0062	501.551
99	0063	496.485
150	0096	327,680
512	0200	96,000
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv [2]

1. ±0.003 percent.
2. Fclk = master clock frequency; e.g.: 49.152MHz.

The maximum recommended analog output clocking rate is 500,000 clocks per second, although clocking rates not exceeding this limit by more than 5-percent should provide acceptable performance.

3.12 Digital I/O Port

The digital I/O port consists of eight bidirectional TTL I/O lines, with the corresponding data bits shown in Table 3.12-1. The DIO lines are arranged as two 4-bit nibbles, with the direction of each nibble controlled independently of the other. Each nibble is an input to the board if the associated DIO 00 03 OUTPUT control bit is LOW, or is an output if the bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the register. All digital I/O lines default to inputs.

Table 3.12-1. Digital I/O Port Register

Offset: 0004h **Default: 0000 0X0Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

3.13 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCI bus reset,
- Analog output range change.
- Modified Output Filter selection.

The analog outputs are autocalibrated on the selected output range.

NOTE: Analog outputs are active during autocalibration, and can vary between positive fullscale and Zero during the calibration sequence.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and for the 16-Channel configuration has a duration of **7 seconds** typically or **10 seconds** maximum. Completion of the operation can be detected either by monitoring the "Autocal completed" status flag in the Primary Status register (Table 3.15-1), or by simply waiting for a time interval sufficient to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate all outputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.14 Front Panel LED Indicator

A red LED indicator on the front panel is ON if the FRONT PANEL LED control bit is HIGH in the BCR, or is OFF if the bit is LOW. This control bit defaults to the HIGH (On) state, and the LED can be used during initialization to indicate that the bus has accessed the board by turning the LED off.

3.15 Primary Status Register (Interrupts)

3.15.1 Status Register Control

Critical status flags are consolidated into a single Primary Status register (Table 3.15-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the cPCI bus, either by clearing the response bit *or by clearing the associated selection bit*.

NOTE: The cPCI bus can only clear Response status bits LOW. A "one" written to a response bit is ignored.

A 'level-detected' event simply duplicates the selected signal, and remains HIGH as long as the event is true. The response bit for an event indicated as 'edge-detected' is set HIGH when the event transitions from false to true. Once asserted, an edge-detected response bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

Real-time access to an edge-detected signal is available by reading the source of the edge-driven response bit (e.g.: BURST READY in the Buffered Output Operations register is the signal that drives the "Burst Ready" response bit in the PSR).

Table 3.15-1 Primary Status Register

Offset: 0x0030 **Default: 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed [3]	D16	3.13
D01	(Reserved)	D17	---
D02	(Reserved)	D18	---
D03	(Reserved)	D19	---
D04	(Reserved)	D20	---
D05	(Reserved)	D21	---
D06	(Reserved)	D22	---
D07	(Reserved)	D23	---
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition [3]	D24	3.12
D09	Output Buffer threshold flag HIGH-to-LOW transition [3]	D25	3.5.5
D10	Output Buffer threshold flag LOW-to-HIGH transition [3]	D26	3.5.5
D11	Output Load-Ready Flag HIGH-to-LOW transition [3]	D27	3.6.3
D12	Output Load-Ready Flag LOW-to-HIGH transition [3]	D28	3.6.3
D13	Burst Ready [3]	D29	3.8.2
D14	AO Buffer Overflow or Frame Overflow [3]	D30	3.5.5, 3.6.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Edge-detected event.

3.15.2 Interrupts:

All of the response bits in the Primary Status Register are logically OR'd together to produce a local interrupt that can in turn invoke a cPCI interrupt on the INTA# line. In order for the board to generate a cPCI interrupt, the cPCI interrupt must be enabled. The cPCI interrupt is enabled by setting the c*PCI Interrupt Enable* and c*PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in the PLX™ PCI-9656 reference manual.

3.16 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.16-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 0XXX XXXXh**

BIT FIELD	DESCRIPTION
D00-D15	Firmware Revision
D16-D17	Number of analog output channels: 0 => 16 output channels. 1 => 12 output channels. 2 => 8 output channels. 3 => 4 output channels.
D18-D19	Master Clock Frequency: 0 => 49.152MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D20-D21	Reconstruction Filter Type (Lowpass): 0 => Type F1: DC-140kHz, Elliptic, 8th Order. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D22-D23	Output Ranges, Software-Selectable: 0 => ±6V, ±3V. 1 => ±10V, ±5V. 2 => (Reserved) 3 => (Reserved)
D24	Output Configuration: 0 => Differential outputs. 1 => Single-Ended outputs
D25-D27	Custom Features: 0-7 => (Reserved).
D28-D31	(Reserved bit field; returns all-zero).

3.17 Buffered Analog Output Application Examples

Specific operating modes and procedures vary widely according to the unique requirements of each application. The examples presented in this section illustrate basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally apply to a single output channel for simplicity of explanation. However, each active channel represents an independent set of function values, and all channels share a common output clock.

Table 3.17-1. Summary of Operation Examples

Operation Example	Description
Sequential Outputs	Each value written to the output data buffer updates the associated analog output channel when clocked, independently of the other channels.
Simultaneous Outputs	Data values accumulate in the output data buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously when clocked.
Continuous Function	An extension of Simultaneous Outputs, in which the buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.17-2 have already been performed.

Table 3.17-2. Initial Operations

Operation	Default Value	Applicable Paragraph
The board has been reset or initialized.	---	3.3.2
The active channel group has been defined .	All channels active	3.4.1
The required output coding has been selected.	Offset binary	3.5.3

The remaining operational parameters are assumed to be in the following *default* states initially:

Parameter	Default
Buffer mode:	Open
Buffer status:	Empty
Clocking rate:	96KSPS
Clocking mode:	Sequential

Parameter	Default
Clock source:	Rate-A Generator
Clock status:	Disabled
Trigger source:	Rate-B Generator
Trigger status:	Disabled

3.17-1 Sequential Outputs

Table 3.17-3. Sequential Outputs Example

Operation	PCI Bus Action	Board Response
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-A GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Load the output value for the first active channel.	Write the first value to the output data buffer.	Output value appears immediately (when clocked) at the analog output.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active analog outputs are updated in ascending sequence.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	Each value written to the buffer is transferred immediately to the associated analog output when clocked

Notes:
1. End-of-frame (EOF) flags are ignored when operating in the open-buffer mode. Only D19..0 are active in the output buffer.
2. Access to an individual output channel is accomplished by first selecting (enabling) only the specific channel, and by then writing the output value to the buffer.

3.17-2 Simultaneous Outputs

Table 3.17-4. Simultaneous Outputs Example (Single Group)

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the BCR.	Simultaneous clocking is selected.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-A GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the output value for the first active channel.	Write the first value to the output data buffer.	First active value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active values are accumulated in the buffer. When the last active value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

3.17-3 Continuous Function

Table 3.17-5. Continuous Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Set the buffer threshold flag to 1/4 of the expected block size.	Write 1/4 block size to the threshold register.	The threshold flag will go LOW when the buffer contents drop below the threshold.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-A GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the selected rate. The internal rate generator is enabled, if internal clocking is required.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Write a block of values to all active channels. To avoid discontinuities in the output functions, the effective loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 50MSPS during DMA transfers.	Write function values for all active channels to the output data buffer.	All active channels produce their respective output functions.
Wait for the buffer threshold flag to go LOW. (See Note 1).	Monitor the analog output buffer threshold flag until LOW.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:
1. Response to the threshold flag must be fast enough to prevent the buffer from going empty.

3.17.4 Periodic Function

Table 3.17-6. Periodic Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. (Note 1) Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Select the circular buffer mode.	Set CIRCULAR BUFFER in the buffer operations register.	The output buffer is closed (circular).
Enable the output clock.	Set ENABLE OUTPUT CLOCKING in the buffer operations register. Set the ENABLE RATE-A GENERATOR control bit HIGH in the BCR.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:

1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.17.5 Function Burst

Table 3.17-7. Function Burst Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Select the triggering rate.	Write the required triggering rate to the Rate-B generator control register.	The burst triggering rate is selected.
Select triggered-burst mode.	Set ENABLE OUTPUT BURST in the buffer operations register.	The triggered-burst operating mode is selected.
Prepare the buffer operations register for burst mode:	Write to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
Enable the output clock.	Set ENABLE OUTPUT CLOCKING.	Output clocking is enabled.
Enable the internal rate generators.	Set the ENABLE RATE-A and RATE-B GENERATOR control bits in the BCR.	Required internal rate generators are enabled.
For external burst triggering, or internal rate-generator triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each trigger.

3.17.6 Function Sequencing (Concatenation)

Table 3.17-8. Function Sequencing (Concatenation) Example

Operation	PCI Bus Action	Board Response
Establish the generation of a periodic function. The following operations will replace the original ('old') function in each channel with a 'new' function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request buffer access	Set LOAD REQUEST in the buffer operations register.	The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Monitor the LOAD READY status flag. The buffer is open when this flag goes HIGH.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode when the EOF flag for the old function is detected, indicating that the last data value in the original function set has left the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Sixteen 20-bit analog output channels (Figure 4.1-1) provide software-selected output ranges of ±6V and ±3V, or optionally ±10V and ±5V, and are accessed from the cPCI bus through a dedicated 256K-sample FIFO buffer. The outputs are factory-configured as either single-ended signals, or as 3-wire balanced differential pairs. An 8-Bit digital port is configured as two independently controlled sets of four bidirectional I/O lines.

A PCI interface adapter provides a 33/66MHz, 32/64-Bit interface between the controlling cPCI bus and a 32-Bit internal local controller. +5 VDC power from the cPCI bus is converted into regulated power voltages for the internal analog networks.

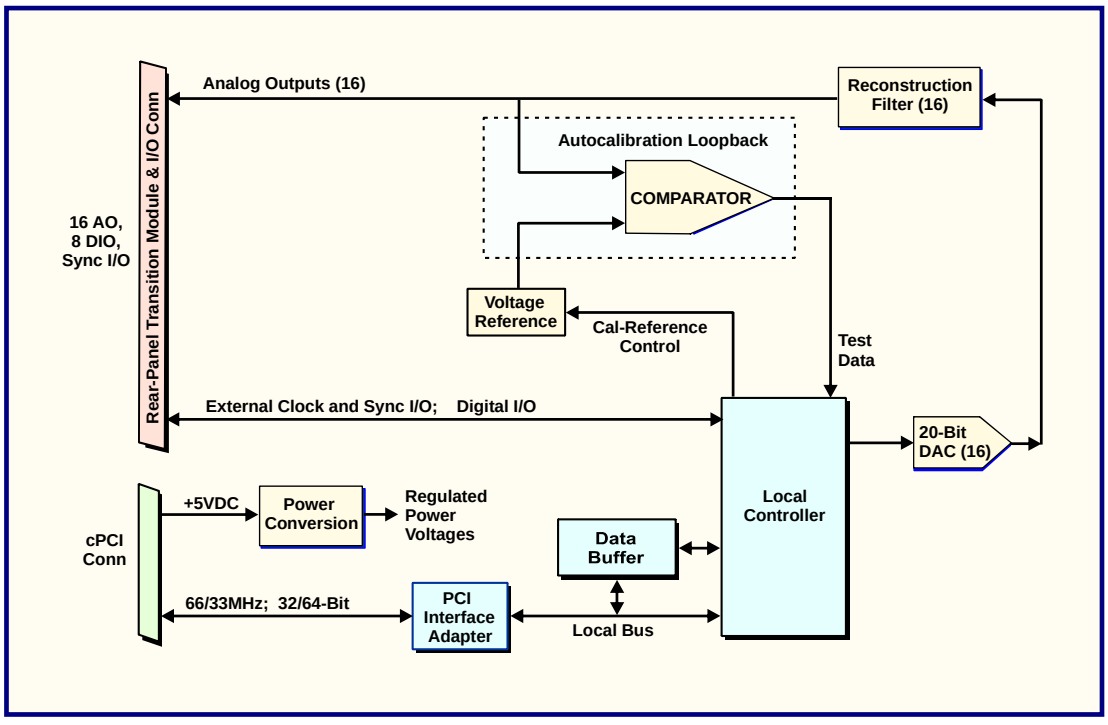

Figure 4.1-1. Functional Block Diagram

Autocalibration loopback provides test signals for autocalibration of all output channels, and are configured to accept either differential or single-ended system outputs.

Analog output clocking on multiple target boards can be synchronized to a single software-designated initiator board.

4.2 Analog Outputs

Sixteen independent 20-bit R-2R DAC's are controlled through a dedicated 256 Ksample FIFO buffer. The buffer can be operated either open for data streaming, or closed (circular) for arbitrary or periodic function generation. Function concatenation from the cPCI bus is supported. The output configuration can be selected as either single-ended or balanced differential.

Each 20-bit DAC implements an R-2R ladder, which eliminates the low-limit on clocking frequencies that is characteristic of high-resolution 'sigma-delta' converters. Output clocking and triggering can be supplied either from two internal 24-Bit analog output rate generators, or from external sources. Triggered bursts, or functions, are supported. The output burst size is controlled by a tag-bit attached to the last output value in a sequence. If the tag-bit is not attached, a burst will operate continuously, or until the buffer goes empty.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The calibration algorithm drives the output of each channel under calibration alternately to ground and to 99-percent of fullscale, and successively iterates the value of a 16-Bit gain (or offset) calibration DAC to match the reference or ground voltage to within approximately 0.00015-percent. A high-gain loopback voltage comparator provides a one/zero test output in response to the output channel under test.

The gain and offset corrections for each channel are adjusted in a series of second-level fullscale/offset adjustment iterations, in which each iteration reduces the adjustment error by one-half. The factor of one-half arises from the fact that each gain adjustment shifts the offset response to a midscale output DAC value by one-half, due to the relative positions of the gain (PFS) and offset midscale (MID) output values on the output DAC response function. Each offset correction however, produces an equal shift in the gain response (to a PFS output DAC value).

Each iteration adjusts the gain first, and then the offset. In the first iteration for each channel, the gain adjustment is performed with the offset caldac adjusted to midrange.

Since the gain adjustment range is on the order of +/-5 percent, 14 second-level iterations are required in order to ensure a maximum final error of +/-0.0005 percent. For this level of accuracy then, each channel requires 2*14*16 = 448 iterations of its two calibration DAC's.

The final value for each gain and offset Calibration DAC is stored in volatile calibration memory, as well as in the DAC itself, and is retained until a cPCI reset occurs or until autocalibration is executed again.

4.4 Power Control

Regulated precision power voltages of ±5 VDC and ±14 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the cPCI bus, both by switching preregulators and by linear postregulators. Postregulation ensures optimum regulation and minimum noise on all power voltages in the analog sections.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2208 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	0000 0X0Xh	Digital I/O port data.	3.12
0008-002C	(Reserved)	RO	0000 0000h	---	---
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register, Interrupts	3.15
0034	ASSEMBLY CONFIGURATION	RO	0XXX XXXXh	Options and firmware revision.	3.16
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1400h	Buffered Analog Outputs Control	3.4
0040	OUTPUT BUFFER THRESHOLD	RW	0003 FFFEh	Output buffer status flag threshold.	3.5.5
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.5.5
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.5
004C	RATE GENERATOR A	RW	0000 0200h	Rate-A generator divider; 24 bits.	3.11
0050	RATE GENERATOR B	RW	0000 3000h	Rate-B generator divider; 24 bits.	3.11
0054	OUTPUT CONFIGURATION	RW	0001 FFFFh	Analog output configuration.	3.4
0056-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2208 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	RW	(Reserved)	0	---	---
D05	RW	DIFFERENTIAL SYNC IO	0	Selects LVDS external sync I/O levels when HIGH.	3.9
D06	RW	ENABLE REMOTE GND SENSE	0	Enables correction for remote ground potential (single-ended outputs only)	3.4.5
D07-D17	RW	(Reserved)	0	---	---
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.7
D19	RW	FRONT PANEL LED	1	Illuminates the front-panel LED when HIGH.	3.14
D20	RW	OUTPUT SW CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.7
D21	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog outputs.	3.11
D22	R/W	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for analog outputs.	3.11
D23	R/W	OUTPUT SW TRIGGER [2,3]	0	Output Burst S/W Trigger. See also Table 3.4-2.	3.8.2
D24	RW	ENABLE OUTPUT FILTERS	0	Activates the lowpass filters in all output channels.	3.4.6
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.5.3
D26-D27	RO	(Reserved)	0	---	---
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.13
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.13
D30	RO	(Reserved)	0	---	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Output Configuration Register

Offset: 0054h **Default: 0001 FFFFh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	RW	OUTPUT 00	1	Analog Output Active Channel selection mask. HIGH to enable.	3.4.1
D01	RW	OUTPUT 01	1		
D02	RW	OUTPUT 02	1		
D03	RW	OUTPUT 03	1		
D04	RW	OUTPUT 04	1		
D05	RW	OUTPUT 05	1		
D06	RW	OUTPUT 06	1		
D07	RW	OUTPUT 07	1		
D08	RW	OUTPUT 08	1		
D09	RW	OUTPUT 09	1		
D10	RW	OUTPUT 10	1		
D11	RW	OUTPUT 11	1		
D12	RW	OUTPUT 12	1		
D13	RW	OUTPUT 13	1		
D14	RW	OUTPUT 14	1		
D15	RW	OUTPUT 15	1		
D16	RW	OUTPUT HIGH RANGE	1	Analog Output Range: Installed Range = ±6V, ±3V: 0 => ±3V 1 => ±6V. Installed Range = ±10V, ±5V: 0 => ±5V 1 => ±10V	3.4.2
D17	RW	CLOCK AND TRIGGER OUT	0	Enables the Analog Output Clock and Trigger external outputs,	3.7.1 3.8.2
D18-D19	RW	CLOCK SOURCE	0	Analog Output clock source: 0 => Rate-A Generator. 1 => Rate-B Generator. 2 => Analog Output External Clock input 3 => (Reserved).	3.7.1
D20-D21	RW	TRIGGER SOURCE	0	Analog Output trigger source: 0 => Rate-B Generator. 1 => Rate-A Generator.. 2 => Analog Output External Trigger input 3 => (Reserved).	3.8.2
D22	RW	(Reserved)	0	---	---
D23	RW	INVERT EXT SYNC	0	Inverts the logic polarities of the external clock and trigger inputs and outputs.	3.7.1.1
D24-D31	RO	(Reserved)	0000h	---	---

Table 3.4-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000 1400h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	R/W	(Reserved)	0h	---	---
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.7
D06	RO	OUTPUT CLOCK READY	0	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.7
D07	R/W	OUTPUT SW CLOCK [1,3]	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.7
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.5.6
D09	R/W	LOAD REQUEST [1]	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.6.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.6.3
D11	R/W	CLEAR OUTPUT BUFFER [1]	0	Resets the output buffer to empty.	3.5.5
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.5.5
D13	RO	OUTPUT BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.5.5
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.5.5
D16	R/W	AO BUFFER OVERFLOW [2]	0	Set HIGH when data is written to a full buffer.	3.5.5
D17	R/W	FRAME OVERFLOW [2]	0	Set HIGH when data is written to a closed buffer.	3.6.3
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.8.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.8.2
D20	R/W	OUTPUT SW TRIGGER [1,3]	0	Produces a single output trigger event when asserted. Clears LOW automatically when the triggered burst is completed. Independent of triggering mode. Duplicated in the BCR.	3.8.2
D21-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

1. Clears LOW automatically when operation is completed.
2. Remains HIGH until cleared by a direct write as LOW, or by initialization.
3. Duplicated elsewhere.

Table 3.5-1. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only; Returns all-zero)**

BIT	MODE [1]	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D18	WO	DATA 01 - DATA 18	Intermediate data bits
D19	WO	DATA 19	Most significant data bit
D20	WO	EOF FLAG	End-of-frame (EOF) flag.
D21-D31	WO	---	(Inactive)

1. "WO" indicates write-only access. Read-access returns an all-zero value.

Table 3.5-2. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of data values in the output buffer
D19-D31	RO	(Inactive)	0	---

Table 3.5-3. Output Buffer Threshold Register

Offset: 0040h **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	(Reserved)	0	---
D20	RO	OUTPUT BUFFER THRESHOLD	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D21-D31	RO	(Reserved)	0	---

Table 3.10-1. Typical Buffer DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A0h	DMA Transfer Byte Count	Number of bytes in transfer	*
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

Table 3.10-2. Typical Buffer DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32)	0002 1943h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

Table 3.11-1. Rate Generator Registers (Rate-A,B)

Offset: 004Ch (Rate-A), 0050h (Rate-B) **Default: 0000 0200 (Rate-A), 0000 3000h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

Table 3.11-2. Typical Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (49.152 MHz Master Clock) [1]
(Dec)	(Hex)	(Hz)
98	0062	501.551
99	0063	496.485
150	0096	327,680
512	0200	96,000
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv [2]

1. ±0.003 percent.

2. Fclk = master clock frequency; e.g.: 49.152MHz.

Table 3.12-1. Digital I/O Port Register

Offset: 0004h **Default: 0000 0X0Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.15-1 Primary Status Register

Offset: 0x0030 **Default: 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed [3]	D16	3.13
D01	(Reserved)	D17	---
D02	(Reserved)	D18	---
D03	(Reserved)	D19	---
D04	(Reserved)	D20	---
D05	(Reserved)	D21	---
D06	(Reserved)	D22	---
D07	(Reserved)	D23	---
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition [3]	D24	3.12
D09	Output Buffer threshold flag HIGH-to-LOW transition [3]	D25	3.5.5
D10	Output Buffer threshold flag LOW-to-HIGH transition [3]	D26	3.5.5
D11	Output Load-Ready Flag HIGH-to-LOW transition [3]	D27	3.6.3
D12	Output Load-Ready Flag LOW-to-HIGH transition [3]	D28	3.6.3
D13	Burst Ready [3]	D29	3.8.2
D14	AO Buffer Overflow or Frame Overflow [3]	D30	3.5.5, 3.6.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Edge-detected event.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 0XXX XXXXh**

BIT FIELD	DESCRIPTION
D00-D15	Firmware Revision
D16-D17	Number of analog output channels: 0 => 16 output channels. 1 => 12 output channels. 2 => 8 output channels. 3 => 4 output channels.
D18-D19	Master Clock Frequency: 0 => 49.152MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D20-D21	Reconstruction Filter Type (Lowpass): 0 => Type F1: DC-140kHz, Elliptic, 8th Order. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D22-D23	Output Ranges, Software-Selectable: 0 => ±6V, ±3V. 1 => ±10V, ±5V. 2 => (Reserved) 3 => (Reserved)
D24	Output Configuration: 0 => Differential outputs. 1 => Single-Ended outputs
D25-D27	Custom Features: 0-7 => (Reserved).
D28-D31	(Reserved bit field; returns all-zero).

APPENDIX B

COMPARISON of CPCI6U64-20AOF16C500KR and PMC66-18AO8

Appendix B

Comparison of CPCI6U64-20AOF16C500KR and PMC66-18AO8

Operation of the CPCI6U64-20AOF16C500KR is similar to that of the PMC66-18AO8. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a comprehensive list of requirements.

B.1. Comparison of Features

Table B.1 compares principal CPCI6U64-20AOF16C500KR and PMC66-18AO8 features. Modifications are shown in bold type.

Table B.1. PMC66-18AO8 and CPCI6U64-20AOF16C500KR Comparison

Feature	CPCI6U64-20AOF16C500KR	PMC66-18AO8
Form Factor	**cPCI 6U, with Rear-Panel Access**	**PMC; Single-width**
Output Channels	**Sixteen 20-Bit Dac's; R-2R**	**Eight 18-Bit Dac's; R-2R Hybrid**
Output Filters	**8th-Order lowpass reconstruction filters**	**1st-order lowpass filters**
PCI Interface	**PCI 2.3; 33MHz/66MHz; 32/64-Bit PCI bus**	**PCI 2.3; 33MHz/66MHz; 32-Bit PCI bus**
PCI Adapter	**PCI-9656 (64/32-Bit, 66MHz PCI)**	**PCI-9056 (32-Bit, 66MHz PCI)**
DMA Access (Buffers)	**Block-mode; Demand-Mode**	**Block mode**
Output Configuration	**Single-Ended or Balanced Differential; Factory-configured**	**Single-Ended or Balanced Differential; Software-selectable**
Output Ranges	**±6V and ±3V; Optionally ±10V, ±5V**	**±10V, ±5V, ±2.5V**
Rate Generators	Two, with 24-Bit dividers	Two, with 24-Bit dividers
Local Clock	48-52 MHz; Standard 49.152MHz	40-45 MHz; Standard 40.32MHz
Output Clock Rates	Zero to 500KSPS/Chan	Zero to 500KSPS/Chan
Output Buffer	256K-Sample FIFO	256K-Sample FIFO
Digital I/O Port	8-Bit Bidirectional TTL; Nibble oriented.	8-Bit Bidirectional TTL; Nibble oriented.

B.2. Migration from PMC66-18AO8:

Section 2: Installation and Maintenance:

- General configuration and system-I/O have changed to accommodate the cPCI 6U form factor.

Table 3.1-1. Control and Status Registers:

- Deleted "Selftest" control registers.
- Renamed Rate-Generator "C" and "D" control registers as "A" and "B" registers.

Table 3.2-1. Board Control Register (BCR):

- Deleted "Selftest" control bits; Added "Enable Output Filters" and "Front Panel LED" control bits.

Table 3.4-1. Output Configuration Register:

- Bit fields have been relocated to accommodate 16 active-channel mask bits.
- The 'Output Range' control field has been reduced to a single 'Output High Range' bit.
- The 'Differential Config' control bit has been deleted.

Paragraph 3.5. Output Buffer:

- Modified to accommodate a 20-Bit data field.

Paragraph 3.10. Buffer DMA:

- Both 'Block Mode' and 'Demand Mode' DMA are now supported.

Paragraph 3.11. Rate Generators:

- The master clock frequency Fclk has changed to 49.152MHz.

Paragraph 3.14. Selftest:

- This section has been redesignated as "Front Panel LED Indicator".

Paragraph 3.18. Auxiliary External Clock and Trigger I/O

- Deleted. This function does not exist in this product.

Revision History:

06-01-2011: Origination. Preliminary draft.

04-04-2012: Table 3.4-1: Corrected clock and trigger sources on Sh-A4.
Table 3.12-1: Corrected offset reference in body of text.
Para 3.13 : Updated autocal duration.

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