General Standards Corporation

High Performance Bus Interface Solutions

Rev: 030512

CCPMC66-14HSAI2

2-CHANNEL, 14-BIT, 50 MSPS/CHANNEL CONDUCTION COOLED PMC ANALOG INPUT BOARD

With Simultaneous Sampling, Local Data Packing and 66MHz PCI Support

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REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The CCPMC66-14HSAI2 board is a conduction cooled single-width PCI mezzanine card (PMC) that provides wideband simultaneously-sampled 14-bit analog input channels. As many as **two** analog input channels can be digitized simultaneously at sustainable aggregate rates up to 100 million samples per second (MSPS). Three input configurations are available, providing software-controlled input ranges from ±0.625V to ±2.5V for the Wideband input configuration, ±2.5V to ±10V for the High-Level configuration, or 1Vp-p to 2Vp-p for the Transformer-Coupled configuration. This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

For the High-level and Wideband configurations, autocalibration determines offset and gain correction values for each input channel, and the corrections are applied subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

Power requirements consist of +5 VDC from the PCI bus in compliance with the PCI specification, and operation over the specified temperature range is achieved with conduction cooling. Specific details of physical characteristics and power requirements are contained in the CCPMC66-14HSAI2 product specification. Figure 1.1-1 shows the physical configuration of the board, and the general arrangement of major components.

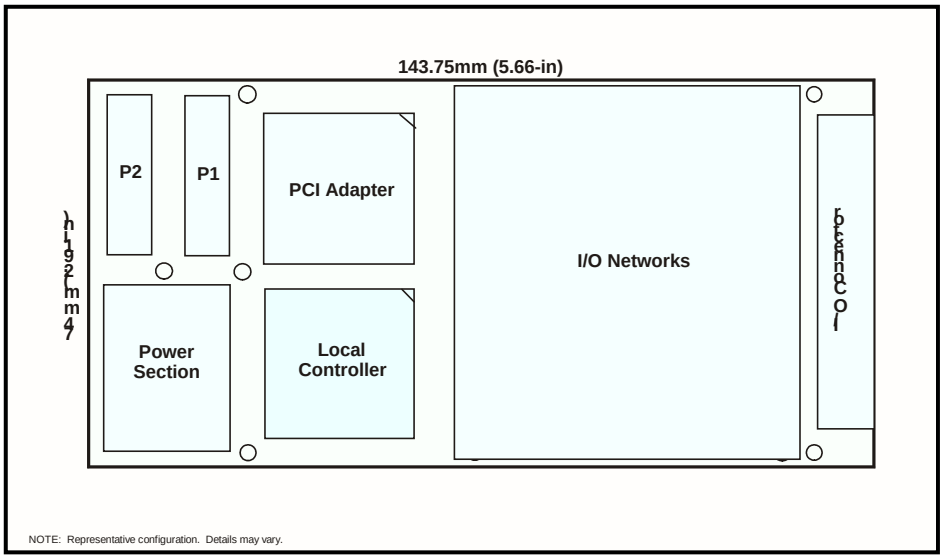

Figure 1.1-1. Physical Configuration

This product is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. System input and output connections can be made either through six standard MMCX coaxial connectors, or through a single high-density ribbon-cable connector.

1.2 Functional Overview

Two 14-Bit analog input channels are sampled and digitized simultaneously at rates up to 50,000,000 samples per second per channel for each of two channels, ~~or up to 25MSPS per channel for four channels~~. Each input channel contains a dedicated 14-Bit pipelined ADC, and the resulting sampled data is available to the PCI bus through a 1-Megabyte FIFO data buffer. All operational parameters are software configurable.

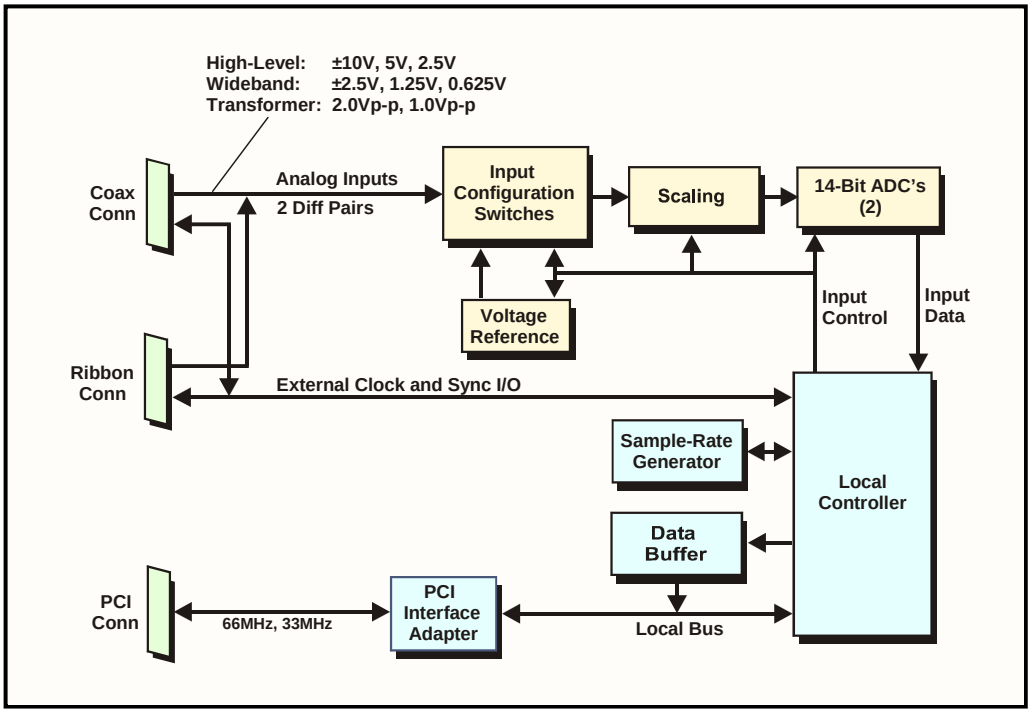

Figure 1.2-1. Functional Organization

The sample clock can be generated by an adjustable internal rate generator or by external hardware. Burst acquisition is supported internally by rate-generator and software triggering, and externally by hardware triggering. Pretriggering and sync-on-level functions are supported, and multiple boards can be synchronized to a common sample clock and a common burst trigger source.

Each data value can be channel-tagged. The data buffer can be operated in a 16-Bit non-packed configuration with a buffer capacity of 256K-samples, or the input data can be packed locally with two data values in a single 32-Bit longword for a 512K-sample capacity.

The High-level and Wideband input configurations are supported with on-demand autocalibration, which uses a precision internal voltage reference to provide maximum accuracy. Offset and gain correction values are determined during autocalibration, and are stored in calibration DAC's for each channel.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

With the single exception of single-ended input selection jumpers, this product has no field-alterable features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before or during installation, this produce should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the standoffs and PCI connectors facing the host board, and with the I/O connector oriented toward the front panel (Figure 2.2-1). Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

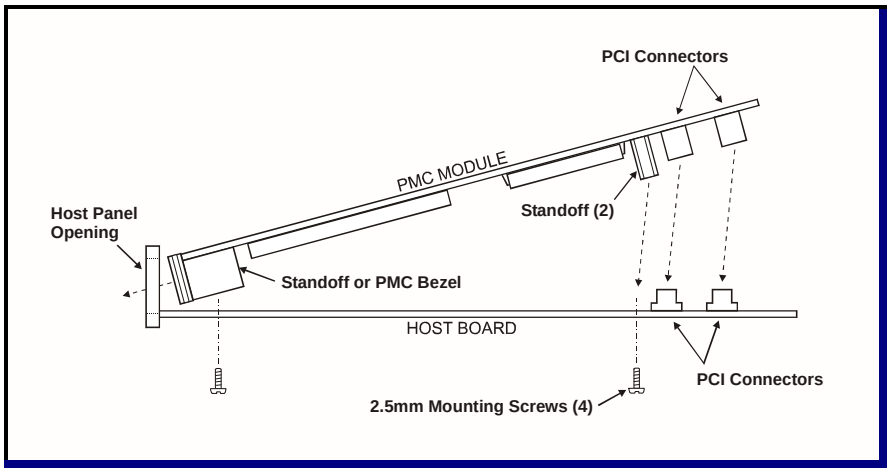

Figure 2.2-1: PMC Physical Installation

2.2.2 Input/Output Cable Connections

System I/O connectors are shown in Figure 2.2-2, and consist of six MMCX coaxial connectors and a 20-Pin ribbon-cable connector. The coaxial connectors provide connections for the **two** differential or single-ended analog input channels, and for bidirectional Clock and Sync (also referred to as Trigger) signals. Suitable MMCX mating cable plugs include Johnson 135-3403-001 for RG-316 coaxial cable, and 135-3402-001 for RG178 cable. MMCX connectors and complete cables are readily available through distributors, and adapters are available for SMA, SMB and BNC connection systems.

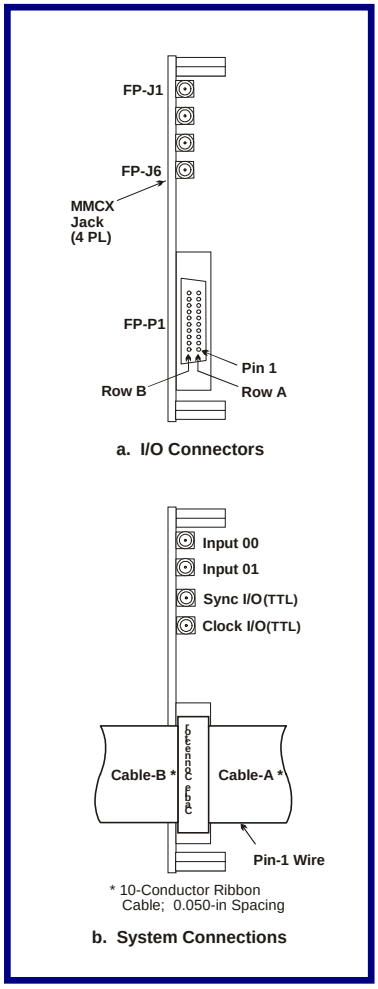

Figure 2.2-2. Input/Output Connectors

Table 2.2-1. Ribbon Cable Pin Functions

ROW-A	
PIN	**SIGNAL**
1	INPUT RETURN
2	INPUT 00 HI
3	INPUT 00 LO
4	INPUT RETURN
5	INPUT 01 HI
6	INPUT 01 LO
7	INPUT RETURN
8	
9	
10	INPUT RETURN

ROW-B	
PIN	**SIGNAL**
1	INPUT RETURN
2	
3	
4	INPUT RETURN
5	DIGITAL RETURN
6	SYNC (TRIGGER) I/O HI
7	SYNC (TRIGGER) I/O LO
8	DIGITAL RETURN
9	CLOCK I/O HI
10	CLOCK I/O LO

The **two** analog inputs and the clock and sync signals are accessible also through the 20-Pin dual-ribbon cable connector. Analog input HI and LO pins are connected internally to the center-conductor and outer shells, respectively, of the coaxial connectors FP-J1 through FP-J4. Clock and sync signals in the ribbon cable implement LVDS differential signaling, while the coaxial clock and sync connectors accept standard TTL levels. The recommended mating cable connector for the ribbon cable connector is a Robinson-Nugent P50E-020S-TG high-density socket connector. Contact the factory if preassembled cables are required.

2.3 System Configuration

2.3.1 Analog Inputs

The analog inputs can be operated in either differential or single-ended configurations, and are factory-configured with a specific input impedance. Refer to the product specification and model number for details.

2.3.1.1 Configuring Differential or Single-Ended Inputs

The **two** differential analog input channels can be configured as single-ended inputs by installing the associated jumpers in Headers J2 ~~and J3,~~ as indicated in Table 2.3-1. Each channel is in differential configuration if the jumper is omitted, or is single-ended if the jumper is installed. The factory default configuration omits the jumpers, which are supplied in an accessory envelope with each product. Headers J2 ~~and J3~~ are located directly behind the coaxial I/O connectors.

Table 2.3-1. Single-Ended Selection Jumpers

Input Channel	Selection Jumper *
00	J2; Pin-1 to Pin-2
01	J2; Pin-3 to Pin-4

* Install for single-ended operation. Omit for differential operation.

2.3.1.2 Differential Operation

Operating in the default differential configuration (Figure 2.3-1a) ensures maximum accuracy and immunity to system noise and interference, and is usually applied in systems in which the signal source return is connected to a system ground. The 'HI' input of a differential channel is measured with respect to the associated 'LO' input of the same channel. In a coaxial connection, the center conductor is the 'HI' input, and the outer conductor or shield is the 'LO' input. The board's input return is not accessible to coaxial inputs, but connection of the signal return to system ground usually is sufficient to provide an acceptable common mode voltage.

Differential operation can be used in any system configuration, if neither the HI or LO input level relative to the board's input return exceeds the maximum common mode voltage (CMV) indicated in the product specification. For the high-impedance version of this product, floating inputs (inputs with no direct connection to the internal system ground) can easily exceed this limit, and should be returned to system ground with a resistance of one K-Ohm or less.

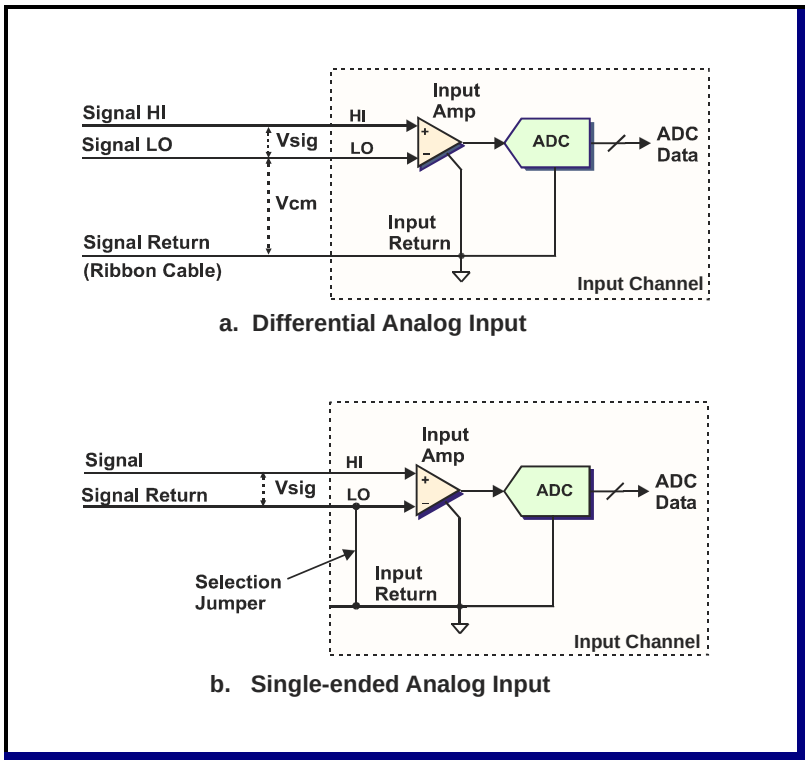

Figure 2.3-1. Analog Input Configurations

2.3.1.3 Single-Ended Operation

Single-ended operation (Figure 2.3-1b) eliminates common mode issues, but requires a direct ground connection for the signal return. This configuration normally is reserved for signal sources that are galvanically isolated from the internal system ground; that is, for signal sources that have no DC connection the system ground.

NOTE: Installing a single-ended selection jumper connects the associated analog input 'LO' signal to internal system ground, which usually is connected eventually to AC service power ground. **Before implementing single-ended operation, ensure that the external signal return can not inject destructive ground current into the board's internal ground.**

2.3.2 External Clock and Sync I/O

Bidirectional Clock and Sync I/O lines support the synchronization of conversion clocking and burst triggering among multiple boards in an initiator-target configuration, and allow these functions to be controlled by external signal sources. Clock and sync signals in the coaxial connectors are standard single-ended TTL levels, while the ribbon cable signals are LVDS differential signal pairs. TTL inputs are pulled up to +3.3 Volts internally through 5 K-Ohms. Maximum TTL output loading is 8 milliamps.

An initiator can directly control up to four target boards (Figure 2.3-2a) using the TTL coaxial connectors, if total cable length is 50 centimeters (20 inches) or less. To avoid fanout or loading issues with LVDS signals (Figure 2.3-2b), a 'star' distribution system (Figure 2.3-2c) is recommended if more than one LVDS target is present.

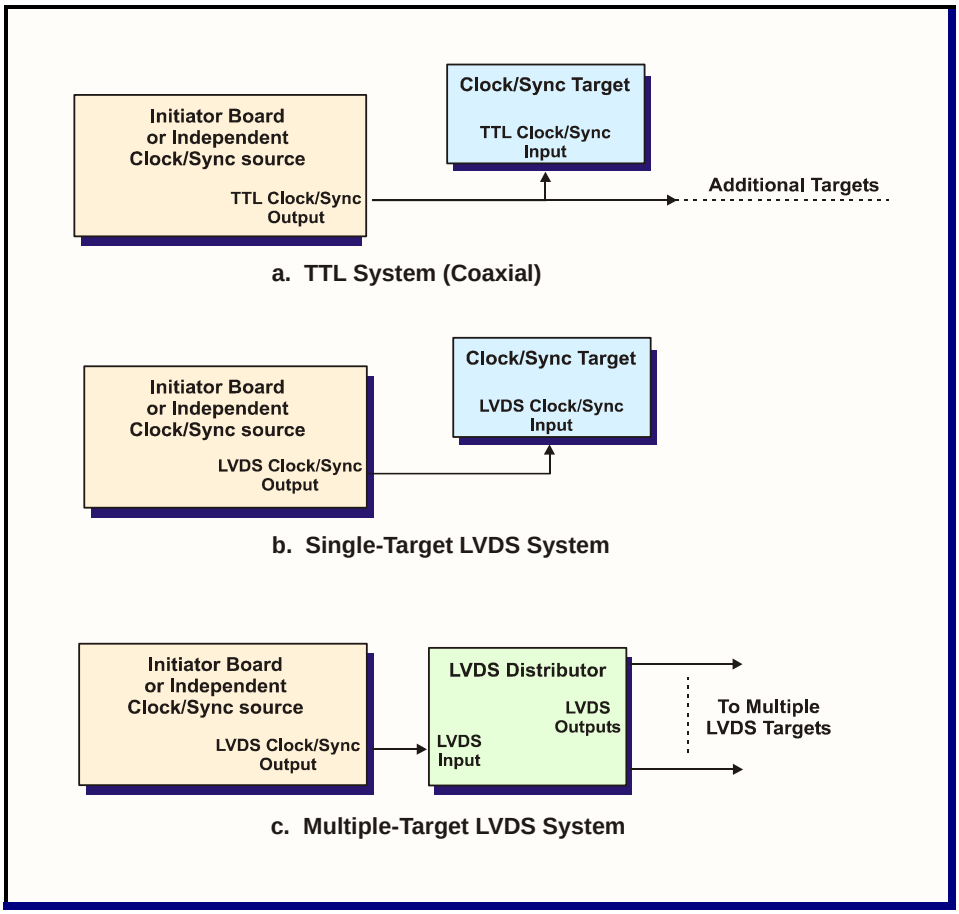

Figure 2.3-2. Multiboard Synchronization

2.3.2.1 External Clocking

The Clock I/O signal is an input if the board is software-configured as a ***target***, or is an output if the board is an ***initiator***. For a target board, a square-wave clock input signal controls the ADC's directly, with each positive edge of the clock initiating a single conversion. The range of acceptable external frequencies is defined in the product specification.

For an initiator, the clock output signal duplicates the internal ADC rate generator, with each positive edge of the clock representing a single ADC conversion. This signal can be used to clock the ADC's on other boards that are configured as targets.

2.3.2.2 External Sync

Like the clock I/O lines, sync I/O signals are inputs for targets or outputs for initiators. Coaxial sync signals are TTL-compatible, while ribbon-cable sync signals are LVDS. A positive transition of the sync signal into a target board initiates a single acquisition burst. As an output from an initiator, a positive sync transition coincides with the initiation of a burst. **A sync *input pulse* must remain high (asserted) for at least three ADC clock periods. Sync *output pulses* are asserted high for four ADC clock periods.**

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application. In most instances however, an interval of one year would be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

For High-Level and Wideband input configurations, all analog input channels are calibrated to a single internal reference voltage by an embedded autocalibration firmware utility. The procedure presented here describes the verification and adjustment of the internal reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC site.	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to two 0.024-inch square test posts.	---	---

2.5.2 Verification and Adjustment

This procedure describes the verification of the single reference voltage that ensures conformance to the product specification. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1. The board is assumed to be installed on an operational host board, and can be in any operating mode during the procedure.

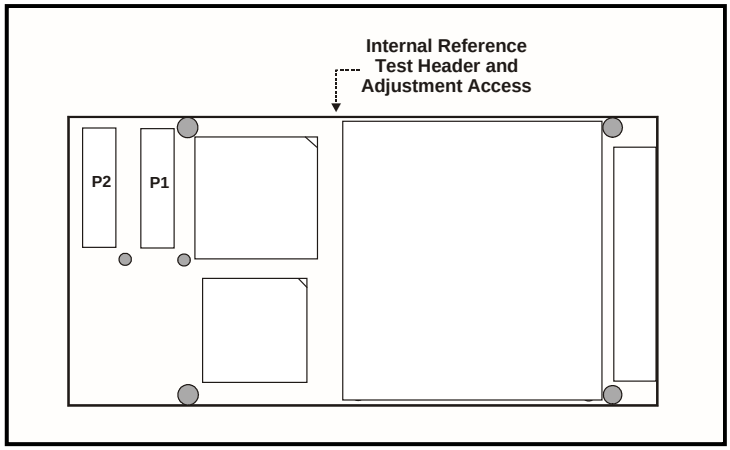

Figure 2.5-1. Reference Adjustment Access

1. Connect the digital multimeter between VTEST (+) Pin-2, and REF RTN (-) Pin-4 in the J4 test header (Figure 2.5-1).
2. If power has been removed from the board, apply power now and wait at least 10 minutes before proceeding..
3. Verify that the digital multimeter indication conforms to Table 2.5-2 for the applicable input configuration. If the indication is not within the specified range, adjust the INTERNAL REFERENCE trimmer until the indication conforms to the table.
4. Verification and adjustment is completed. Remove all test connections.

Table 2.5-2. Reference Values

Input Configuration *	Reference Value
High-Level	+9.990V ±0.004V
Wideband	+2.4975V ±0.0010V
Transformer-Coupled	+2.50V ±0.05V

* Ordering option. Refer to the product specification.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-14HSAI4 board is compatible with the PCI Local Bus specification, and supports auto-configuration at the time of power-up. A PLX™ PCI-9056 adapter operating in J-mode controls the PCI interface, and supports both 33MHz and 66MHz PCI clock frequencies, as well as 32-Bit PCI bus width. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All local data transfers are long-word D32. DMA access is supported for data transfers from the analog input data buffer.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	DEFA ULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	R/W	0000 4060h	Board Control Register (BCR)
0004	PRIMARY STATUS	R/W	0000 0000h	Critical status flags and events
0008	INPUT DATA BUFFER	RO	0000 XXXXh	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control
0010	BUFFER SIZE	RO	0000 0000h	Total samples present in the input buffer
0014	RATE GENERATOR ADJUST	R/W	0030 0050h	Rate generator frequency control
0018	RATE DIVISORS	R/W	1900 61A8h	Clock and sync frequency divisors.
001C	DECIMATION FACTOR	R/W	0000 0001h	Sampling decimation factor.
0020	CLOCKING AND SYNC CONTROL	R/W	0001 440Fh	Active-Channel selection. Clocking control. Sync control and trigger-level.
0024	BURST SIZE	R/W	0000 0004h	Total post-sync samples acquired during a burst.
0028	PRETRIGGER SIZE	R/W	0000 0004h	Total number of pretrigger samples.
002C	TEST UTILITY **	R/W	0000 0000h	Maintenance register. No user functions.
0030	BOARD CONFIGURATION	RO	000X XXXXh	Firmware revision and hardware options.
0034	Autocal Values **	R/W	0000 XXXXh	Autocal value readback.
0038-003C	(Reserved)	---	---	Inactive. Read back all-zero.

* R/W = Read/Write, RO = Read-Only. ** Maintenance register. No user functions Shown for reference only..

3.2 Board Control Register (BCR)

The Board Control Register (BCR) controls primary board functions, including analog input mode and range, and consists of 32 control bits and status flags. Table 3.2-1 provides a brief description of the BCR bit fields, as well as indicating associated text references.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D02	R/W	AIM[2..0]	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	(Reserved)	0	---	---
D04-D05	R/W	RANGE[1..0]	2h	Analog input range. Defaults to ±10V range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog input data format when asserted HIGH, or two's complement when LOW.	3.5.1.3
D07	R/W	DIFF CLK AND SYNC INPUTS	0	Selects the LVDS clock and sync inputs when HIGH, or the TTL inputs when LOW.	3.4.5
D08	R/W	ENABLE ADC CLOCKING	0	Enables ADC clocking when HIGH, disables clocking when LOW.	3.4.3.1
D09	R/W	ENABLE BURST	0	Enables triggered-burst mode when HIGH, disables bursting when LOW.	3.4.4.1
D10	R/W	ENABLE BURST MARKER	0	Enables insertion of a burst-trigger marker when bursting is enabled.	3.4.4.4
D11	R/W	SINGLE BURST	0	Terminates burst acquisition after a single burst.	3.4.4.1
D12	R/W	INPUT SYNC (Burst Trigger) *	0	Triggers a single burst of all active channels when bursting is enabled. Independent of all other sync sources. ***Forced high during a burst***.	3.4.4.1
D13	R/W	AUTOCAL *	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.6
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	3.5.2
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.5.1.2
D19-D31	RO	(Reserved)	000h	Inactive. Reads back as all-zero.	---

* Clears automatically when the associated operation is completed

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset, and should be required only once after the initial application of power.

3.3.2 Initialization

Internal control logic can be initialized without reconfiguration of the PCI registers by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. ***Initialization requires approximately 20 milliseconds for completion, including rate-generator settling***, and produces the following default conditions:

- All register defaults are invoked (Paragraph 3.1),
- The highest available analog input voltage range is selected (3.4.1),
- All channels are active (3.4.2),
- ADC clocking is configured for 2.0 MSPS, with Fgen = 50.000MHz (3.4.3),
- ADC clocking is disabled (3.4.3.1).
- Clocking and Sync Initiator modes are selected (3.4.3.1, 3.4.4.1),
- Sample decimation is disabled (3.4.3.2),
- Input bursting is disabled (3.4.4),
- Channel tags are enabled (3.5.1.1),
- Analog input data coding format is offset binary; Data packing is disabled (3.5.1),
- The analog input buffer is reset to empty (3.5.2),

Upon completion of initialization, the INITIALIZE control bit is cleared automatically. ***Altering the contents of any register during initialization may produce unpredictable behavior.***

3.4 Analog Input Parameters

3.4.1 Input Voltage Range

BCR control field RANGE[] selects the analog input voltage range, as shown in Table 3.4-1. For High-Level and Wideband board configurations, the analog inputs are DC-coupled and have bipolar voltage ranges. Transformer inputs are AC-coupled, with voltage ranges specified in Volts peak-peak.

Table 3.4-1. Input Voltage Range Selection

	ANALOG INPUT RANGE		
RANGE[1:0]	**High-Level Inputs**	**Wideband**	**Transformer**
0	±2.5 Volts	±0.625 Volts	1.0 Vp-p
1	±5 Volts	±1.25 Volts	2.0 Vp-p
2	±10 Volts	±2.5 Volts	2.0 Vp-p
3	(Reserved)	(Reserved)	(Reserved)

3.4.2 Active Channel Selection

Each input channel can be designated as either active or inactive through the Clocking and Sync control register shown in Table 3.4-2. A channel is active if the corresponding CHANNEL-xx ACTIVE control bit is HIGH, or is inactive if the bit is LOW. An inactive channel produces no data and occupies no space in the data buffer.

Table 3.4-2. Clocking and Sync Control Register

Offset: 0020h **Default: 0001 440Fh**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	CHANNEL-00 ACTIVE	1	Active-channel mask. HI for active; LOW for inactive
D01	R/W	CHANNEL-01 ACTIVE	1	
D02	R/W	CHANNEL-02 ACTIVE	1	
D03	R/W	CHANNEL-03 ACTIVE	1	
D04	R/W	CLOCK TARGET	0	Selects external hardware clock source when HI.
D05	RO	RATE GEN NOT READY	0	Internal rate generator settling interval.
D06-D07	R/W	SYNC-ON-LEVEL CHANNEL	0h	Sync-on-level input channel.
D08-D10	R/W	SYNC SOURCE	4h	Selects the sync (trigger) source: 0 => Internal rate generator,. 1 => SYNC TARGET (External hardware sync input), 2 => Sync on sync-channel value above Sync Level,. 3 => Sync on sync-channel value below Sync Level. 4 => Sync on BCR Input Sync only (S/W Sync). 5-7 => (Reserved).
D11	R/W	ENABLE INITIATOR OUTPUTS	0	Enable external clock and sync I/O as outputs.
D12	R/W	ENABLE PRETRIGGERING	0	Selects burst pretriggering when High. Disables bus access to the buffer while high. Clears when a sync event occurs. Forces single-burst mode.
D13	RO	PRETRIGGER ARMED *	0	Indicates that pretrigger sampling is completed. Clears when a sync event occurs.
D14-D15	R/W	SYNC-ON-LEVEL INTEGRATION	1h	Number of samples required to cause a sync-on-level sync event: 0 => MInimum delay (1-3 samples) 1 => 4 samples (Default) 2 => 16 samples 3 => 64 samples
D16-D17	R/W	SYNC-ON-LEVEL HOLDOFF	1h	Minimum number of sample clocks between sync-on-level sync events: 0 => 8 samples 1 => 64 samples (Default) 2 => 512 samples 3 => “Infinite” (One-shot sync)
D18-D31	R/W	SYNC LEVEL **	0000h	Sync-on-level threshold level

* Cleared by a sync event.

** SYNC LEVEL coding is the same as that selected for analog input coding (3.5.1.3).

3.4.3 ADC Clocking

A single sample is digitized in all active channels at each occurrence of the ADC clock. Consequently, the ADC sampling rate is identical to the ADC clocking frequency. Since the minimum ADC clocking frequency is specified as 1-MHz, lower effective sample rates are obtained by decimating the sample stream; that is, by retaining only selected samples at the lower rates.

3.4.3.1 Clock Source Selection

ADC clocking is enabled by setting the ENABLE ADC CLOCKING control bit HIGH in the BCR, and is disabled by clearing the bit LOW. The ADC sample clock can be derived from an internal adjustable rate generator or from an external clock source (Figure 3.4-1) The rate generator output is divided by an internal divider **Ndiv-clk** to produce an ADC clocking range from 1-50 MHz. Due to the pipelined nature of data from each ADC, initial data samples appear in the buffer approximately 12 ADC clock periods plus 500 nanoseconds after clocking is enabled.

NOTE: The ADC clock is used internally to control the input data stream. An external clock input, if selected, should be applied continuously.

If the default ***clock-initiato*r** mode is selected (i.e.: Clock-target mode deselected and initiator outputs enabled in the Clocking and Sync control register), the ADC clock is directed also to the External Clock I/O line as an output signal. If the clock-target mode is selected, the External Clock I/O line is configured as an input, and controls the ADC's directly.

The internal rate generator is available also as an input to the Sync control networks.

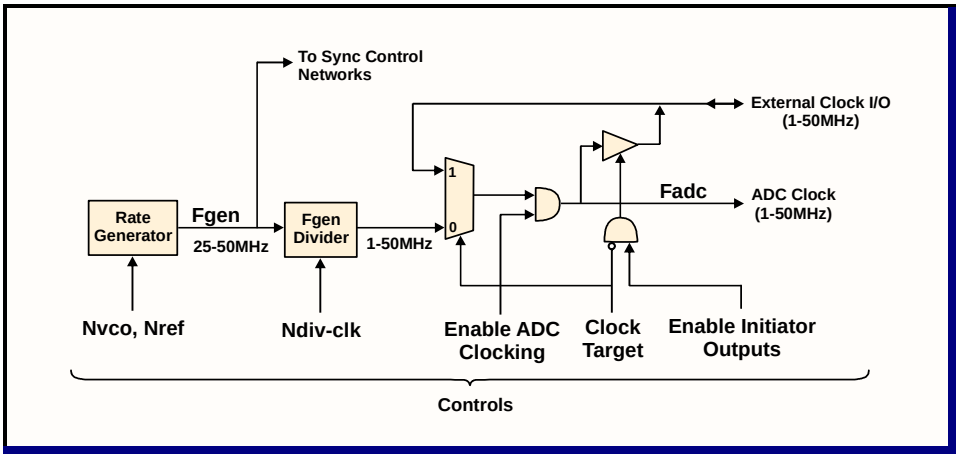

Figure 3.4-1. ADC Clock Selection

3.4.3.2 Sample Rate Control and Sample Decimation

The control parameters involved in establishing a specific sample rate are shown in Figure 3.4-2. In this illustration, the board is in the clock-initiator mode (CLOCK TARGET control bit deasserted), and the internal rate generator is selected.

The frequency **Fgen** of the rate generator is controlled by two integers **Nvco** and **Nref**, and is divided by a third integer **Ndiv-clk** to a clocking frequency **Fadc** with a range of 1-50MHz. **Fadc** is the ADC clocking frequency, and is the rate at which each ADC digitizes its analog input signal. A fourth integer **Ndec** divides the ADC sampling frequency further if effective sample rates below 1-MHz are required.

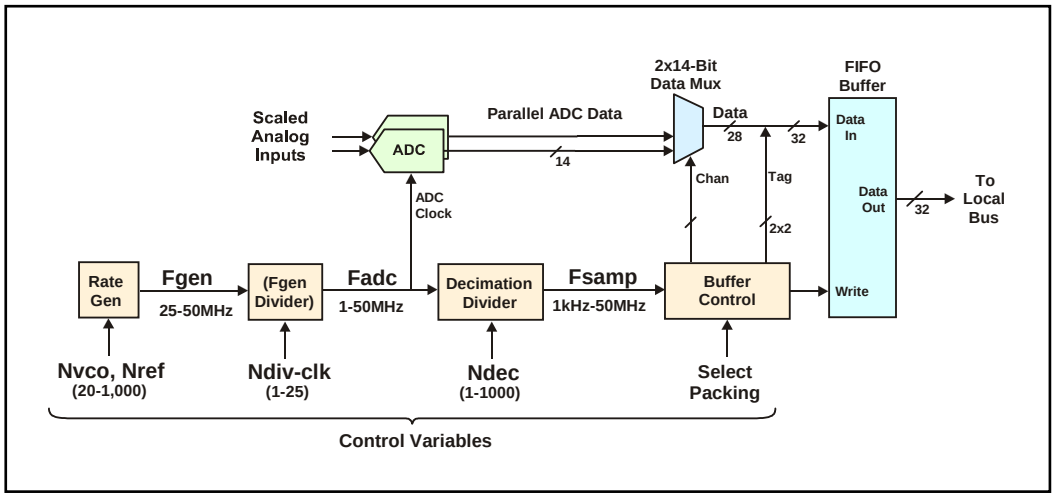

Figure 3.4-2. Clocking Control and Sample Decimation

The decimation divider produces a single ***sample clock*** for every **Ndec *ADC clocks***, and this sample clock initiates a single acquisition sequence in the buffer controller. An acquisition sequence stores a single value from each active channel into the buffer. The default decimation factor of '1' produces no decimation, and all digitized ADC values are acquired in the buffer.

The effective sample rate **Fsamp** is a function of the generator frequency **Fgen** and control variables **Ndiv-clk** and **Ndec**:

$$\mathbf{Fsamp} = \frac{\mathbf{Fgen}}{\mathbf{(Ndiv\text{-}clk * Ndec)}} \quad , \qquad \textbf{(3-1)}$$

where **Ndiv-clk** is an integer from 1 through 25, and **Ndec** has a range from 1 to 1,000.

Note: Because large decimation factors can degrade the signal-to-noise ratio (SNR), the clocking control parameters should be selected to use the lowest possible value for Ndec.

If the clock-initiator mode is selected (3.4.3.1), **Fgen** is generated by an internal phase-locked loop (PLL) rate generator that is controlled by an internal reference frequency **Fref** as:

$$\mathbf{Fgen} = \mathbf{Fref} * \frac{\mathbf{Nvco}}{\mathbf{Nref}} \quad , \qquad \textbf{(3-2)}$$

where integers **Nvco** and **Nref** both have a valid range from 20 to 1000. The standard value for **Fref** is **30.000 MHz**. **Fgen** should be constrained to the range of 25-50MHz.

Integers **Nvco** and **Nref** are controlled by the VCO RATE FACTOR and REF RATE FACTOR control fields in the Rate Generator Adjust register shown in Table 3.4-3. **Ndiv-clk** is controlled by the CLOCK RATE DIVISOR field in the Rate Divisors register (Table 3.4-4), and **Ndec** by the DECIMATION FACTOR field in the Decimation Factor register (Table 3.4-5).

Table 3.4-3. Rate Generator Adjust Register

Offset: 0014h **Default: 0030 0050h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	VCO RATE FACTOR (**Nvco**)	0050h	Rate generator frequency control. **Valid range: 20-1000.**
D16-D31	R/W	REF RATE FACTOR (**Nref**)	0030h	Rate generator frequency control. **Valid range: 20-1000.**

Note: The RATE GEN NOT READY flag in the Clocking and Sync control register goes HIGH when either the Rate Generator Adjust register or the Rate Divisors register is modified, or during initialization. This flag indicates that the rate generator is establishing a new frequency, and remains HIGH for approximately 20 milliseconds. While this flag is asserted, ADC data acquisition is disabled and ADC clocking is indeterminate.

Table 3.4-4. Rate Divisors Register

Offset: 0018h **Default: 1900 61A8h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D19	R/W	SYNC RATE DIVISOR **(Ndiv-sync**)	0 61A8h	Fgen divisor for sync (burst trigger). **Valid range: 10-1048575 (F_FFFFh)**
D20-D23	RO	(Reserved)	0h	Inactive. Reads back all-zero.
D24-D28	R/W	CLOCK RATE DIVISOR **(Ndiv-clk**)	19h	Fgen divisor for the ADC clock. **Valid range: 1-25 (19h)**
D29-D31	RO	(Reserved)	0h	Inactive. Reads back all-zero.

Table 3.4-5. Decimation Factor Register

Offset: 001Ch **Default: 0000 0001h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D09	R/W	DECIMATION FACTOR (**Ndec**)	001h	Sampling decimation factor. **Valid range: 1-1000.**
D10-D31	RO	(Reserved)	0000 00h	Inactive. Reads back all-zero.

Table 3.4-6 provides examples of sampling rates obtained by various sets of control parameters and frequency sources.

NOTE: The maximum sustainable sample rate (Table 3.4-7) depends upon the number of active channels and whether or not data packing is enabled (3.5.1.2). Exceeding the indicated maximum sample rate will produce unpredictable behavior.

Table 3.4-6. Sample Rate Control Examples

Clock Source:	Nvco	Nref	Ndiv-clk	Ndec	Fgen (MHz)	Fadc (MHz)	Fsamp
Rate Gen	**80**	**48**	**1**	**1**	50.000	50.000	**50.000 MHz**
	40	**24**	**25**	**1**	50.000	2.000	**2.000 MHz**
	40	**24**	**25**	**10**	50.000	2.000	**200.0 kHz**
	80	**48**	**25**	**1**	50.000	2.000	*** 2.000 MHz**
Ext Clk I/O @ 4 MHz	**---**	**---**	**---**	**400**	---	4.000	**10.00 kHz**

* Default configuration.

Note: If the last channel in an active channel group falls in the lower 16 bits of a longword when data-packing is selected (3.5.1.2), then the upper 16 bits of that longword contains the first channel in the next active group sample.

Table 3.4-7. Maximum Sustainable Sample Rates

NUMBER OF ACTIVE CHANNELS	DATA PACKING MODE	MAXIMUM SAMPLE RATE PER CHANNEL (MSPS)	MAXIMUM AGGREGATE SAMPLE RATE (MSPS)
1-2	**Nonpacked**	**25**	**50 MSPS**
~~3~~-4		~~**12.5**~~	~~**50 MSPS**~~
1-2	**Packed**	**50**	**100 MSPS**
~~3~~-4		~~**25**~~	~~**100 MSPS**~~

3.4.4 Burst Acquisition

Input data can be acquired in discrete bursts, in which each burst contains a specific number of samples from each active channel. A burst is initiated by a trigger, or sync-event, which can originate either locally on the board, or externally through the system I/O interface.

Note: The terms 'sync event' and 'trigger' are used interchangeably throughout this text.

3.4.4.1 Enabling and Triggering

To enable bursting, set the ENABLE BURST control bit high in the BCR. When this bit is set, each sync event initiates an acquisition burst in which a specific number of input samples is acquired. The INPUT SYNC bit in the BCR goes HIGH after a sync event when the first burst data value enters the buffer, indicating that a burst is in progress. This INPUT SYNC bit returns LOW when the last value enters the buffer. Sync events occurring during a triggered burst are ignored.

If SINGLE BURST is LOW in the BCR, burst acquisition proceeds continuously, with each sync event initiating a new burst. If SINGLE BURST is HIGH, acquisition terminates after a single burst, and subsequent sync events are ignored. To execute another burst after one has terminated, write a HIGH level to the already-asserted ENABLE BURST control bit in the BCR.

Figure 3.4-3 illustrates the available sync sources, as controlled through the BCR and the Clocking and Sync Control register. A Sync event can be generated at any time by setting the INPUT SYNC control bit HIGH in the BCR. The control bit reads back LOW until a sync event occurs, then goes HIGH for the remainder of the burst.

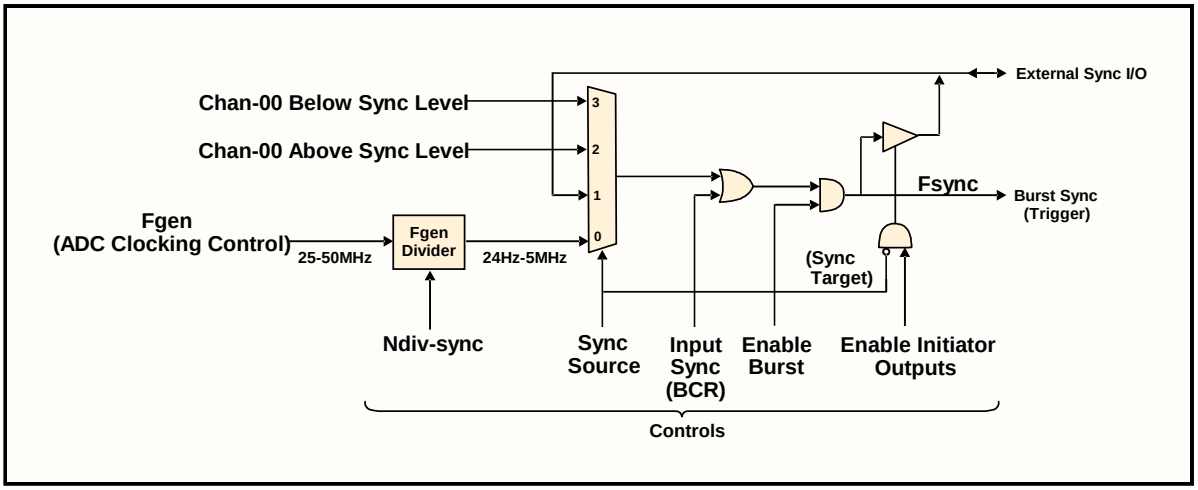

Figure 3.4-3. Burst Sync Selection

For all Sync Source selections except **Sync Target**, the External Sync I/O line is an output if ENABLE INITIATOR OUTPUTS is HIGH. If **Sync Target** is selected, the External Sync I/O line becomes an input, and the sync event is received directly from an external hardware source.

NOTE: Due to internal pipelining, the latency of an internal (recognized) sync event relative to the associated sync condition can be a high as ten ADC sample clocks. This latency limits the maximum triggering rate to approximately Fsamp/10, and can be minimized by selecting the maximum practical sample rate.

If the Internal Rate Generator is selected (default trigger source), the local rate generator frequency **Fgen** is available through a divider controlled by **Ndiv-sync** (Table 3.4-4), which provides local sync rates from 24Hz to as high as 5MHz at Fsamp = 50 MHz; (see note above):

$$\textbf{Fsync (MHz)} = \frac{\textbf{Fgen (MHz)}}{\textbf{Ndiv-sync}}, \qquad \textbf{(3-3)}$$

where **Ndiv-sync** is an integer from 10 through 1048575.

3.4.4.2 Sync On Level

If either of the two "***sync on sync-channel***" sync sources are selected in the Clocking and Sync control register, a sync event occurs when the values acquired in the selected ***sync-channe***l become either greater than or less than the level specified in the SYNC LEVEL field, as shown below:

Sync Source Selection	Condition for Sync Event
Sync on sync-channel above Sync Level	Sync-channel value is greater than the sync level.
Sync on sync-channel below Sync Level	Sync-channel value is less than the sync level.

The SYNC-ON-LEVEL CHANNEL control field designates any of the active input channels as the ***sync-channel***.

The number of consecutive samples that must meet the selected requirement before a sync-event occurs is selected with the SYNC-ON- LEVEL INTEGRATION control field. After a sync event occurs, subsequent events are ignored for an interval corresponding to the number of ***sample clocks*** specified by the SYNC-ON-LEVEL HOLDOFF control field. Selection of "infinite" for holdoff creates a one-shot situation, in which only the first sync event will be acknowledged. To recover from the "infinite" holdoff mode after sync occurs, clear the ENABLE BURST control bit in the BCR.

Note: The holdoff interval commences immediately after the integration interval, and the minimum interval between sync events is:

Minimum Sync-on-level Interval = Holdoff + Integration.

3.4.4.3 Burst Size

The Burst Size register shown in Table 3.4-8 defines the total number of input sample clocks that occur during a burst. For nonpacked data (3.5.1.1), the number of input samples acquired per channel equals BURST SIZE.

Table 3.4-8. Burst Size Register

Offset: 0024h **Default: 0000 0004h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D19	R/W	BURST SIZE	0 0004h	Total number of samples per active channel acquired after a sync event. **0 => continuous sampling after sync event.**
D20-D31	RO	(Reserved)	000h	Inactive. Reads back as all-zero.

If data packing (3.5.1.2) is selected during burst acquisition, the number of complete samples contained in each longword varies, depending upon the number of active channels. To ensure that all channels in each sample are acquired during a burst, and that no partial samples are acquired, the relationship between BURST SIZE and the number of packed samples acquired from each channel is established as shown in Table 3.4-9.

Table 3.4-9. Packed Data Burst Acquisition

ACTIVE CHANNELS	SAMPLES PER LWORD	TOTAL LWORDS *	TOTAL SAMPLES *
1	2	SIZE	2* SIZE
2	1	SIZE	SIZE
3	2/3	3 * SIZE	2 * SIZE
4	1/2	2 * SIZE	SIZE

* "SIZE" = BURST SIZE or PRETRIGGER SIZE.

Note: A value of zero for BURST SIZE produces continuous sampling after a sync event. The event clears the ENABLE BURST control bit in the BCR, and sampling proceeds indefinitely until either the ENABLE BURST control bit is reasserted or ADC clocking is disabled. The burst marker (3.4.4.4) is disabled when operating in this mode.

3.4.4.4 Burst Marker

If the ENABLE BURST MARKER control bit is set HIGH in the BCR, the final data sample in a burst is followed by an all-zero longword end-of-burst (EOB) marker, and input data values are constrained to the range from 0001h to 3FFFh. The marker is an all-zero *longword* value for both packed and nonpacked data. The burst marker is not considered as a data value, and does not affect the relationship between the BURST SIZE variable and the number of samples acquired during a burst.

Notes: If the burst marker is enabled during pretriggering (3.4.4.5), an all-zero marker is inserted immediately after the last pretrigger sample, as well as after the last posttrigger sample.

Burst markers, if enabled, do not affect the selected burst size or pretrigger size, but do occupy space within the buffer.

3.4.4.5 Pretriggering

Pretriggering permits the acquisition of a specific number of "***pretrigger***" input samples that occur immediately prior to a sync event, in addition to the "***posttrigger***" samples occurring after the event. This triggering mode is selected by setting the ENABLE PRETRIGGERING control bit HIGH in the Clocking and Sync register. Sampling commences immediately when this bit is ENABLE BURST are asserted .

Once a pretriggered burst has been initiated, the buffer is closed (inaccessible from the PCIbus) until after the sync event occurs, as indicated by the PRETRIGGER ARMED status bit going LOW.

The number of pretrigger samples per channel is specified in the Pretrigger Size register shown in Table 3.4-10. When the number of accumulated samples acquired equals the PRETRIGGER SIZE value, the PRETRIGGER ARMED status bit goes HIGH to indicate that the controller is waiting for a sync event. While PRETRIGGER ARMED is HIGH, new data replaces old data until a sync event occurs.

Note: If data packing (3.5.1.2) is selected during a burst, the relationship between PRETRIGGER SIZE and the number of samples acquired depends upon the number of active channels, as described in Paragraph 3.4.4.3 and Table 3.4-9.

Table 3.4-10. Pretrigger Size Register

Offset: 0028h **Default: 0000 0004h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D17	R/W	PRETRIGGER SIZE	0 0004h	Total number of samples per active channel acquired before a sync event. **Valid range = 0_0002h through 3_FFFFh**.
D18-D31	RO	(Reserved)	0000 0h	Inactive. Reads back as all-zero.

When a sync event occurs, the PRETRIGGER ARMED bit goes LOW to indicate that the pretriggering interval has been terminated and that posttrigger data is being acquired. At the end of the posttrigger interval, when BURST SIZE posttrigger samples have been acquired, the burst terminates and acquisition ceases.

The following sequence illustrates a typical pretriggered burst (Figure 3.4-4):

1. In the BCR, clear the ENABLE ADC CLOCKING and ENABLE BURST control bits LOW.
2. Write the required burst size to the Burst Size register, and write the required number of pretrigger sample clocks (samples per channel) to the Pretrigger Size register.
3. Select the required Clocking mode and SYNC SOURCE in the Clocking and Sync control register. Set the ENABLE PRETRIGGERING control bit HIGH, and select the SYNC LEVEL if necessary.
4. To initiate the burst, set the ENABLE ADC CLOCKING and ENABLE BURST control bits HIGH in the BCR. Also set the ENABLE BURST MARKER control HIGH if burst marking is required.
5. The number of samples specified in the Pretrigger Size register are acquired from each active channel, then are rotated out continuously as new samples arrive (i.e.: ring-buffered) until a sync event occurs. This ensures that the pretrigger samples will be contiguous with the samples acquired after a sync event.

   Sync events are ignored during the pretrigger interval. When pretrigger sampling is completed, the PRETRIGGER ARMED status flag is asserted and a subsequent sync event will be acknowledged. The PRETRIGGER ARMED flag is available as a primary status flag (Table 3.7-1).
6. After the burst is armed (PRETRIGGER ARMED = HIGH), a sync event will terminate the pretrigger sample rotation process, and subsequent samples will be appended to the pretrigger samples. The burst terminates when the total number of samples acquired ***after the sync event*** equals the number determined by the Burst Size register.

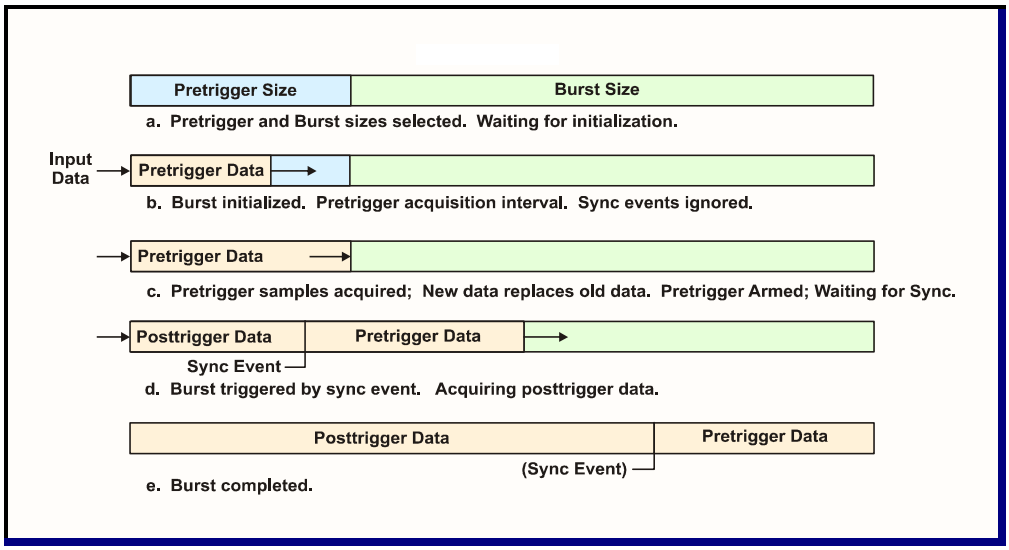

Figure 3.4-4. Pretriggered Burst Sequence

Note: To avoid overwriting data from a previous burst, pretriggered bursts are always single bursts, regardless of the state of the SINGLE BURST control bit in the BCR. To execute a new pretriggered burst after a previous burst has terminated, write a HIGH level to the already-asserted ENABLE BURST control bit in the BCR.

3.4.5 Multiboard Synchronization

Multiple boards can be interconnected externally to produce synchronous analog input sampling. Section 2.3.2 describes the available multiboard configurations. One of the boards is designated as the ***Initiator***, and the boards to be synchronized to the initiator are designated as ***targets***. The initiator/target status can be assigned independently for the clock and sync functions on any board. For example, a clock-initiator (Section 3.4.3) can also be designated as either a sync-initiator or a sync-target (Section 3.4.4).

Note: An external sync input pulse must be LOW for at least three ADC-clock periods to ensure acknowledgement.

For initiators, both the differential (LVDS) and TTL clock and sync *outputs* are active. For designated targets, the TTL clock and sync *inputs* from the coaxial connectors are selected by default. To select the differential clock and sync input signals at the ribbon cable connector, set the DIFF CLK AND SYNC INPUTS control bit HIGH in the BCR. When configured as outputs, the clock and sync TTL and differential *outputs* are active, regardless of the state of the DIFF CLK AND SYNC INPUTS control bit.

Note: To avoid contention on the SYNC and CLOCK I/O lines at power-up in multiboard configurations, the ENABLE INITIATOR OUTPUTS control bit in the Clocking and Sync control register defaults LOW, and disables the clock and sync output drivers. Only one board can be designated as a clock or sync initiator.

3.5 Analog Input Data Control

3.5.1 Input Data Organization

Buffered data can be arranged in either a nonpacked (16-Bit) or packed (32-Bit) configuration, and appears as a single 32-Bit long-word in the Input Data Buffer data register. Buffer capacity is 256K samples for nonpacked data, or 512K samples for packed data. Input data can be identified with a channel tag, and both packed and nonpacked data can be supported with a burst marker (3.5.1.2). An empty buffer returns an indeterminate value.

3.5.1.1 Nonpacked Data

Nonpacked analog input data is right-justified to the LSB, and occupies bit positions D00 through D13 (Table 3.5-1). Bits D14-D15 can be configured by the DISABLE CHANNEL TAG control bit in the Buffer Control register (Table 3.5-5). If this control bit is LOW, Bits D14-D15 contain the associated channel number. If the control bit is HIGH, data bits D14-D15 either are all-zero if offset binary coding is selected, or become the data sign extension if two-s complement coding is selected (Paragraph 3.5.1.3).

Table 3.5-1. Input Data Buffer; Nonpacked Data

Offset: 0008h **Default: N/A**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D12	RO	DATA01 - DATA12	Intermediate data bits
D13	RO	DATA13	Most significant data bit
D14-D15	RO	0h or 3h *	All-zero or two's complement sign extension
		Channel Tag **	Channel number
D16-D31	RO	(Inactive)	Reads back all-zero

* Channel tag disabled. ** Channel tag enabled.

Each acquisition sequence commences with the lowest-numbered active channel. and proceeds upward to the highest active channel (Table 3.5-2).

Table 3.5-2. Data Organization; Burst Marker Disabled

	Buffer Data Field			
	ENABLE DATA PACKING = Low		ENABLE DATA PACKING = High	
Buffer Lword Order	D[31..16]	D[15..0] *	D[31..16] *	D[15..0] *
---	---	---	---	---
Last -3	0000h	Chan 00 Data	Chan 01 Data	Chan 00 Data
Last -2	0000h	Chan 01 Data	Chan 03 Data	Chan 02 Data
Last -1	0000h	Chan 02 Data	Chan 01 Data	Chan 00 Data
Last	0000h	Chan 03 Data	Chan 03 Data	Chan 02 Data
---	---	---	---	---

* Includes channel tag or sign extension.

3.5.1.2 Packed Data

Setting the ENABLE DATA PACKING control bit HIGH in the BCR selects the data packing mode, in which two consecutive 16-bit data values are packed into a single 32-Bit local data longword. Each acquisition sequence commences with the lowest-numbered active channel positioned in the D00-D15 field, the second in the D16-D31 field, and continues in this sequence through all active channels (Table 3.5-2). The lowest-numbered active channel immediately follows the highest active channel, regardless of its position in the lower or upper word. A single active channel appears in both lower and upper words.

If burst marking is enabled (3.4.4.4), an all-zero marker is inserted directly after the last channel in each burst (Table 3.5-3), and every all-zero data value is forced to 0001h.

Table 3.5-3. Data Organization; Burst Marker Enabled

	Buffer Data Field			
	ENABLE DATA PACKING = Low		ENABLE DATA PACKING = High	
Buffer Lword Order	D[31..16]	D[15..0] *	D[31..16] *	D[15..0] *
---	---	---	---	---
Last -3	0000h	Chan 00 Data	Chan 01 Data	Chan 00 Data
Last -2	0000h	Chan 01 Data	Chan 03 Data	Chan 02 Data
Last -1	0000h	Chan 02 Data	Chan 01 Data	Chan 00 Data
Last	0000h	Chan 03 Data	Chan 03 Data	Chan 02 Data
EOB Marker	0000h	0000h	0000h	0000h
---	---	---	---	---

* Includes channel tag or sign extension.

3.5.1.3 Data Coding Format

Analog input data is arranged as 14 right-justified data bits with the coding conventions shown in Table 3.5-4. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR, and extends the sign bit through D15 unless channel tagging is selected (3.5.1.1). Unless indicated otherwise, offset binary coding is assumed throughout this document.

Table 3.5-4. Input Data Coding; 14-Bit Data

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	3FFF	1FFF
Zero	2000	0000
Zero minus 1 LSB	1FFF	3FFF
Negative Full Scale	0000	2000

3.5.2 Input Data Buffer Control

The Input Buffer control register shown in Table 3.5-5 controls and monitors the flow of data through the analog input data buffer. Asserting the CLEAR BUFFER control bit HIGH clears, or empties, the buffer. The THRESHOLD FLAG bit is HIGH when the number of Lword locations occupied in the input data buffer ***exceeds the*** *THRESHOLD VALUE*, and is LOW if the number is equal to or less than the threshold. The threshold flag is available as a primary status flag (3.7).

Table 3.5-5. Input Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D17	R/W	THRESHOLD VALUE	3 FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of Lword locations occupied in the input buffer ***exceeds*** the THRESHOLD VALUE.
D20	R/W	DISABLE BUFFER	0	Prevents input data from entering the buffer.
D21	R/W	DISABLE CHANNEL TAG	0	Designates data field D14-D15 as a sign extension when HIGH, or as a channel tag when LOW.
D22-D31	RO	(Reserved)	000h	Inactive. Reads back all-zero.

*Clears automatically within 5 microseconds of being set

Input data is discarded if the DISABLE BUFFER control bit is set HIGH, but data already present in the buffer is unaffected and can be accessed from the PCIbus.

The Buffer Size register shown in Table 3.5-6 contains the total number of Lword buffer locations occupied with valid data, and is updated continuously.

Buffer underflow and overflow flags in the BCR indicate that the buffer has been read while empty or written to when full, respectively. These situations indicate either data loss or corruption. Once set HIGH, each flag remains HIGH until cleared, either by directly clearing the bit LOW, by clearing the buffer, or by initializing the board. When selected, the level-detected 'Buffer UnderFlow/Overflow' response bit in the PSR (Table 3.7-1) is asserted if either the underflow or overflow flag is asserted.

Table 3.5-6. Buffer Size Register

Offset: 0010h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of buffer Lword locations containing valid input data.
D19-D31	RO	(Inactive)	0000h	---

3.5.3 Analog Input Function Modes

For High-level and Wideband board configurations, BCR control field AIM[] selects the analog input signal source, and provides selftest modes for monitoring the integrity of the analog input networks. Table 3.5-7 summarizes the input function modes.

Table 3.5-7. Analog Input Function Selection

AIM[2:0]	FUNCTION OR MODE (Wideband and Hi-Level Configurations)
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Note: For the Transformer-Coupled input configuration, this control field has no effect, and the system inputs are always selected

3.5.3.1 System Analog Inputs

With the default value of 'Zero' selected for the AIM[] field in the BCR, all ADC channels are connected to the system analog inputs from the system I/O connector.

3.5.3.2 Selftest Modes

In the High-Level and Wideband selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and the averaged values of multiple samples should be used for critical measurements.

The ZERO selftest applies a Zero reference signal to all input channels, and should produce a nominal midscale reading of 2000h (offset binary). For the +VREF test, a precision reference voltage equal to 99.90% of the positive fullscale value for the selected input range is applied to the input channels, and should produce a nominal reading of 0000 3FF8h.

3.6 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- A PCIbus or software reset,
- An input range change,
- A sample rate change, if greater than 10-percent.

Note: Autocalibration uses the selected ADC clock source (3.4.3.1) when acquiring input data, and requires that the clock be active. An inactive ADC clock source may cause autocalibration to pause indefinitely.

During autocalibration, no control settings are altered and external analog input signals are ignored. Autocalibration overrides the ENABLE ADC CLOCKING control bit in the BCR, if deasserted, and uses the currently selected input range and ADC clock during the calibration process. Upon completion of autocalibration, the buffer is cleared automatically and normal operation resumes. **The autocalibration function applies only to the High-Level and Wideband input configurations, and is inactive for Transformer-coupled inputs.**

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of approximately 6 seconds. Completion of the operation can be detected either by selecting the associated status flag in Table 3.7-1, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. ***AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs, or if autocalibration is aborted by clearing the AUTOCAL control bit during the calibration sequence.***

3.7 Primary Status Register

Critical status flags are consolidated into a single Primary Status register (Table 3.7-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected.

Response status bits can be either level-detected or edge-detected, as indicated in the table. A ***level-detected*** response bit follows the associated event or process in real time, and is high if the event is currently true, or is low otherwise.

An ***edge-detected*** response bit is latched high when the associated event occurs. The latched bit remains high until cleared from the PCI bus, either by clearing the response bit, *or by clearing the associated selection bit*.

NOTE: A "one" written to any response bit is ignored. Edge-detected response bits can *only* be cleared LOW from the PCI bus.

Table 3.7-1. Primary Status Register

Offset 0x0004 **Default 0x0000 0000**

SELECTION BIT [1]	STATUS EVENT	RESPONSE BIT [2]	REFERENCE	DETECTION METHOD
D00	(Reserved)	D16	---	Level
D01	Autocal in progress	D17	3.6	
D02	Triggered Burst in progress	D18	3.4.4	
D03	Buffer Threshold Flag	D19	3,5,2	
D04	Burst Pretrigger-Armed Interval	D20	3.4.4.5	
D05	Buffer Underflow/Overflow	D21	3.5.2	
D06	(Reserved)	D22	---	
D07	(Reserved)	D23	---	
D08	Autocal completed	D24	3.6	Edge
D09	Input Burst triggered	D25	3.4.4	
D10	Input Burst completed	D26		
D11	Buffer Threshold flag LOW-to-HIGH transition	D27	3.5.2	
D12	Buffer Threshold flag HIGH-to-LOW	D28		
D13	Pretrigger Armed	D29	3.4.4.5	
D14	(Reserved)	D30	---	
D15	(Reserved)	D31	---	

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Remains HIGH until cleared LOW.

A PCI interrupt (INT A#) can be generated in response to the assertion of any response flag, by enabling the PCI local interrupt response through the PCI9056 configuration registers. The interrupt flag will remain asserted until all response bits are cleared.

3.8 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master, in either DMA Channel 00 or Channel 01. Set Bit 02 in the PCI Command register HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a detailed description of DMA configuration registers.

3.8.1 Block Mode

Table 3.8-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.8.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.8-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained in the buffer until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

3.9 Board Configuration Register

The read-only Board Configuration register shown in Table 3.9-1 contains the existing firmware revision and the configuration of optional features.

Table 3.9-1. Board Configuration Register

Offset: 0000 0030h **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16	High if the board contains only Channels 00 and 01.
D17-D18	Input Configuration: 0 => High-Level inputs 1 => Wideband inputs 2 => Transformer-Coupled inputs. 3 => (Reserved)
D19	Input Impedance: 0 => 2 Megohms 1 => 50 Ohms
D20-D31	(Reserved)

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

For the High-Level and Wideband input configurations, each of the **two** analog input channels contains a selftest input switching network, a scaling network, calibration DAC's and a dedicated 14-Bit ADC (Figure 4.1-1). Optional transformer-coupled inputs are routed directly to the ADC's to provide the highest possible input bandwidth. (All references to configuration switches, input scaling and calibration DAC's pertain to the High-Level and Wideband input configurations).

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller. +5 VDC power from the PCIbus is converted into regulated power voltages for the internal analog networks.

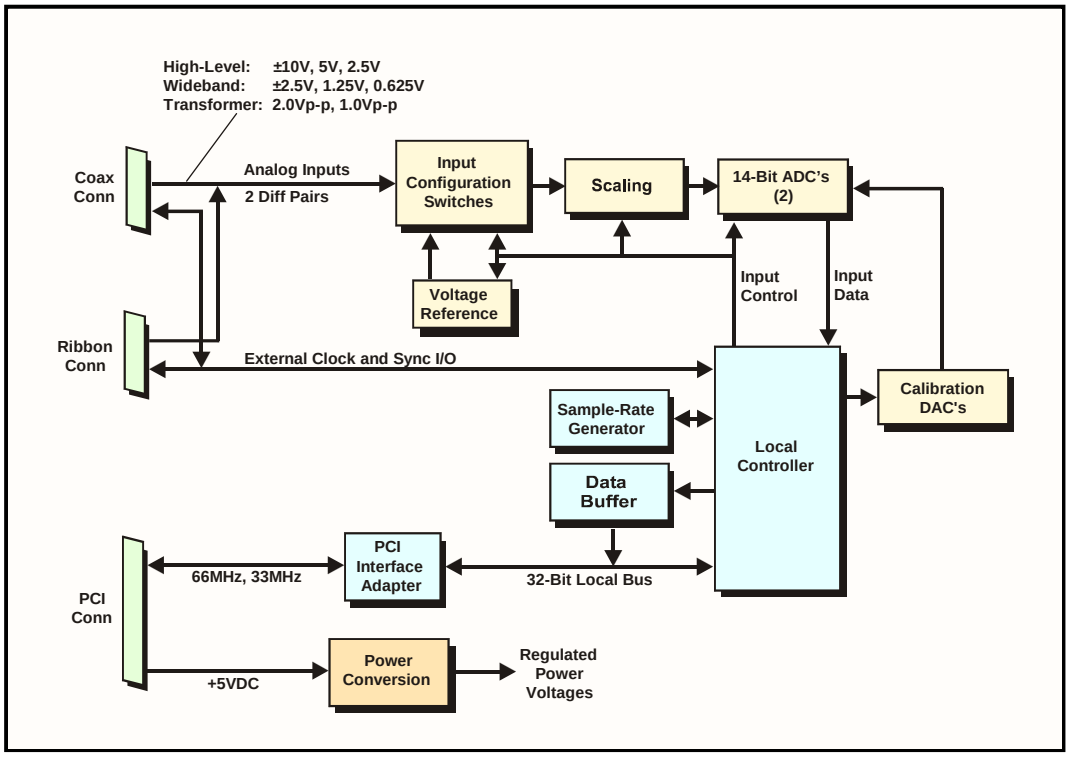

Figure 4.1-1. Functional Block Diagram

Configuration switches at the inputs provide test signals for autocalibration of all input channels, and for verification of board integrity by the host. The input range is controlled both by directly scaling the signal level, and by adjusting the ADC reference voltage. Autocalibration implements calibration DAC's to correct each input channel for gain and offset errors. A 1-Megabyte FIFO buffer accumulates analog input data for subsequent retrieval by a PMC host.

Analog input sampling and burst-triggering on multiple target boards can be synchronized to a single software-designated initiator board.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the configuration switches shown in Figure 4.1-1. During normal operation, each pipelined ADC receives system analog input signals from the input connector. For selftest and autocalibration operations, the internal voltage reference can be routed through the configuration switches to the ADC. A scaling network selects the high and mid ranges, while the low range combines mid-range scaling with a reduced ADC reference voltage..

The local controller adds a channel tag to the 14-Bit parallel data from each active ADC, and multiplexes the data into either a 16-Bit or 32-Bit data path before loading the data into the FIFO buffer. The 16-Bit data path represents nonpacked data acquisition, while the 32-Bit path packs two data values into a single longword in the buffer.

4.3 ADC Clocking

The ADC sample clock can be derived from an internal adjustable frequency servo or from an external clock source. An internal adjustable divider provides a range of direct sample rates from 1.0MSPS to 50MSPS. A second divider provides sample decimation to effectively extend the minimum sample rate down to approximately 1.0KSPS

4.4 Data Buffer

A 1-Megabyte FIFO buffer accumulates analog input data for subsequent retrieval through the PCIbus. The effective width of the buffer can be software-configured as either 16 bits for nonpacked data, or as 32 bits with local data packing. A 'size' register tracks the number of values in the buffer, and an adjustable threshold can be used to assert a status flag when the number of values in the buffer moves above or below a selected count.

Buffer DMA transfers can support a theoretical maximum sustainable transfer rate of 100 megasamples per second (200 MB/sec). However, host architecture, the operating system, and bus arbitration will reduce the actual maximum rate to a lower value.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

Configuration switches select an internal voltage reference to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are stored in serial calibration DAC's, which apply the corrections continuously during normal operation. Correction values are retained until either the autocalibration sequence is repeated, a PCI Reset occurs, or power is removed.

4.6 Power Control

Regulated supply voltages of ±5 VDC and ±14 VDC are required for the internal analog networks. These voltages are derived from the +5-Volt input provided by the PCI bus, first by switching preregulators, and then by linear postregulators to achieve close regulation and minimum noise.

APPENDIX A

Local Control Register Quick Reference

APPENDIX A

Local Control Register Quick Reference

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	DEFA ULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	R/W	0000 4060h	Board Control Register (BCR)
0004	PRIMARY STATUS	R/W	0000 0000h	Critical status flags and events
0008	INPUT DATA BUFFER	RO	0000 XXXXh	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control
0010	BUFFER SIZE	RO	0000 0000h	Total samples present in the input buffer
0014	RATE GENERATOR ADJUST	R/W	0030 0050h	Rate generator frequency control
0018	RATE DIVISORS	R/W	1900 61A8h	Clock and sync frequency divisors.
001C	DECIMATION FACTOR	R/W	0000 0001h	Sampling decimation factor.
0020	CLOCKING AND SYNC CONTROL	R/W	0001 440Fh	Active-Channel selection. Clocking control. Sync control and trigger-level.
0024	BURST SIZE	R/W	0000 0004h	Total post-sync samples acquired during a burst.
0028	PRETRIGGER SIZE	R/W	0000 0004h	Total number of pretrigger samples.
002C	TEST UTILITY **	R/W	0000 0000h	Maintenance register. No user functions.
0030	BOARD CONFIGURATION	RO	000X XXXXh	Firmware revision and hardware options.
0034	Autocal Values **	R/W	0000 XXXXh	Autocal value readback.
0038-003C	(Reserved)	---	---	Inactive. Read back all-zero.

* R/W = Read/Write, RO = Read-Only. ** Maintenance register. No user functions Shown for reference only..

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D02	R/W	AIM[2..0]	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	(Reserved)	0	---	---
D04-D05	R/W	RANGE[1..0]	2h	Analog input range. Defaults to ±10V range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog input data format when asserted HIGH, or two's complement when LOW.	3.5.1.3
D07	R/W	DIFF CLK AND SYNC INPUTS	0	Selects the LVDS clock and sync inputs when HIGH, or the TTL inputs when LOW.	3.4.5
D08	R/W	ENABLE ADC CLOCKING	0	Enables ADC clocking when HIGH, disables clocking when LOW.	3.4.3.1
D09	R/W	ENABLE BURST	0	Enables triggered-burst mode when HIGH, disables bursting when LOW.	3.4.4.1
D10	R/W	ENABLE BURST MARKER	0	Enables insertion of a burst-trigger marker when bursting is enabled.	3.4.4.4
D11	R/W	SINGLE BURST	0	Terminates burst acquisition after a single burst.	3.4.4.1
D12	R/W	INPUT SYNC (Burst Trigger) *	0	Triggers a single burst of all active channels when bursting is enabled. Independent of all other sync sources. ***Forced high during a burst.***	3.4.4.1
D13	R/W	AUTOCAL *	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.6
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	3.5.2
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.5.1.2
D19-D31	RO	(Reserved)	000h	Inactive. Reads back as all-zero.	---

* Clears automatically when the associated operation is completed

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Input Voltage Range Selection

	ANALOG INPUT RANGE		
RANGE[1:0]	**High-Level Inputs**	**Wideband**	**Transformer**
0	±2.5 Volts	±0.625 Volts	1.0 Vp-p
1	±5 Volts	±1.25 Volts	2.0 Vp-p
2	±10 Volts	±2.5 Volts	2.0 Vp-p
3	(Reserved)	(Reserved)	(Reserved)

Table 3.4-2. Clocking and Sync Control Register

Offset: 0020h **Default: 0001 440Fh**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	CHANNEL-00 ACTIVE	1	Active-channel mask. HI for active; LOW for inactive
D01	R/W	CHANNEL-01 ACTIVE	1	
D02	R/W	CHANNEL-02 ACTIVE	1	
D03	R/W	CHANNEL-03 ACTIVE	1	
D04	R/W	CLOCK TARGET	0	Selects external hardware clock source when HI.
D05	RO	RATE GEN NOT READY	0	Internal rate generator settling interval.
D06-D07	R/W	SYNC-ON-LEVEL CHANNEL	0h	Sync-on-level input channel.
D08-D10	R/W	SYNC SOURCE	4h	Selects the sync (trigger) source: 0 => Internal rate generator,. 1 => SYNC TARGET (External hardware sync input), 2 => Sync on sync-channel value above Sync Level,. 3 => Sync on sync-channel value below Sync Level. 4 => Sync on BCR Input Sync only (S/W Sync). 5-7 => (Reserved).
D11	R/W	ENABLE INITIATOR OUTPUTS	0	Enable external clock and sync I/O as outputs.
D12	R/W	ENABLE PRETRIGGERING	0	Selects burst pretriggering when High. Disables bus access to the buffer while high. Clears when a sync event occurs. Forces single-burst mode.
D13	RO	PRETRIGGER ARMED *	0	Indicates that pretrigger sampling is completed. Clears when a sync event occurs.
D14-D15	R/W	SYNC-ON-LEVEL INTEGRATION	1h	Number of samples required to cause a sync-on-level sync event: 0 => MInimum delay (1-3 samples) 1 => 4 samples (Default) 2 => 16 samples 3 => 64 samples
D16-D17	R/W	SYNC-ON-LEVEL HOLDOFF	1h	Minimum number of sample clocks between sync-on-level sync events: 0 => 8 samples 1 => 64 samples (Default) 2 => 512 samples 3 => “Infinite” (One-shot sync)
D18-D31	R/W	SYNC LEVEL **	0000h	Sync-on-level threshold level

* Cleared by a sync event.

** SYNC LEVEL coding is the same as that selected for analog input coding (3.5.1.3).

Table 3.4-3. Rate Generator Adjust Register

Offset: 0014h **Default: 0030 0050h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	VCO RATE FACTOR (**Nvco**)	0050h	Rate generator frequency control. **Valid range: 20-1000**.
D16-D31	R/W	REF RATE FACTOR (**Nref**)	0030h	Rate generator frequency control. **Valid range: 20-1000.**

Table 3.4-4. Rate Divisors Register

Offset: 0018h **Default: 1900 61A8h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D19	R/W	SYNC RATE DIVISOR **(Ndiv-sync**)	0 61A8h	Fgen divisor for sync (burst trigger). Valid range: 10-1048575 (F FFFFh)
D20-D23	RO	(Reserved)	0h	Inactive. Reads back all-zero.
D24-D28	R/W	CLOCK RATE DIVISOR **(Ndiv-clk**)	19h	Fgen divisor for the ADC clock. Valid range: 1-25 (19h)
D29-D31	RO	(Reserved)	0h	Inactive. Reads back all-zero.

Table 3.4-5. Decimation Factor Register

Offset: 001Ch **Default: 0000 0001h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D09	R/W	DECIMATION FACTOR (**Ndec**)	001h	Sampling decimation factor. **Valid range: 1-1000.**
D10-D31	RO	(Reserved)	0000 00h	Inactive. Reads back all-zero.

Table 3.4-6. Sample Rate Control Examples

Clock Source:	Nvco	Nref	Ndiv-clk	Ndec	Fgen (MHz)	Fadc (MHz)	Fsamp
Rate Gen	**80**	**48**	**1**	**1**	50.000	50.000	**50.000 MHz**
	40	**24**	**25**	**1**	50.000	2.000	**2.000 MHz**
	40	**24**	**25**	**10**	50.000	2.000	**200.0 kHz**
	80	**48**	**25**	**1**	50.000	2.000	*** 2.000 MHz**
Ext Clk I/O @ 4 MHz	**---**	**---**	**---**	**400**	---	4.000	**10.00 kHz**

* Default configuration.

Table 3.4-7. Maximum Sustainable Sample Rates

NUMBER OF ACTIVE CHANNELS	DATA PACKING MODE	MAXIMUM SAMPLE RATE PER CHANNEL (MSPS)	MAXIMUM AGGREGATE SAMPLE RATE (MSPS)
1-2	Nonpacked	**25**	**50 MSPS**
3-4		**12.5**	**50 MSPS**
1-2	Packed	**50**	**100 MSPS**
3-4		**25**	**100 MSPS**

Table 3.4-8. Burst Size Register

Offset: 0024h **Default: 0000 0004h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D19	R/W	BURST SIZE	0 0004h	Total number of samples per active channel acquired after a sync event. **0 => continuous sampling after sync event.**
D20-D31	RO	(Reserved)	000h	Inactive. Reads back as all-zero.

Table 3.4-9. Packed Data Burst Acquisition

ACTIVE CHANNELS	SAMPLES PER LWORD	TOTAL LWORDS	TOTAL SAMPLES
1	2	SIZE	2* SIZE
2	1	SIZE	SIZE
3	2/3	3 * SIZE	2 * SIZE
4	1/2	2 * SIZE	SIZE

* “SIZE” = BURST SIZE or PRETRIGGER SIZE.

Table 3.4-10. Pretrigger Size Register

Offset: 0028h **Default: 0000 0004h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D17	R/W	PRETRIGGER SIZE	0 0004h	Total number of samples per active channel acquired before a sync event. **Valid range = 0_0002h through 3_FFFFh**.
D18-D31	RO	(Reserved)	0000 0h	Inactive. Reads back as all-zero.

Table 3.5-1. Input Data Buffer; Nonpacked Data

Offset: 0008h **Default: N/A**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D12	RO	DATA01 - DATA12	Intermediate data bits
D13	RO	DATA13	Most significant data bit
D14-D15	RO	0h or 3h *	All-zero or two's complement sign extension
		Channel Tag **	Channel number
D16-D31	RO	(Inactive)	Reads back all-zero

* Channel tag disabled. ** Channel tag enabled.

Table 3.5-2. Data Organization; Burst Marker Disabled

	Buffer Data Field			
	ENABLE DATA PACKING = Low		ENABLE DATA PACKING = High	
Buffer Lword Order	D[31..16]	D[15..0] *	D[31..16] *	D[15..0] *
---	---	---	---	---
Last -3	0000h	Chan 00 Data	Chan 01 Data	Chan 00 Data
Last -2	0000h	Chan 01 Data	Chan 03 Data	Chan 02 Data
Last -1	0000h	Chan 02 Data	Chan 01 Data	Chan 00 Data
Last	0000h	Chan 03 Data	Chan 03 Data	Chan 02 Data
---	---	---	---	---

* Includes channel tag or sign extension.

Table 3.5-3. Data Organization; Burst Marker Enabled

	Buffer Data Field			
	ENABLE DATA PACKING = Low		ENABLE DATA PACKING = High	
Buffer Lword Order	D[31..16]	D[15..0] *	D[31..16] *	D[15..0] *
---	---	---	---	---
Last -3	0000h	Chan 00 Data	Chan 01 Data	Chan 00 Data
Last -2	0000h	Chan 01 Data	Chan 03 Data	Chan 02 Data
Last -1	0000h	Chan 02 Data	Chan 01 Data	Chan 00 Data
Last	0000h	Chan 03 Data	Chan 03 Data	Chan 02 Data
EOB Marker	0000h	0000h	0000h	0000h
---	---	---	---	---

* Includes channel tag or sign extension.

Table 3.5-4. Input Data Coding; 14-Bit Data

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	3FFF	1FFF
Zero	2000	0000
Zero minus 1 LSB	1FFF	3FFF
Negative Full Scale	0000	2000

Table 3.5-5. Input Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D17	R/W	THRESHOLD VALUE	3 FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of Lword locations occupied in the input buffer ***exceeds*** the THRESHOLD VALUE.
D20	R/W	DISABLE BUFFER	0	Prevents input data from entering the buffer.
D21	R/W	DISABLE CHANNEL TAG	0	Designates data field D14-D15 as a sign extension when HIGH, or as a channel tag when LOW.
D22-D31	RO	(Reserved)	000h	Inactive. Reads back all-zero.

* Clears automatically within 5 microseconds of being set

Table 3.5-6. Buffer Size Register

Offset: 0010h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	0 0000h	Number of buffer Lword locations containing valid input data.
D19-D31	RO	(Inactive)	0000h	---

Table 3.5-7. Analog Input Function Selection

AIM[2:0]	FUNCTION OR MODE (Wideband and Hi-Level Configurations)
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Table 3.7-1. Primary Status Register

Offset 0x0004 **Default 0x0000 0000**

SELECTION BIT [1]	STATUS EVENT	RESPONSE BIT [2]	REFERENCE	DETECTION METHOD
D00	(Reserved)	D16	---	Level
D01	Autocal in progress	D17	3.6	
D02	Triggered Burst in progress	D18	3.4.4	
D03	Buffer Threshold Flag	D19	3,5,2	
D04	Burst Pretrigger-Armed Interval	D20	3.4.4.5	
D05	Buffer Underflow/Overflow	D21	3.5.2	
D06	(Reserved)	D22	---	
D07	(Reserved)	D23	---	
D08	Autocal completed	D24	3.6	Edge
D09	Input Burst triggered	D25	3.4.4	
D10	Input Burst completed	D26		
D11	Buffer Threshold flag LOW-to-HIGH transition	D27	3.5.2	
D12	Buffer Threshold flag HIGH-to-LOW	D28		
D13	Pretrigger Armed	D29	3.4.4.5	
D14	(Reserved)	D30	---	
D15	(Reserved)	D31	---	

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Remains HIGH until cleared LOW.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.9-1. Board Configuration Register

Offset: 0000 0030h **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16	High if the board contains only Channels 00 and 01.
D17-D18	Input Configuration: 0 => High-Level inputs 1 => Wideband inputs 2 => Transformer-Coupled inputs. 3 => (Reserved)
D19	Input Impedance: 0 => 2 Megohms 1 => 50 Ohms
D20-D31	(Reserved)

APPENDIX B

Comparison with PMC66-16AI64SSA

Appendix B

Comparison with PMC66-16AI64SSA

Operation of the PMC66-14HSAI4 is similar to that of the PMC66-16AI64SSA. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 summarizes principal PMC66-16AI64SSA and PMC66-14HSAI4 features.

Table B.1. PMC-16AI64SSA, PMC66-14HSAI4 Features Comparison

Feature	PMC66-16AI64SSA	PMC66-14HSAI4
Number of Channels	**64**	**4**
Data Width	**16 Bits**	**14 Bits**
Sample Rates	**Zero to 200KSPS/Channel**	**1MSPS to 50MSPS/Channel; 1KSPS to 50MSPS with decimation.**
Data Buffer	**256K-Sample FIFO (512KB)**	**512K-Sample FIFO (1MB)**
Buffer Data Field	32 Active bits	32 Active bits
ADC Type	**Direct Sampling (SAR)**	**Pipelined conversion; 6-stage**
PCI Adapter	**PCI-9056 (32-Bit PCI)**	**PCI-9056 (32-Bit PCI)**
PCI Interface	PCI 2.3; D32; 33MHz/66MHz	PCI 2.3; D32; 33MHz/66MHz
Adjustable Clock	**None (Divided fixed clk-freq)**	**Two-Integer Ratiometric Control**
Pretriggered Bursts	**No**	**Yes**
Sync On Level	**No**	**Yes**
Interrupt	2x8 Local Config; INTA#	16-Bit; Primary status register; INTA#
DMA	Buffer only	Buffer only
Autocalibration	**All production configurations**	**High-Level and Wideband configurations only.**
Local Clock	50 MHz	50 MHz

B.2. General Migration Issues; PMC66-16AI64SSA to PMC66-14HSAI4:

Table 3.1-1. Control and Data Registers:

- The "Scan and Sync" register has been renamed "Clocking and Sync."
- The following registers no longer apply, and have been deleted:
  - Auxiliary R/W Register,
  - Auxiliary Sync I/O Control.
- A new "Utilities" register has been added, and will be activated and documented at a later date.

Table 3.1-1. Control and Data Registers:
Paragraph 3.4.3. ADC Clocking:

- Registers "Rate Generator Adjust" and "Rate Divisors" replace the original "Rate A/B Generator" registers.
- The frequency of the rate generator is now controlled by the ratio of two integers (Nvco, Nref) instead of by a single integer (Nrate)
- A new register "Decimation Factor" provides decimated sampling below 1-Mhz.

Table 3.1-1. Control and Data Registers:
Paragraph 3.4.4.3 Burst Size:

- A new register "Burst Size" defines the size of triggered bursts.

Table 3.1-1. Control and Data Registers:
Paragraph 3.4.4.4 Burst Marker:

- The burst marker has been moved to the end of the burst, as End-of-Burst (EOB).
- The following registers no longer apply, and have been deleted:
  - Scan Marker Upper Word,
  - Scan Marker Lower Word

The scan marker is always all-zero when selected in the PMC66-14HSAI4.

Table 3.1-1. Control and Data Registers:
Paragraph 3.4.4.5 Pretriggering:

- A new register "Pretrigger Size" allows acquisition of pretrigger data.

Table 3.2-1. Board Control Register:

- The following control bits no longer apply, and have been deleted:
  - UNIPOLAR INPUTS,
  - DIFFERENTIAL PROCESSING,
- The ENABLE EXTERNAL SYNC control bit has been relocated to the Clocking and Sync control register as a 'SYNC TARGET' code.
- Three new control bits have been added to the BCR; "ENABLE ADC CLOCKING," "ENABLE BURST" and "ENABLE BURST MARKER."

Table 3.4-2. Clocking and Sync Control Register:

- Replaces the "Scan and Sync Control" register. Designates active channels and selects target or initiator operating modes independently for clocking and sync. Also controls pretriggering.

Table 3.4-2. Clocking and Sync Control Register:

Paragraph 3.4.4.2 Sync On Level:

- A new field "Sync Level" allows synchronization to the Channel-00 input level.
- New fields "Integration" and "Holdoff" add oscilloscope triggering functions.

Table 3.4-3. Rate Generator Adjust Register:

- Replaces the Rate-A Generator register. Contains PLL control integers Nvco and Nref.

Table 3.4-4. Rate Divisors Register:

- Replaces the Rate-B Generator register. Contains the clock and sync rate divisors.

Table 3.5-1. Input Data Buffer; Tables 3.5-2, 3.5-3. Data Organization:

- Data fields are now 14 bits wide instead of 16 bits.

Table 3.5-5. Input Buffer Control Register:

- Two new control bits: DISABLE BUFFER and DISABLE CHANNEL TAG.

Table 3.7. Primary Status Register:

Paragraph 3.7. Primary Status Register:

- The original interrupt control register has been replaced with a status-flag register that provides both level-detected and edge-detected information.

Paragraph 3.8 DMA Operation

- Demand-mode operation has been revised to eliminate the "Disable Demand Mode" control bit in the BCR, and no longer requires a threshold input from the buffer control register.

Table 3.9-1. Board Configuration Register

- Production options have changed.

Revision History:

02-01-2008: Initial release as preliminary.

03-17-2008: Table 3.4-6.

02-25-2009: Paragraph 3.3.2. Updated initialization duration and effects.
Paragraph 3.4.3.2. Modified note regarding the 'Rate Gen Not Ready' flag.

12-22-2010: Table 3.4-2: Revised minimum integration interval.
Paragraph 3.4.4.1. Revised Ndiv-sync range.
Removed 'Preliminary' status.

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