General Standards Corporation

High Performance Bus Interface Solutions

Rev: 090406

PCI-16SDI

16-BIT, 16-CHANNEL SIGMA-DELTA, 220 KSPS ANALOG INPUT PCI BOARD

With Optional 68-Pin or 50-Pin System I/O Connector

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PCI-16SDI board is a single-width board that provides 16-bit analog input capability for the PCI bus at sample rates up to 220 KSPS per channel. In addition to providing sixteen analog input channels and four independently adjustable rate generators, the board supports multiboard clocking and synchronization. The board is functionally and mechanically compatible with the IEEE PCI local bus specification Revision 2.1, and supports the "plug-n-play" initialization concept. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with minimal (200 LFPM) air cooling. Specific details pertaining to physical characteristics and performance are contained in the PCI-16SDI product specification.

The board is designed for minimum off-line maintenance, and includes internal monitoring features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made at the panel bracket through a single 68-pin or 50-pin connector. Figure 1.1 shows the physical configuration of the board, and the general arrangement of major components.

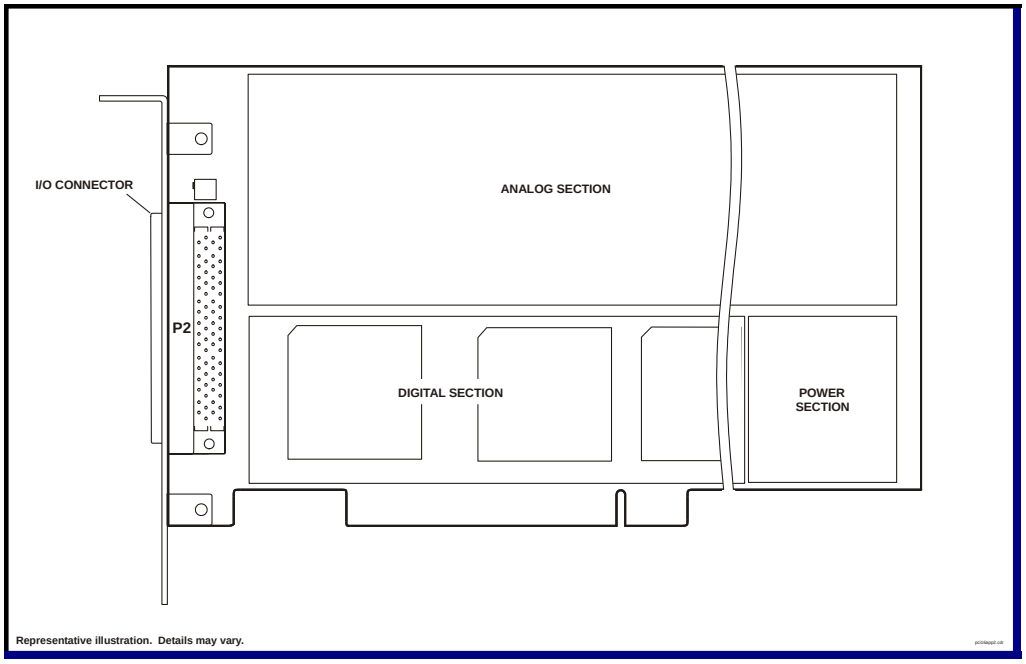

Figure 1.1. Physical Configuration

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1.2). Each of the sixteen analog input channels contains a lowpass antialiasing filter and a dedicated sigma-delta A/D converter (ADC). The inputs can be configured for either differential or single-ended operation, or an internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming of the input channels is performed by calibration DAC's that are loaded with channel correction values during autocalibration. The use of calibration DAC's prevents the missing codes that occur when analog input channels are calibrated exclusively in the digital domain.

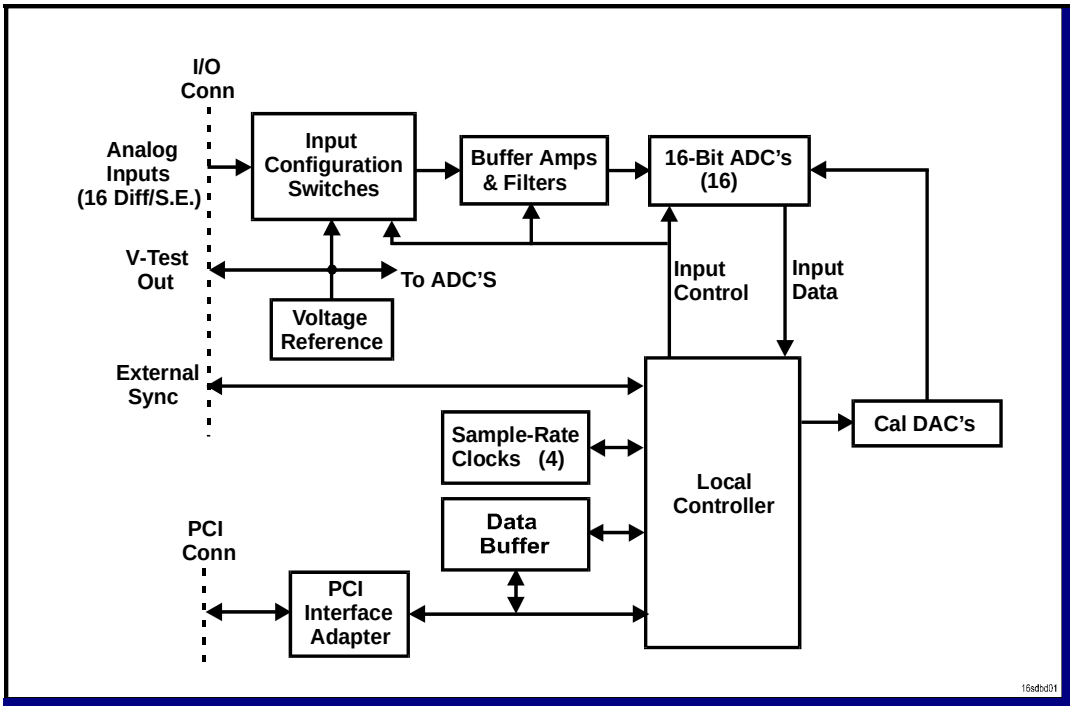

Figure 1.2. Functional Organization

Four independent sample-rate clock generators are individually adjustable from 8 MHz to 16 MHz, and are divided down within the local controller to provide individual channel sample rates from 5 KSPS to 220 KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that has a software-controlled threshold for generating interrupt requests.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be daisy-chained together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host system are properly discharged to ground.

Before removing the board from the protective shipping envelope, select an empty PCI slot in the host computer and, if a blank panel bracket is located in the slot position, remove the bracket. Then remove the board from the shipping envelope and position the board with the panel bracket oriented toward the expansion panel opening. Align the board's PCI edge-connector with the mating connector on the motherboard, and carefully press the board into position. Verify that the PCI connector has mated completely, and that the panel bracket is seated against the fastener bracket above the panel opening. To complete the installation, secure the panel bracket with an appropriate machine or panhead screw; do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

I/O connector P2 is designed to mate with a 68-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-068-S-TG. The insulation displacement (IDC) Robinson Nugent cable connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2.2 and in Figure 2.2.2.

A 50-Pin D-subminiature system I/O connector also is available, with the pin configuration and assignments shown in Figure 2.2.2 and Table 2.2.2. A suitable mating IDC connector is AMP #746790-1, with strain-relief AMP # 746785-1, which accepts a single 50-wire 0.050-inch ribbon cable.

Table 2.2.2. System Connector Pin Assignments

68-PIN I/O CONNECTOR

ROW-A (Cable-A)			ROW-B (Cable-B)	
PIN	SIGNAL		PIN	SIGNAL
1	DIGITAL RETURN		1	DIGITAL RETURN
2	DIGITAL RETURN		2	DIGITAL RETURN
3	CLOCK INPUT LO		3	CLOCK OUTPUT LO
4	CLOCK INPUT HI		4	CLOCK OUTPUT HI
5	DIGITAL RETURN		5	DIGITAL RETURN
6	DIGITAL RETURN		6	DIGITAL RETURN
7	SYNC INPUT LO		7	SYNC OUTPUT LO
8	SYNC INPUT HI		8	SYNC OUTPUT HI
9	DIGITAL RETURN		9	DIGITAL RETURN
10	DIGITAL RETURN		10	DIGITAL RETURN
11	INPUT RETURN		11	INPUT RETURN
12	INPUT RETURN		12	INPUT RETURN
13	INPUT RETURN		13	INPUT RETURN
14	INPUT RETURN		14	INPUT RETURN
15	VTEST RETURN		15	INPUT RETURN
16	VTEST OUTPUT		16	INPUT RETURN
17	INPUT CH 07 LO		17	INPUT CH 15 LO
18	INPUT CH 07 HI		18	INPUT CH 15 HI
19	INPUT CH 06 LO		19	INPUT CH 14 LO
20	INPUT CH 06 HI		20	INPUT CH 14 HI
21	INPUT CH 05 LO		21	INPUT CH 13 LO
22	INPUT CH 05 HI		22	INPUT CH 13 HI
23	INPUT CH 04 LO		23	INPUT CH 12 LO
24	INPUT CH 04 HI		24	INPUT CH 12 HI
25	INPUT CH 03 LO		25	INPUT CH 11 LO
26	INPUT CH 03 HI		26	INPUT CH 11 HI
27	INPUT CH 02 LO		27	INPUT CH 10 LO
28	INPUT CH 02 HI		28	INPUT CH 10 HI
29	INPUT CH 01 LO		29	INPUT CH 09 LO
30	INPUT CH 01 HI		30	INPUT CH 09 HI
31	INPUT CH 00 LO		31	INPUT CH 08 LO
32	INPUT CH 00 HI		32	INPUT CH 08 HI
33	INPUT RETURN		33	INPUT RETURN
34	INPUT RETURN		34	INPUT RETURN

50-PIN D-SUB I/O CONNECTOR

PIN	SIGNAL		PIN	SIGNAL
1	CLOCK INPUT LO		42	INPUT CH 11 HI
34	CLOCK INPUT HI		26	INPUT CH 10 LO
18	SYNC INPUT LO		10	INPUT CH 10 HI
2	SYNC INPUT HI		43	INPUT CH 09 LO
35	DIGITAL RETURN		27	INPUT CH 09 HI
19	DIGITAL RETURN		11	INPUT CH 08 LO
3	CLOCK OUTPUT LO		44	INPUT CH 08 HI
36	CLOCK OUTPUT HI		28	INPUT CH 07 LO
20	SYNC OUTPUT LO		12	INPUT CH 07 HI
4	SYNC OUTPUT HI		45	INPUT CH 06 LO
37	INPUT RETURN		29	INPUT CH 06 HI
21	INPUT RETURN		13	INPUT CH 05 LO
5	VTEST RETURN		46	INPUT CH 05 HI
38	VTEST OUTPUT		30	INPUT CH 04 LO
22	INPUT RETURN		14	INPUT CH 04 HI
6	INPUT RETURN		47	INPUT CH 03 LO
39	INPUT CH 15 LO		31	INPUT CH 03 HI
23	INPUT CH 15 HI		15	INPUT CH 02 LO
7	INPUT CH 14 LO		48	INPUT CH 02 HI
40	INPUT CH 14 HI		32	INPUT CH 01 LO
24	INPUT CH 13 LO		16	INPUT CH 01 HI
8	INPUT CH 13 HI		49	INPUT CH 00 LO
41	INPUT CH 12 LO		33	INPUT CH 00 HI
25	INPUT CH 12 HI		17	INPUT RETURN
9	INPUT CH 11 LO		50	INPUT RETURN

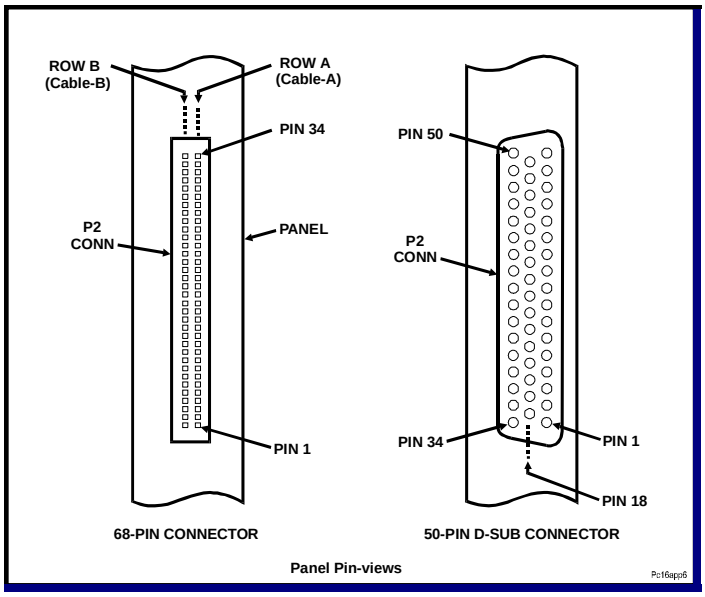

Figure 2.2.2. System Input/Output Connector

2.3 Analog Input Configuration

Analog inputs can be configured either as 16 single-ended channels or as 16 differential channels. Differential operation usually provides the highest noise immunity, and is recommended for most applications. The hardware input configuration must be acknowledged by the control software, which configures the internal controller for either single-ended or differential operation. Pull-down resistors are provided on all analog inputs.

2.3.1 Single-Ended Inputs

The single-ended operating mode generally provides optimum performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

For applications in which the signal sources are isolated from each other (mutual isolation), single-ended operation may be recommended. In this case, as shown in Figure 2.3.1a, the input return is connected to the internal ADC return. Isolation from system grounds is a critical issue in single-ended operation. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and the input return can generate excessive return current and cause erroneous measurements or possibly damage the board.

2.3.2 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1b, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return is connected to system ground as closely as possible to the input sources.

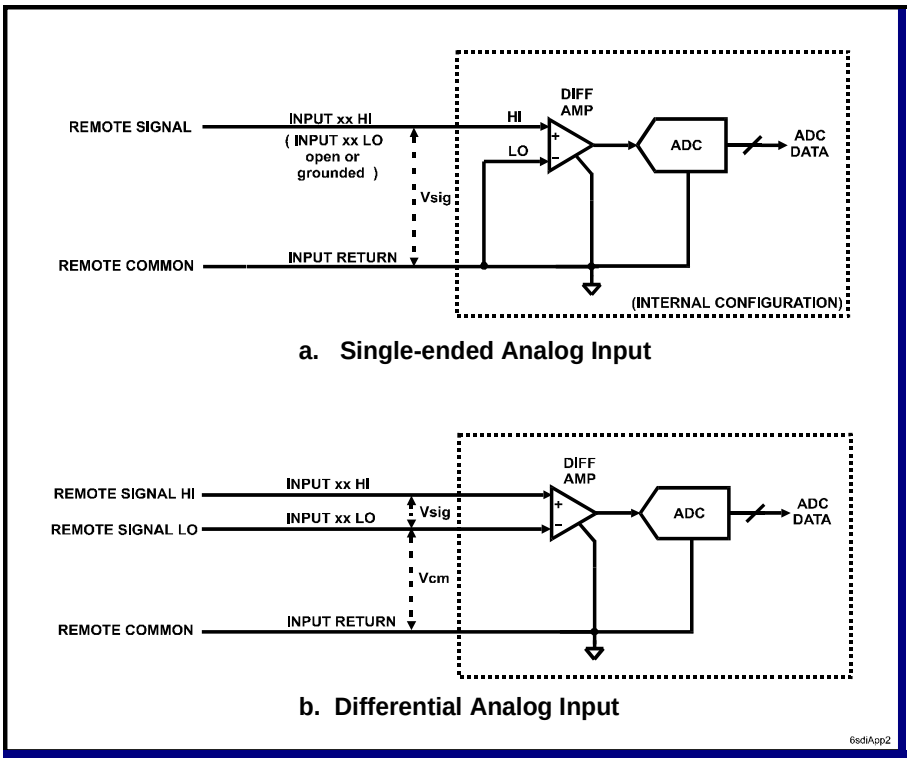

Figure 2.3.1. Input Configurations

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.4.1 Interboard Connections

Figure 2.4.1 illustrates how multiple PCI-16SDI boards can be daisy-chained together in an initiator-target sequence to provide synchronization and common clocking between boards. (The initiator clock output signal is the output of Rate Generator "A" on the initiator board.) Pins 1-10 in ribbon Cable-A at the I/O connector contain the differential clock and sync input lines, while ribbon Cable-B contains the corresponding outputs. To connect multiple boards together, the ten-wire section corresponding to Pins 1-10 in Cable-B can be separated from the remainder of the cable, and connected to the Cable-A section (Pins 1-10) of the next I/O connector in the chain.

A similar arrangement is available for the optional 50-Pin D-subminiature system connector.

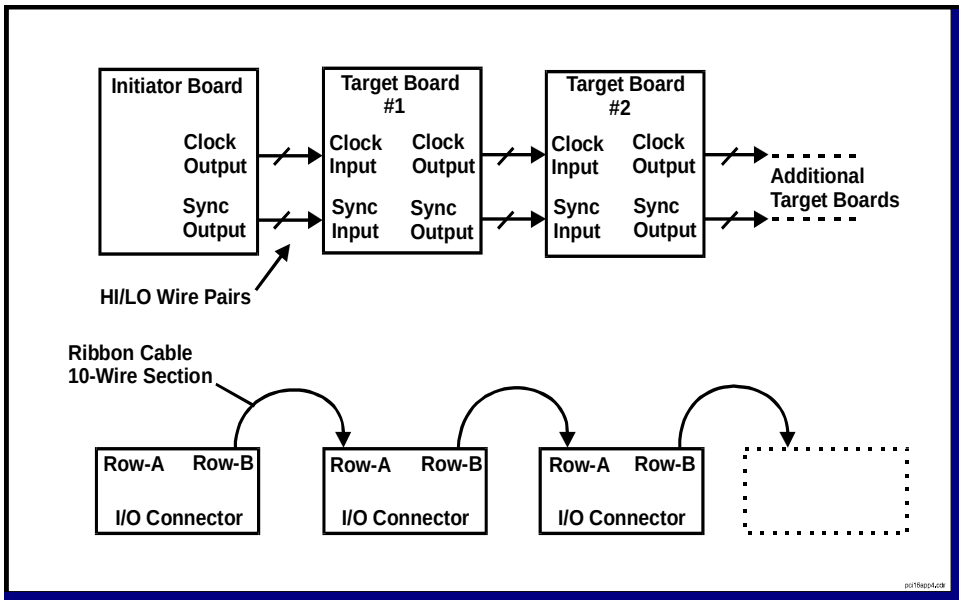

Figure 2.4.1. Multiboard Clock/Sync Connections

Note: External clock and sync inputs can be provided from external sources other than an initiator board. Alternate clock and sync sources must be LVDS-compatible.

Because each board provides active differential outputs for the next board in the chain, the number of boards in the chain is limited only by the maximum time-skew of approximately 1 nanosecond introduced by each board. The length of cable between boards should be minimized, preferably to no more than 5 feet.

Software controls the designation of each board as an initiator or a target, and also selects the specific channels on each board that will respond to the daisy-chained clock. Although only software-designated channels respond to the daisy-chained clock, all channels on all target boards respond to the sync signal.

2.4.2 Multiboard Synchronization

Boards that are daisy-chained together for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The sequence has a duration of approximately 128 conversion cycles, after which all synchronized channels that have the same conversion rate will sample their inputs simultaneously. Synchronized channels also can be harmonically locked by adjusting their sample rates to integral submultiples of the initiator clock output frequency.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference adjustment. The optimum adjustment interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This procedure describes the adjustment of the internal reference. For applications in which the system must not be powered down, the adjustment can be performed while the board is installed in an operating system.

To eliminate the requirement for a special test connector, the two connections required for the reference adjustment, VTEST OUTPUT and VTEST RETURN, can be made available at a system breakout connector or test panel. This arrangement also eliminates the necessity of disconnecting the system input/output cable for the adjustment.

2.6.1 Equipment Required

Table 2.6.1 lists the equipment requirements for calibrating the PCI-16SDI board. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Adjustment Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with PCI expansion slot	---	---
Cable connector, with test leads. (Not required if calibration test points are made permanently available at a system connection point)	Robinson Nugent	P50E-068-S-TG

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimpot that is accessible from the front panel, adjacent to the P2 system I/O connector, as shown in Figure 2.6.2. The adjustment seal on the trimmer should be removed before beginning the procedure, and the trimmer should then be resealed with a suitable sealing agent after adjustment has been completed.

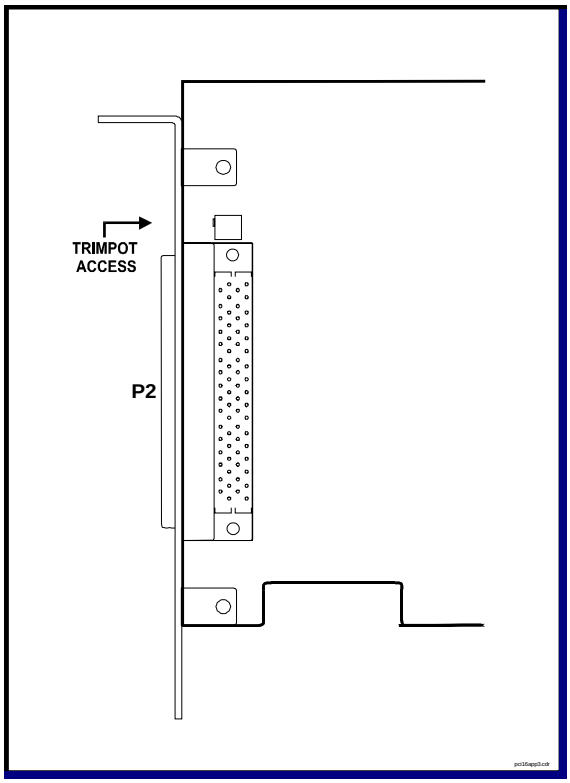

Figure 2.6.2. Reference Adjustment Access

This procedure assumes that the board is installed in an operating system. The board can be in any operating mode when the adjustment is performed. Refer to Table 2.2.2 for pin assignments.

1. Connect the digital multimeter between the VTEST OUTPUT (+) and VTEST RETURN (-) pins in the system I/O connector. Refer to Table 2.2.2 for pin assignments.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding.

3. Adjust the reference adjustment trimmer until the digital multimeter indication is within the range +9.9000 ±0.0005 VDC.

4. Reference adjustment is complete. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PCI-16SDI board is compatible with the PCI Local Bus specification and supports "plug-n-play" autoconfiguration at the time of power-up. That is, the host can obtain the amount of I/O space required by the board, and return the configuration base address into the PCI Configuration Register at Offset 18h on this board. The PCI interface is controlled by a PLX™ PCI-9080 I/O accelerator device. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization has been completed, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. Reserved bits in each register are ignored during write operations, and are forced LOW during read operations. Writing reserved bits as LOW is recommended.

Table 3.1. Control and Data Registers

LOCAL ADDR	ACCESS MODE *	REGISTER	DEFAULT	DESCRIPTION
00	R/W	BOARD CONTROL	0000 383Ch	Board Control Register (BCR)
04	R/W	RATE CONTROL A	0000 0000h	Rate control for Rate Generator-A
08	R/W	RATE CONTROL B	0000 0000h	Rate control for Rate Generator-B
0C	R/W	RATE CONTROL C	0000 0000h	Rate control for Rate Generator-C
10	R/W	RATE CONTROL D	0000 0000h	Rate control for Rate Generator-D
14	R/W	RATE ASSIGNMENTS	0000 3210h	Channel-group rate generator assignments
18	R/W	RATE DIVISOR 00,01	0000 0505h	Channels 00 and 01 sample rate divisors
1C	R/W	RATE DIVISOR 02,03	0000 0505h	Channels 02 and 03 sample rate divisors
20	R/W	RATE DIVISOR 04,05	0000 0505h	Channels 04 and 05 sample rate divisors
24	R/W	RATE DIVISOR 06,07	0000 0505h	Channels 06 and 07 sample rate divisors
28	R/W	RATE DIVISOR 08,09	0000 0505h	Channels 08 and 09 sample rate divisors
2C	R/W	RATE DIVISOR 10,11	0000 0505h	Channels 10 and 11 sample rate divisors
30	R/W	RATE DIVISOR 12,13	0000 0505h	Channels 12 and 13 sample rate divisors
34	R/W	RATE DIVISOR 14,15	0000 0505h	Channels 14 and 15 sample rate divisors
38	R/W	BUFFER THRESHOLD	0003 FFFEh	Input buffer control and status threshold
3C	RO	Firmware Revision **	---	---
40	RO	BUFFER SIZE	---	Number of ADC values in the input buffer.
44	RO	Autocal Values **	---	---
48	RO (DMA)	INPUT DATA BUFFER	---	Input Data Buffer; Data and channel tag
4C	R/W	Auxiliary register **	---	Reserved 20-Bit auxiliary register.
50-7C	--	(Reserved)	---	---

* R/W = Read/Write; RO = Read-Only. ** Maintenance register. Shown for reference only.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and input range selections, and consists of 32 control bits and status flags (Table 3.2). Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects input configuration or selftest mode. Defaults to differential input mode.
D01	R/W	AIM1	
D02	R/W	RANGE0	Analog input range selection. Defaults to ±10V range.
D03	R/W	RANGE1	
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults to offset binary.
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults HIGH to Initiator mode.
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.
D07	R/W	*AUTOCAL	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.
D09	R/W	INTERRUPT A1	
D10	R/W	INTERRUPT A2	
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D12	RO	AUTOCAL PASS	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.
D13	RO	CHANNELS READY	LOW during change in channel parameters. Asserted HIGH when inputs are ready to acquire data.
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.
D15	R/W	*INITIALIZE	Initializes the board when asserted. Sets all defaults.
D16	R/W	SYNCHRONIZE SCAN	Selects synchronous sampling mode.
D17	R/W	CLEAR BUFFER ON SYNC	When this bit is HIGH, the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.
D18-31	RO	(Reserved)	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Register value changes to 0000 783Ch approximately 400 milliseconds after initialization.

3.3 Configuration and Initialization

3.3.1 Board Configuration

Board configuration is initiated by a PCI bus RESET, and should be required only once after the initial application of power. During board configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
Rate generator clocks are initialized	250 ms

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 253 milliseconds, and produces the following conditions:

- Calibration D/A converters are initialized with midrange values
- All rate generators are adjusted to 125 KSPS
- Rate generator-A controls all channels; all divisor ratios are set to equal 5.
  I.e.: All sample rates are 25 kHz (125kHz÷5).
- The analog input buffer is reset to empty; Buffer threshold equals 0003 FFFEh
- Analog inputs are configured for ±10Volt differential operation
- The BCR is initialized; all defaults are invoked
- The local interrupt request is asserted as an initialization-completed event.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[1..0], the effects of which are summarized in Table 3.4. The analog input selection arranges all input channels in either single-ended or differential configuration during normal operation, or invokes one of two selftest modes.

Table 3.4. Analog Input Function Selection

AIM[1:0]	FUNCTION OR MODE
0	Differential analog input mode.
1	Single-Ended analog input mode.
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

3.4.1 Differential/Single-Ended Input Modes

Selection of the differential or single-ended mode input shown in Table 3.4 establishes compatibility with system wiring, as described in Section 2. The input mode determines only the system input connections, and has no effect upon the sample rate, input range, or any other aspect of input acquisition.

3.4.2 Selftest Modes

Two selftest modes provide the ability to verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). The +VREF test produces a positive value equal to 99.00 percent of the selected input range (e.g. +9.900 Volts for the ±10 Volt range) from all input channels, and the ZERO test should produce a value of 0.000 Volts. The accuracy of selftest measurements should correspond to the product accuracy specification.

3.4.3 Input Range Selection

Any one of four input voltage ranges can be selected for all channels. RANGE[1..0] control bits in the BCR select the input range, as shown in Table 3.4.3.

Table 3.4.3. Analog Input Range Selection

RANGE[1..0]	ANALOG INPUT RANGE
0	±1.25 Volts
1	±2.5 Volts
2	±5 Volts
3	±10 Volts

3.4.4 Settling Delays and the Channels Ready Flag

When a critical parameter of an input channel, such as input mode, input range or sample rate is changed, the channel undergoes a settling transition during which the measured values are unpredictable. The settling delay required before input data is reliable varies with the individual channel sample rates, but will not exceed 130 conversion intervals. A delay of 26 milliseconds will accommodate all valid sample rates down to 5 KSPS. The CHANNELS READY status flag in the BCR eliminates the need for control software to insert settling delays.

The CHANNELS READY status flag in the BCR goes LOW when any critical channel parameter is changed, or when a sync or autocal sequence commences, and returns HIGH only when all input channels are ready to acquire data. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1).

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input values pass through a 256-Word transfer FIFO into the analog input data FIFO data buffer, which has a capacity of 256K (262,144) data values. Input data accumulates in the data buffer until extracted by the PCI bus from a single register location, indicated as INPUT DATA BUFFER in Table 3.1. Note: Reading an empty buffer returns an indeterminate value.

3.5.2 Data Organization

Each value in the data buffer contains 20 active bits, consisting of 16 data bits and four tag bits as shown in Table 3.5.2.

Table 3.5.2. Input Buffer Data Organization

Offset: 0000 0048h **Default: N/A**

CHANNEL TAG			CHANNEL DATA VALUE		
D19 (MSB)	D17-D18	D16 (LSB)	D15 (MSB)	D01-D14	D00 (LSB)

3.5.2.1 Channel Tags

Because all channels have individually adjustable sample rates, the order in which channel data accumulates in the buffer is not generally predictable. Therefore, a 4-bit channel tag that identifies each input channel is attached to each associated data value in the buffer, and occupies data bits D16 through D19 (Table 3.5.2).

3.5.2.2 Input Data Format

Input data values occupy buffer data bits D00 through D15. Values can be represented either in 16-bit offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +5.000 Volts for the ±5V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. One LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V option).

3.5.3 Buffer Threshold Register

The buffer threshold register (Table 3.5.3) contains the threshold value for the buffer status flag, and also provides control bits for clearing the buffer and for disabling the buffer inputs.

Table 3.5.3. Buffer Threshold Register

Offset: 0000 0038h **Default: 0003 FFFEh**

REGISTER BITS	ACCESS MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold
D[18]	R/W	DISABLE BUFFER INPUT	Disables ADC inputs to the buffer
D[19]	R/W	CLEAR BUFFER	Clears (empties) the buffer
D[31..20]	RO	(Reserved)	

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer and the 256-Word transfer FIFO can be monitored either by polling the BUFFER THRESHOLD FLAG status bit in the BCR, or by selecting the flag as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Section 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer exceeds the BUFFER THRESHOLD value D[17..0] in the Buffer Threshold register shown in Table 3.5.3. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h, and the threshold flag undergoes a HIGH-to-LOW transition. Likewise, a LOW-to-HIGH transition of the flag with a threshold value of 0003 FFFEh, indicates a buffer-full event. The default value for the buffer threshold is 0003 FFFEh.

3.5.3.2 Buffer Clearing and Disabling

Asserting the CLEAR BUFFER control bit in the threshold register empties the buffer. This bit does not clear automatically, and must be written LOW to clear.

Asserting the DISABLE BUFFER INPUT control bit disables inputs to the buffer from the ADC input channels, and halts the accumulation of further input data. Input data already present in the buffer when this bit is asserted remains in the buffer.

3.6 Input Sampling Control

The local controller provides control of the following aspects of input sampling:

a. Sample Rate
b. Phase, or skew
c. Channel synchronization.

Sample rates are determined primarily by the bandwidth requirements for individual channels, while phase and synchronization control the timing and coherence of sampling between multiple channels. The sample rate usually is a significant consideration. Phase and synchronization are important in applications that require consistent relative timing of sampling among multiple channels.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

Note: Unless indicated otherwise, the term "simultaneous" is used here to refer to both simultaneous and harmonically locked operation.

3.6.1 Sample Rate Control

The sample rate for each channel is controlled by the following board parameters:

a. Assignment of the channel to a specific rate generator
b. Rate generator frequency
c. Channel rate divisor.

These parameters are described individually in the following paragraphs, and are summarized in Paragraph 3.6.1.5 "Sampling Frequency Summary."

3.6.1.1 Rate Clock Organization

Sample rates are derived from one or more of the four independently adjustable internal rate generators, as shown in Figure 3.6.1.1, or from a single external clock input that is divided by two internally. Input channels are arranged into four groups of four channels (Table 3.6.1.1), each of which can be assigned to any one the four rate generators, or to the external clock.

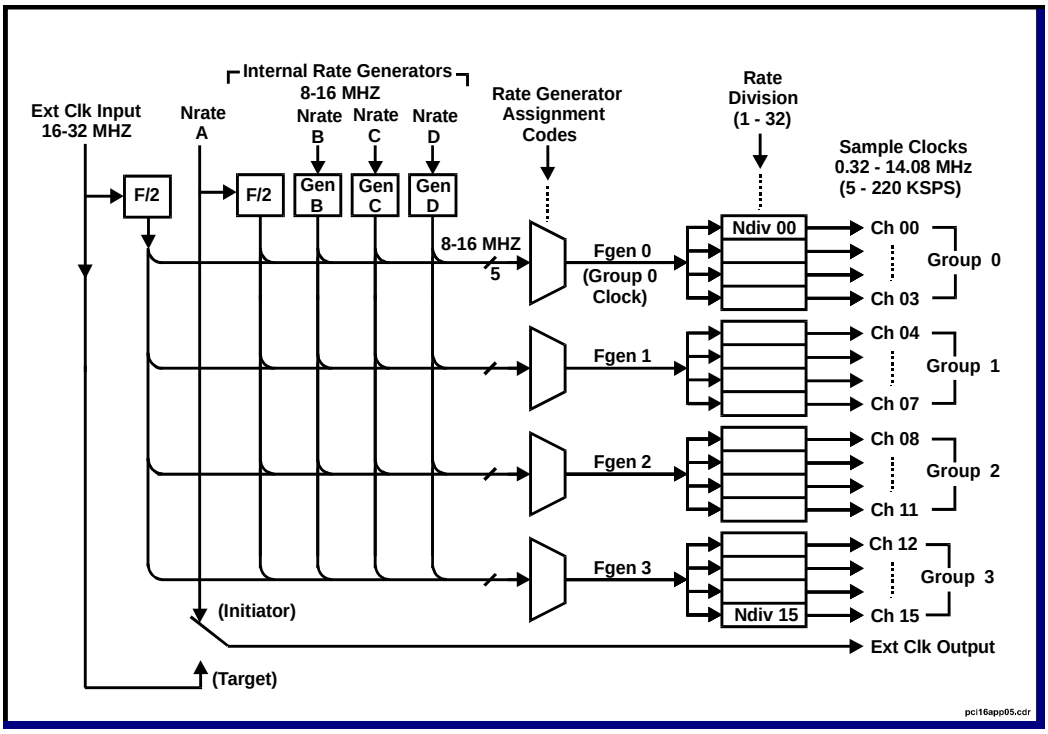

Figure 3.6.1.1. Rate Clocks Organization, 16-Channel Board

The number of channels per group is reduced to two channels for 8-channel boards, or to one channel for 4-Channel boards. This scheme ensures access to all four rate generators, regardless of the number of channels present on a board.

Table 3.6.1.1. Channel Groups

	INPUT CHANNELS		
CHANNEL GROUP	**16-CHANNEL BOARD**	**8-CHANNEL BOARD**	**4-CHANNEL BOARD**
0	00,01,02,03	00,01	00
1	04,05,06,07	02,03	01
2	08,09,10,11	04,05	02
3	12,13,14,15	06,07	03
(Reserved)	---	---	---

3.6.1.2 Rate Generator Assignment

A 4-bit code ASSIGN 0-3 in the RATE ASSIGNMENTS register assigns each channel group to a specific rate generator, or to an external sample rate clock. The group selection codes are arranged in the register as shown in Table 3.6.1.2-1, and use the assignment codes listed in Table 3.6.1.2-2. The output of the generator assigned to a specific group provides the input frequency for all channel divisors in the group. Channels in a group with a rate generator assignment of "none" are disabled and do not provide data to the input data buffer.

Table 3.6.1.2-1. Rate Assignments Register
Offset: 0000 0014h Default: 0000 3210h

REGISTER BITS	ACCESS MODE	DESIGNATION	CHANNEL GROUP
D[03:00]	R/W	ASSIGN 0	0
D[07:04]	R/W	ASSIGN 1	1
D[11:08]	R/W	ASSIGN 2	2
D[15:12]	R/W	ASSIGN 3	3
D[31:16]	RO	(Reserved, read-only)	(Reserved)

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	ASSIGNMENT
0	Generator-A
1	Generator-B
2	Generator-C
3	Generator-D
4	External Sample Clock
5-15	None (Disabled)

3.6.1.3 Channel Rate Divisors

Each input channel has a dedicated 6-bit rate divisor that divides the assigned rate generator frequency to 64 times the sampling frequency for the channel (64 is the oversampling factor for the A/D converters). The divisors reside in the RATE DIVISOR registers shown in Table 3.1, with each register containing the divisors for two channels. Each RATE DIVISOR register is configured as shown in Table 3.6.1.3.

Note: The valid range of divisor values is from 1 to 32. A value of zero, or a value greater than 32 will produce unpredictable results.

Table 3.6.1.3. Rate Divisor Registers
Offset: (As Shown in table) Default: 0000 0505h

REGISTER BITS	REG 00,01	REG 02,03	REG 04,05	REG 06,07	REG 08,09	REG 10,11	REG 12,13	REG 14,15
D[05..00]	CHAN 00	02	04	06	08	10	12	14
D[07..06]	*	*	*	*	*	*	*	*
D[13..08]	CHAN 01	03	05	07	09	11	13	15
D[31..14]	*	*	*	*	*	*	*	*
Offset:	0018h	001Ch	0020h	0024h	0028h	002Ch	0030h	0034h

* Reserved read-only bit(s).

The required rate generator frequency **Fgen** is determined by the sampling frequency **Fsamp** and the rate divisor value **Ndiv** as:

Fgen = 64 * Fsamp * Ndiv,

where **Fsamp** and **Fgen** are in kilohertz.

For example, a sample rate of 44 kHz and a divisor value of 4 would require a rate generator frequency of 11,264 kHz (11.264 MHz).

3.6.1.4 Rate Generator Control

The four internal rate generators are designated Generator-A,B,C and D, and are controlled by the four RATE CONTROL registers listed in Table 3.1. (Bits [31..09] in the RATE CONTROL registers are read-only reserved bits). The frequency **Fgen** of each generator is controlled by a 9-bit value **Nrate** in the associated RATE CONTROL register, according to the relationship:

Nrate = (0.063875 * Fgen) - 511,

where **Fgen** is in kilohertz, and **Nrate** is rounded to the nearest integer value.

For example, a rate generator frequency of 11.264 MHz would require an **Nrate** value of 208.488, or 208 when rounded to the nearest integer value. The integer value of 208 in turn, would provide an actual generator frequency of 11.256 MHz, which is within 0.08% of the required value.

3.6.1.5 Sampling Frequency Summary

Adjustment of the sampling rate involves the parameters listed in Table 3.6.1.5-1, which also shows the valid range for each parameter.

Table 3.6.1.5-1. Rate Parameter Constraints

RATE PARAMETER	SYMBOL	VALID RANGE
Sample Rate	Fsamp	5 kHz to 220 kHz
Rate Generator Frequency *	Fgen	8 MHz to 16 MHz
Rate Control Value	Nrate	Integer; Zero to 511
Rate Divisor	Ndiv	Integer; 1 to 32

* Included for reference. Not required in calculations.

The rate control value **Nrate** is common to all channels within a group, and must be determined for the highest sample rate required in the group. To determine **Nrate** for a channel group:

a. Assign the associated channel group to a specific rate generator, using the RATE ASSIGNMENTS register.

b. Using the following relationship for the highest-frequency channel in the group, select the lowest rate divisor **Ndiv** that produces **Nrate** between zero and 511 (In an iterative loop, the initial value for **Ndiv** can be 1).

$$\mathbf{Nrate = (4.088 * Fsamp * Ndiv) - 511,}$$

where **Fsamp** is in kilohertz, and **Nrate** is rounded to the nearest integer value.

c. Once **Fsamp** and **Ndiv** have been determined for any channel in a group, the rate divisors for the remaining channels is calculated from:

$$\mathbf{NdivY = NdivX * FsampX / FsampY ,}$$

where **NdivX** and **NdivY** are the divisors for any two channels **X** and **Y** in the group, and **FsampX** and **FsampY** are their respective sample rates.

Table 3.6.1.5-2 lists a number of examples for determining **Nrate**. Notice that, when **Nrate** is held within the required range from zero to 511, **Fgen** is automatically constrained to the required range of 8 MHz to 16 MHz and consequently is not a required calculation.

Table 3.6.1.5-2. Rate Generator Control Examples

Sample Rate (Fsamp), kHz	Divisor Register Value (Ndiv)	Rate Control Value (Nrate)	* Rate Generator Frequency (Fgen), MHz
5	32	**143**	10.24
11 **	16	**208**	11.26
22 **	8	**208**	11.26
44 **	4	**208**	11.26
22	6	**29**	8.45
22	10	**388**	14.08
22	11	**478**	15.49
100	2	**307**	12.80
220	1	**388**	14.08

* Not a required calculation.
** Harmonically locked if all channels are assigned to the same rate generator.

3.6.1.6 Harmonically Locked Channels

Multiple channels operating at different frequencies that are submultiples of a common frequency (i.e. the group rate generator frequency), will perform conversions repetitively relative to a sampling frame, and are *harmonically locked*. Therefore, all channels within a single channel group are harmonically locked, by definition. Table 3.6.1.5-2 lists an example of three harmonically locked channels.

3.6.2 Channel Synchronization

Each conversion has a duration of 64 clock cycles, so simply operating all converters from a common clock does not ensure simultaneous sampling. All conversions may not commence in the same clock cycle. To guaranty simultaneous sampling, the converters must first be synchronized to initiate conversions simultaneously at a common point in time. Thereafter, the converters will continue to sample simultaneously if they are operating from a common clock.

Synchronization is invoked by setting the SOFTWARE SYNC control bit HIGH in the BCR. Completion of the synchronization sequence is indicated by the control bit clearing automatically to the LOW state. Clearing of the SOFTWARE SYNC bit is a condition for asserting the CHANNELS READY status flag (Paragraph 3.4.4), which can be selected as an interrupt request event.

The synchronization sequence has a duration of approximately 128 conversions for the lowest frequency channel.

3.6.3 Multiboard Operation

Multiple PCI-16SDI can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*. A board is designated as an initiator by setting the INITIATOR control bit HIGH in the BCR, or is designated as a target when the control bit is LOW.

Note: External clock and sync inputs can be provided from external sources other than an initiator board.

3.6.3.1 External Sample Clock

All target boards receive an external clock from the Clock Input I/O connection, and duplicate the input clock at the Clock Output I/O connection (Figure 3.6.1.1). The external clock input is assigned to specific channel groups on target boards by writing the "External Sample Clock" assignment code to the target boards' associated RATE ASSIGNMENTS registers described in Paragraph 3.6.1.2. For calculation of target board sample rates, the external sample clock corresponds to the rate generator frequency **Fgen** described in Section 3.6.1.

3.6.3.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board. The sequence has a duration of approximately 128 conversion cycles, after which all synchronized channels that have the same conversion rate sample their inputs simultaneously. Synchronized channels also can be harmonically locked by adjusting their sample rates to integral submultiples of the initiator sample rate.

3.7 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are implemented with hardware DAC's that retain the correction values until either: (a) power is removed or (b) autocalibration is invoked again.

Autocalibration is invoked by writing setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration, which has a maximum duration of approximately 3-10 seconds, depending on the average selected sample rate of all channels, is indicated by the AUTOCAL flag clearing automatically to the LOW state. Clearing of the AUTOCAL control bit is selectable as an interrupt request event. Read/write accesses from the PCI bus should be avoided during autocalibration. The autocalibration operation should be followed by initialization, in order to clear the contents of the analog input buffer.

NOTE: Read or write access from the PCI bus during autocalibration can disrupt the calibration process, and should be avoided. The "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful.

To ensure full conformance to the product specification, autocalibration should always be invoked after power has been applied to the board, after a change in input range or sampling rate, or after a software or hardware reset event has occurred. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. A warmup delay of 1-5 minutes is recommended.

3.8 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described below in Paragraph 3.8.2.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The source condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Transfer Buffer Almost Empty
6	Transfer Buffer Almost Full
7	(Reserved)

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX™ PCI-9080 reference manual..

3.9 DMA Operation

DMA transfers from the analog input buffer are supported in either of two DMA channels with the board operating as bus master. Table 3.9.1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0048h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***exceeds the selected buffer threshold*** *(Table 3.5.3).*

The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The number of values read from the buffer equals the threshold value plus one,
(c) The buffer is cleared,
(d) The board is reset,
(e) Autocalibration is executed.

The first occurrence of any of these events terminates the DMA request.

NOTE: Demand-mode DMA is available only with PCI-16SDI products that have Bit-15 (0000 8000h) set HIGH in the board revision register (Paragraph 3.12).

3.10 Buffer Size Register

The read-only register located at Offset 0040h contains the number of analog input values currently stored in the input data buffer.

NOTE: The value in the size register does not include the data values that have been transferred to the associated 256-location transfer FIFO (Paragraphs 3.5.1, 3.9.2). The internal FIFO arbiter attempts to keep the transfer FIFO full at all times, and extracts values from the 256K data FIFO until either the data FIFO is empty or the transfer FIFO is full.

3.11 Scan Synchronization

Although the data sequence for any specific channel in the data buffer represents the actual sampling sequence for that channel, the ordering of multiple channels in the buffer can vary due to the asynchronous nature of the sample clock relative to the board's master clock. These variations in channel order can occur even if all channels are synchronized to a common rate generator and are operating at the same sample rate.

Variations in the ordering of multiple channels can be eliminated by grouping all active channels into discrete scans, and by synchronizing the acquisition of each scan to the board's master clock. This ***scan-synchronization*** is effective only if all active channels are:

a. Channel-synchronized (Paragraph 3.6.2), and

b. Operating at a common sample rate that is derived from a single source.

Note: All preceding references to synchronization in this manual pertain to *channel-synchronization*, in which the sampling of all input channels occurs either simultaneously or at harmonics of a common base frequency. *Scan-synchronization* refers to synchronization of discrete data scans to the master clock.

In synchronized scans, the channel sequence for each scan in the buffer is ordered from lowest to highest. All samples in each scan represent the same sample event, and are arranged beginning with the lowest active channel and proceeding upward through the highest active channel. Table 3.11.1 illustrates examples of channel sequences in both synchronized and nonsynchronized scans in which all channels are active. Scan synchronization is invoked by setting the SYNCHRONIZE SCAN control bit HIGH in the BCR.

Table 3.11.1. Channel Order (Active channels 00-05)

	CHANNEL ORDER	
SAMPLE EVENT	**NON-SYNCHRONIZED SCANS (Typical)**	**SYNCHRONIZED SCANS**
Tn	345012	012345
Tn+1	501234	012345
Tn+2	012345	012345
Tn+3	450123	012345
Tn+4	123450	012345

The following procedure illustrates one method of implementing scan-synchronization:

1. Assign all active channels to the same clocking source, and adjust all channels to the same sample rate. Wait for the CHANNELS READY flag in the BCR to go HIGH.

2. Synchronize all active channels by setting the SOFTWARE SYNC control bit HIGH in the BCR. Wait for the CHANNELS READY flag in the BCR to go HIGH.

3. Set the SYNCHRONIZE SCAN control bit HIGH in the BCR (Table 3.2). Wait for the CHANNELS READY flag in the BCR to undergo a LOW-to-HIGH transition

4. Clear the buffer by setting and clearing the CLEAR BUFFER control bit in the Buffer Threshold register (Table 3.5.3).

NOTE: If one or more target boards are synchronized to a single initiator (3.6.3), clear the buffers on all boards by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR, then writing the SOFTWARE SYNC bit HIGH.

The CHANNELS READY flag falls LOW, the buffer clears to empty, and the first two scans are discarded to ensure full synchronization. At the end of this sequence, the CHANNELS-READY flag returns HIGH and all subsequent samples are scan-synchronized as described above.

3.12 Board Revision Register

The board revision register (Table 3.12.1) contains the existing firmware revision, and a status field that indicates the availability of optional features.

Table 3.12.1. Board Revision Register

REG BIT	MODE *	DESCRIPTION
D00-D11	RO	Firmware Revision
D12-D14	RO	(Reserved status flags).
D15	RO	High if both block-mode and demand-mode DMA operations are available. LOW if only block-mode operation is available.
D16	RO	High if the board contains only eight input channels.
D17	RO	High if the board contains only four input channels.
D18-D31	RO	(Reserved)

* RO = Read-only.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PCI-16SDI board contains sixteen sigma-delta A/D converters and all supporting functions necessary for adding analog I/O capability to a PCI expansion system. As Figure 4.1 illustrates, a PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

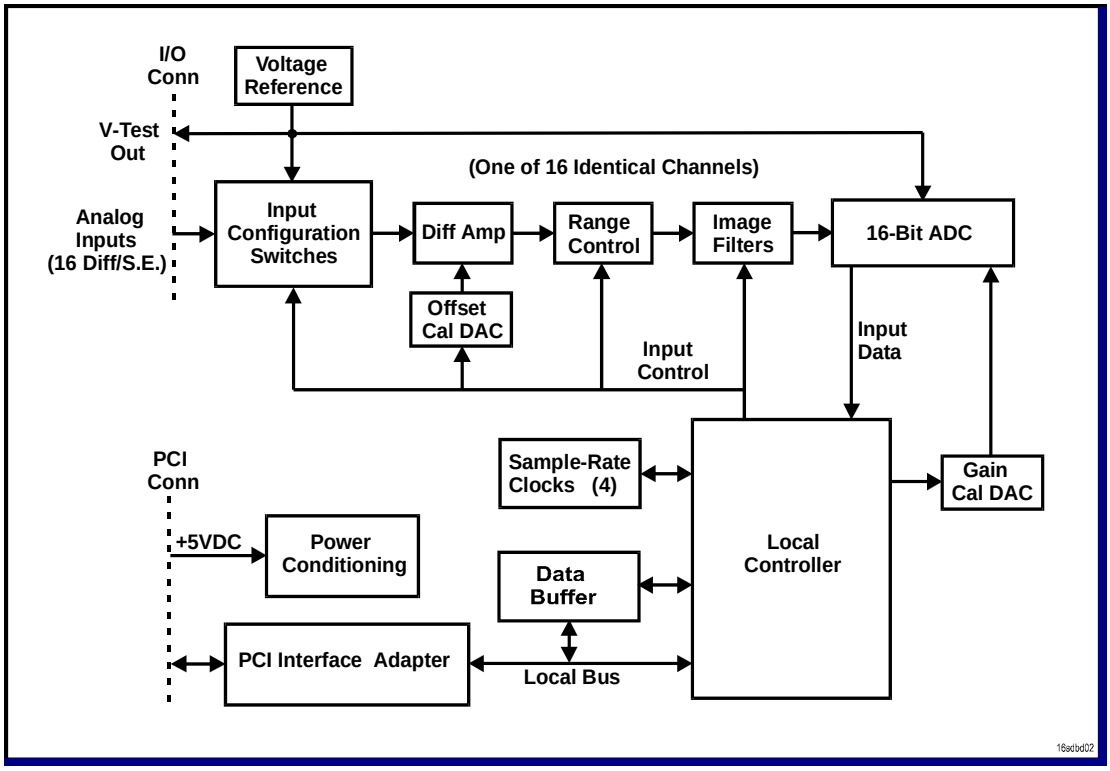

Figure 4.1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibration of each input channel is adjusted with a pair of 12-bit Calibration DAC's, the control values for which are determined during autocalibration.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a differential amplifier, which removes common mode errors from the signal, and which accepts the output from the offset DAC as the channel offset correction voltage. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or positive full-scale reference voltage.

A range control attenuator adjusts the maximum level of the signal to the full-scale input range of 0/+2.5 Volts required by the ADC. High frequency noise and digital filter images are attenuated by a lowpass filter, the cutoff frequency of which is adjusted automatically to be compatible with the selected sample rate.

The final conditioned, scaled and filtered input signal is digitized by the ADC into a serial 16-bit data word, which is deserialized into parallel format by the local controller. The local controller then attaches a 4-bit channel tag to the data word and transfers the 20-bit result to the input data buffer. Channel gain calibration is accomplished by adjusting the reference voltage used by the ADC.

Antialias filtering is provided by each ADC in the form of a lowpass digital filter with a sharp cutoff frequency at approximately 47 percent of the sampling frequency. The digital filter has no filtering effect at multiples of 64 times the sampling frequency (i.e.: 64x, 128x,...). To prevent extraneous signal frequency components within these "filter images" from aliasing into the passband, the hardware image filters shown in Figure 4.1 are configured automatically to provide filtering within the digital filter images.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is adjusted to equal 99.000 percent of the maximum input voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

The gain of each channel is adjusted first, with the offset DAC adjusted to maximum negative correction. The values obtained from the ADC with its input at full-scale and zero levels are subtracted to determine the effective gain of the channel, and the gain DAC is adjusted until the gain is correct. After the gain has been corrected, the offset DAC is adjusted until a zero input level produces the required midrange (zero) digital value from the ADC.

Each 12-bit calibration DAC is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 12 bits have been tested and adjusted.

4.4 Sampling Clocks

Four independent sample rate generators provide four distinct clocks, each of which can be used by any or all of the four 4-channel groups present on the board. Each of the four channels in each group can further divide the sample rate generator assigned to the group by any integer from 1 through 32. Because the ADC's operate with an oversampling factor of 64, the sample rate clocks are adjustable from 320 kHz to 14.08 MHz to provide the required sample rates from 5KSPS to 220KSPS.

One of the four rate generators can be routed to the I/O connector as a clock output signal, to phase lock the converters on other boards to a common clock. To further support this feature, the external clock input can be selected as the rate generator for any channel group on the board. A board on which a sample rate clock output originates is a *clock initiator*. Boards that receive and retransmit the external clock are *clock targets*.

4.5 Power Control

Regulated supply voltages of +5 Volts and ±14 Volts are required by the analog networks. Two DC/DC converters in the power conditioner produce +6VDC and ±16VDC voltages from the PCI +5 Volt bus. These voltages subsequently are filtered and series-regulated to the required output levels of +5VDC and ±14VDC. The series regulators following the DC/DC converters ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers and principal control-bit fields, in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

LOCAL ADDR	ACCESS MODE *	REGISTER	DEFAULT	DESCRIPTION
00	R/W	BOARD CONTROL	0000 383Ch	Board Control Register (BCR)
04	R/W	RATE CONTROL A	0000 0000h	Rate control for Rate Generator-A
08	R/W	RATE CONTROL B	0000 0000h	Rate control for Rate Generator-B
0C	R/W	RATE CONTROL C	0000 0000h	Rate control for Rate Generator-C
10	R/W	RATE CONTROL D	0000 0000h	Rate control for Rate Generator-D
14	R/W	RATE ASSIGNMENTS	0000 3210h	Channel-group rate generator assignments
18	R/W	RATE DIVISOR 00,01	0000 0505h	Channels 00 and 01 sample rate divisors
1C	R/W	RATE DIVISOR 02,03	0000 0505h	Channels 02 and 03 sample rate divisors
20	R/W	RATE DIVISOR 04,05	0000 0505h	Channels 04 and 05 sample rate divisors
24	R/W	RATE DIVISOR 06,07	0000 0505h	Channels 06 and 07 sample rate divisors
28	R/W	RATE DIVISOR 08,09	0000 0505h	Channels 08 and 09 sample rate divisors
2C	R/W	RATE DIVISOR 10,11	0000 0505h	Channels 10 and 11 sample rate divisors
30	R/W	RATE DIVISOR 12,13	0000 0505h	Channels 12 and 13 sample rate divisors
34	R/W	RATE DIVISOR 14,15	0000 0505h	Channels 14 and 15 sample rate divisors
38	R/W	BUFFER THRESHOLD	0003 FFFEh	Input buffer control and status threshold
3C	RO	Firmware Revision **	---	---
40	RO	BUFFER SIZE	---	Number of ADC values in the input buffer.
44	RO	Autocal Values **	---	---
48	RO (DMA)	INPUT DATA BUFFER	---	Input Data Buffer; Data and channel tag
4C	R/W	Auxiliary register **	---	Reserved 20-Bit auxiliary register.
50-7C	--	(Reserved)	---	---

* R/W = Read/Write; RO = Read-Only. ** Maintenance register. Shown for reference only.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 383Ch**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects input configuration or selftest mode. Defaults to differential input mode.
D01	R/W	AIM1	
D02	R/W	RANGE0	Analog input range selection. Defaults to ±10V range.
D03	R/W	RANGE1	
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults to offset binary.
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults HIGH to Initiator mode.
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.
D07	R/W	*AUTOCAL	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.
D09	R/W	INTERRUPT A1	
D10	R/W	INTERRUPT A2	
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D12	RO	AUTOCAL PASS	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.
D13	RO	CHANNELS READY	LOW during change in channel parameters. Asserted HIGH when inputs are ready to acquire data.
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.
D15	R/W	*INITIALIZE	Initializes the board when asserted. Sets all defaults.
D16	R/W	SYNCHRONIZE SCAN	Selects synchronous sampling mode.
D17	R/W	CLEAR BUFFER ON SYNC	When this bit is HIGH, the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.
D18-31	RO	(Reserved)	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Register value changes to 0000 783Ch approximately 400 milliseconds after initialization.

Table 3.4. Analog Input Function Selection

AIM[1:0]	FUNCTION OR MODE
0	Differential analog input mode.
1	Single-Ended analog input mode.
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.4.3. Analog Input Range Selection

RANGE[1:0]	ANALOG INPUT RANGE
0	±1.25 Volts
1	±2.5 Volts
2	±5 Volts
3	±10 Volts

Table 3.5.2. Input Buffer Data Organization

Offset: 0000 0048h **Default: N/A**

CHANNEL TAG			CHANNEL DATA VALUE		
D19 (MSB)	D17-D18	D16 (LSB)	D15 (MSB)	D01-D14	D00 (LSB)

Table 3.5.3. Buffer Threshold Register

Offset: 0000 0038h **Default: 0003 FFFEh**

REGISTER BITS	ACCESS MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold
D[18]	R/W	DISABLE BUFFER INPUT	Disables ADC inputs to the buffer
D[19]	R/W	CLEAR BUFFER	Clears (empties) the buffer
D[31..20]	RO	(Reserved)	

Table 3.6.1.1. Channel Groups

	INPUT CHANNELS		
CHANNEL GROUP	16-CHANNEL BOARD	8-CHANNEL BOARD	4-CHANNEL BOARD
0	00,01,02,03	00,01	00
1	04,05,06,07	02,03	01
2	08,09,10,11	04,05	02
3	12,13,14,15	06,07	03
(Reserved)	---	---	---

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 0014h **Default: 0000 3210h**

REGISTER BITS	ACCESS MODE	DESIGNATION	CHANNEL GROUP
D[03..00]	R/W	ASSIGN 0	0
D[07..04]	R/W	ASSIGN 1	1
D[11..08]	R/W	ASSIGN 2	2
D[15..12]	R/W	ASSIGN 3	3
D[31..16]	RO	(Reserved, read-only)	(Reserved)

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	ASSIGNMENT
0	Generator-A
1	Generator-B
2	Generator-C
3	Generator-D
4	External Sample Clock
5-15	None (Disabled)

Table 3.6.1.3. Rate Divisor Registers

Offset: (As Shown in table) **Default: 0000 0505h**

REGISTER BITS	REG 00,01	REG 02,03	REG 04,05	REG 06,07	REG 08,09	REG 10,11	REG 12,13	REG 14,15
D[05..00]	CHAN 00	02	04	06	08	10	12	14
D[07..06]	*	*	*	*	*	*	*	*
D[13..08]	CHAN 01	03	05	07	09	11	13	15
D[31..14]	*	*	*	*	*	*	*	*
Offset:	0018h	001Ch	0020h	0024h	0028h	002Ch	0030h	0034h

* Reserved read-only bit(s).

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Transfer Buffer Almost Empty
6	Transfer Buffer Almost Full
7	(Reserved)

Table 3.9-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0048h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.11.1 Channel Order (Active channels 00-05)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	345012	012345
Tn+1	501234	012345
Tn+2	012345	012345
Tn+3	450123	012345
Tn+4	123450	012345

Table 3.12.1. Board Revision Register

REG BIT	MODE *	DESCRIPTION
D00-D11	RO	Firmware Revision
D12-D14	RO	(Reserved status flags).
D15	RO	High if both block-mode and demand-mode DMA operations are available. LOW if only block-mode operation is available.
D16	RO	High if the board contains only eight input channels.
D17	RO	High if the board contains only four input channels.
D18-D31	RO	(Reserved)

* RO = Read-only.

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