XMC-24DSI24WRC
Wide-Range 24-Bit, 24-Channel, 200KSPS
XMC Analog Input Module
With 24 Wide-Range (High-Level, Low-Level) Delta-Sigma Input Channels

Features Include:

- 24 wide-range differential 24-Bit simultaneously-sampled analog input channels.

- Sample rates from 1.0 Kilosamples per second (KSPS) to 200 KSPS per channel.

- Synchronous operation; all channels clocked simultaneously.

- Software-selectable analog input ranges of ±10V, ±1V, ±100mV, ±10mV. (Optional ±10V, ±5V, ±2V, ±1V ranges, or ±5V, ±0.5V, 50mV, ±5mV ranges also available).

- Delta-Sigma input conversion minimizes or eliminates the need for antialias filtering.

- Low noise: 106dB typical dynamic range.

- 256K-sample analog input FIFO buffer.

- Sample clock source selected as internal or external.

- Hardware sync and clock I/O for multiboard synchronization.

- On-demand autocalibration ensures DC offset precision as well as AC performance.

- Conforms to PCI Express Specification revision 1.0a, single-lane.

- DMA engine supports both block-mode and demand-Mode transfers.

- Integrated DC/DC conversion and regulation of precision internal supply voltages.

Applications:

- ✓ Sonar Arrays
- ✓ Analog Inputs
- ✓ Voltage Acquisition
- ✓ Acoustic Research
- ✓ Low-level Inputs
- ✓ Audio Waveform Analysis

PRELIMINARY

REV 062415

Overview:

The 24-channel XMC-24DSI24WRC analog input module provides high-density 24-bit analog input resources on a standard single-width XMC. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms.

Functional Description:

Each of the 24 analog input channels contains a lowpass image filter, and a delta-sigma A/D converter that provides inherent antialias suppression and sharp cutoff lowpass filtering. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration. A linear-phase digital antialiasing filter rejects out-of-band signals, and a lowpass analog filter minimizes those interference signals that fall within the harmonic images of the digital filter.

An internal sample-rate generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide individual channel sample rates from 1.0KSPS to 200KSPS in three selectable power modes. Conversion data from all active channels is transferred to the PCI Express bus through a 256K-sample data buffer that is supported by two DMA channels. Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals.
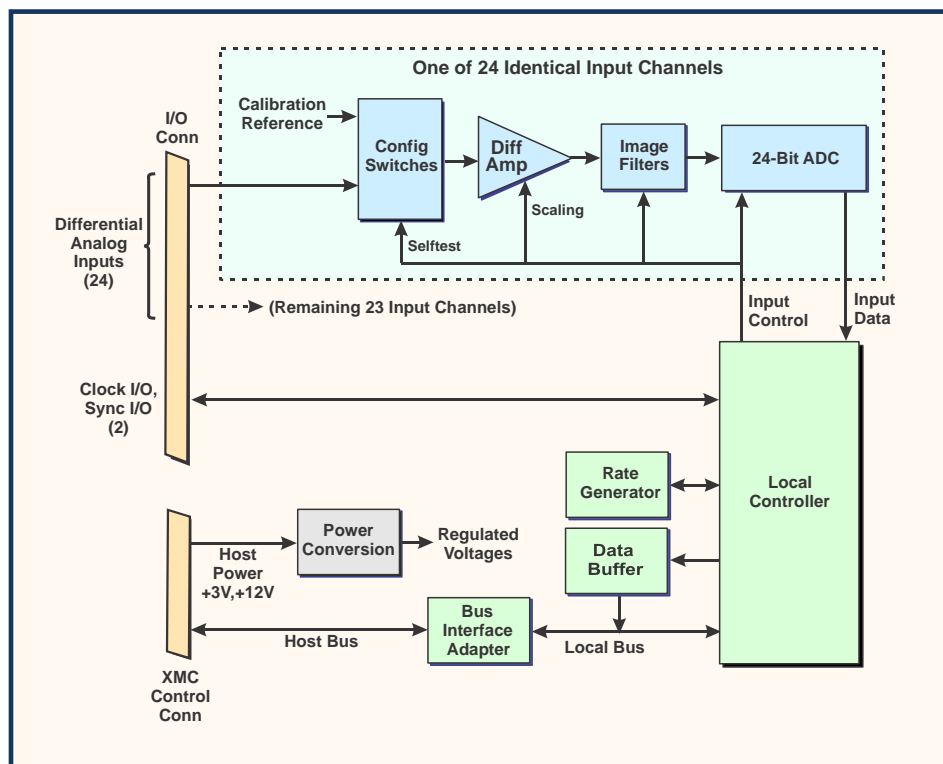

Figure 1. XMC-24DSI24WRC; Functional Organization

This product is functionally compatible with the PCI Express Specification revision 1.0a. System input/output connections are made at the front panel through a high-density 80-Pin connector. Power requirements consist of +3.3 VDC and +12 VDC in compliance with the PCI Express specification, and operation over the specified temperature range is achieved with conventional air cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating conditions.

Input Characteristics:

Configuration:	24 differential input channels. 16 and 8-channel configurations available.
Voltage Range:	Software Configurable as ±10V, ±1V, ±100mV or ±10mV. (See Ordering Information for optional range sets)
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2.0 Megohms line-line.
Common Mode Rejection:	80dB to 15kHz on ±10V range; 95dB on lower ranges; typical
Common Mode Range:	±11 Volts with zero normal-mode input
Overvoltage Protection:	±25-Volt transients with power applied; ±12 Volts with power removed

Transfer Characteristics:

Conversion Architecture: 24-Bit Delta-Sigma

Sample Rate: 1-200 kilosamples per second in three selectable power modes.

Decimation Rate: Selectable as x32, x64, x128 or x1024.

DC Accuracy:
(Mean composite error
  after autocalibration)

Input Range	Midrange (Zero) Accuracy	Gain Accuracy
±10V	±1.0mv	±6.0mv
±1V	±0.3mv	±1.0mv
±100mV	±0.08mv	±0.20mv
±10mV	±0.02mv	±0.05mv

Passband; -3dB	DC to typically 43 percent of the selected sample rate.
Passband Ripple:	±0.01 dB maximum.
Stopband threshold:	Typically 50 percent of the selected sample rate.
Stopband Attenuation:	110dB typical.
-3dB Bandwidth	DC to typically 49 percent of the selected sample rate.
Integral Nonlinearity (INL)	0.001 percent of fullscale range; typical.
No Missing Codes	24 Bits.
Dynamic Range:	106dB typical.
Harmonic Distortion (THD):	105dB typical.
Group Delay:	Selectable as 32/Fsamp or 4/Fsamp (Fsamp equals the sample rate).
Antialias Filtering:	Each ADC provides linear-phase digital lowpass filtering as indicated for "passband" and "stopband". In addition to the digital filter, a single-pole lowpass analog image filter in each channel provides a -3dB cutoff frequency of approximately 200kHz to suppress images from the digital filter. Optional alternative image filter frequencies are available, and should be selected to be well above the expected passband.

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Operating Modes and Controls:

Organization:

All input channels operate at the same sample rate, controlled by division of an internal or external rate generator frequency.

Sampling Clock I/O:

The sampling clock can be derived either from an internal rate generator, or from a TTL or LVDS external hardware input. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. The 'star-configuration' also is supported.

Internal Rate Generator:

An internal PLL rate generator provides sample rates from 1.0 KSPS to 200 KSPS. The frequency of the generator is controlled by the ratio of two 10-Bit integers, and setting accuracy is 25 PPM.

Synchronization:

Daisy-chained or 'star-configuration' hardware sync inputs and outputs can be used to synchronize sampling among multiple boards.

Burst Timing:

Triggered burst sampling can be timed either internally or externally.

Data Format:

Software-selectable as either offset binary or two's complement. Data width is selectable as 16, 18, 20 or 24 bits.

Channel Tags:

A 5-bit channel tag is appended to each input data value.

Buffer Access:

The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.

Auxiliary External Sync I/O:

A 6-pin connector on the back of the module provides clock and sync I/O capability within the enclosure.

PCIe Compatibility:

Conforms to PCIe Specification revision 1.0a.
Supports block-mode and demand-mode DMA transfers as bus master with two DMA channels.

Power Requirements:

24-Channel Configuration:
+3.3±0.3VDC at 1.0 Amps typical; 1.2 Amps max. +12.0±0.8VDC at 0.6 Amp typical; 0.7 Amp max.
Maximum power dissipation: 12 Watts.

Mechanical Characteristic:

Dimensions (HxWxD): 13.5 mm (0.53 in) x 74.0 mm (2.91 in) x 149.0 mm (5.87 in)

Environmental Specifications:

Ambient Temperature Range:

Standard Temperature:

Operating: 0 to +70 Degrees Celsius *
Storage: -40 to +85 Degrees Celsius

Extended Temperature:

Operating: -40 to +80 Degrees Celsius *
Storage: -40 to +85 Degrees Celsius

* Air temperature at board surface.

Relative Humidity:

0 to 95%, non-condensing

Altitude:

Operation to 10,000 ft.

Cooling:

Conventional air cooling; 150 LFPM

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Ordering Information:

Specify the basic product model number followed by an option suffix "-A-B-C-D as indicated below. For example, model number XMC-24DSI24WRC-16-SR-SF-0 describes a XMC module with 16 input channels, standard input ranges, standard image filter frequency, and no custom features. For industrial (extended) temperature operation, add "-I" at the end of the model number.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	8 Channels	A = 8
	16 Channels	A = 16
	24 Channels	A = 24
Input Voltage Range	Standard ±10V, ±1V, ±100mV, ±10mV	B = SR
	±10V, ±5V, ±2V, ±1V	B = R1
	±5V, ±500mV, ±50mV, ±5mV	B = R2
	(TBD)	B = Rx
Image Filter -3dB Frequency	Standard 200kHz	C = SF
	Custom Frequencies:	C = CFxK *
	No Filter:	C = NF
Custom Features	No custom features	D = 0

* "x" indicates filter frequency in kilohertz. ±15% frequency accuracy, 1kHz-300kHz. Contact factory for availability of specific frequencies.

SYSTEM I/O CONNECTIONS

Table 1. System I/O Connector

ROW-A		ROW-B	
PIN	SIGNAL	PIN	SIGNAL
1	INP00 LO	1	INP12 LO
2	INP00 HI	2	INP12 HI
3	INP01 LO	3	INP13 LO
4	INP01 HI	4	INP13 HI
5	INPUT RTN	5	INPUT RTN
6	INPUT RTN	6	INPUT RTN
7	INP02 LO	7	INP14 LO
8	INP02 HI	8	INP14 HI
9	INP03 LO	9	INP15 LO
10	INP03 HI	10	INP15 HI
11	INPUT RTN	11	INPUT RTN
12	INPUT RTN	12	INPUT RTN
13	INP04 LO	13	INP16 LO
14	INP04 HI	14	INP16 HI
15	INP05 LO	15	INP17 LO
16	INP05 HI	16	INP17 HI
17	INPUT RTN	17	INPUT RTN
18	INPUT RTN	18	INPUT RTN
19	INP06 LO	19	INP18 LO
20	INP06 HI	20	INP18 HI
21	INP07 LO	21	INP19 LO
22	INP07 HI	22	INP19 HI
23	INPUT RTN	23	INPUT RTN
24	INPUT RTN	24	INPUT RTN
25	INP08 LO	25	INP20 LO
26	INP08 HI	26	INP20 HI
27	INP09 LO	27	INP21 LO
28	INP09 HI	28	INP21 HI
29	INPUT RTN	29	INPUT RTN
30	INPUT RTN	30	INPUT RTN
31	INP10 LO	31	INP22 LO
32	INP10 HI	32	INP22 HI
33	INP11 LO	33	INP23 LO
34	INP11 HI	34	INP23 HI
35	INPUT RTN	35	INPUT RTN
36	DIGITAL RTN	36	DIGITAL RTN
37	EXT CLK INP LO	37	EXT CLK OUT LO
38	EXT CLK INP HI *	38	EXT CLK OUT HI *
39	EXT SYNC INP LO	39	EXT SYNC OUT LO
40	EXT SYNC INP HI *	40	EXT SYNC OUT HI *

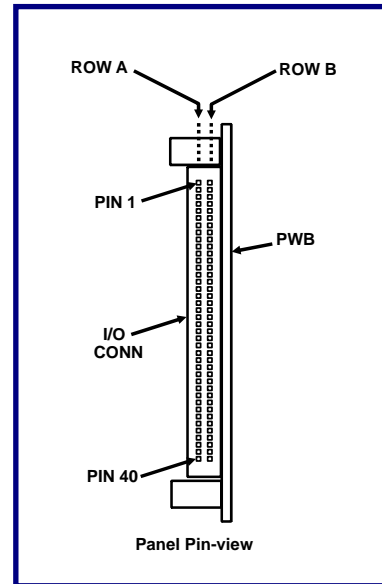* TTL signal levels when TTL sync I/O is selected. Otherwise LVDS.

Figure 2. System I/O Connector

System Mating Connector:
Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG**
or equivalent.

PIN	SIGNAL
1	DIGITAL RTN
2	AUX CLOCK
3	DIGITAL RTN
4	AUX SYNC
5	DIGITAL RTN
6	Reserved. Ground or leave disconnected.