General Standards Corporation

High Performance Bus Interface Solutions

Rev: 112911

PMC66-18AISS6C

Six-Input 18-Bit Precision Wideband 550KSPS Analog Input PMC

REFERENCE MANUAL

- PRELIMINARY -

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SECTION 1.0

INTRODUCTION

The PMC66-18AISS6C is a precision 18-Bit analog input PMC product that provides six simultaneously sampled input channels. The inputs can be sampled at rates up to 550 KSPS per channel, and are supported by a 256K-Sample FIFO data buffer. Both continuous and burst clocking modes are supported. The input range [1] is software-selectable as ±20V or ±10V, or optionally as ±10V or ±5V. Clocking and burst-triggering rates can be derived either from internal rate generators, or from external clock and trigger sources to support the synchronous operation of multiple boards.

Input sampling employs successive-approximation (SAR) conversion, which avoids the high latency or minimum-rate limitations of delta-sigma and pipelined conversion schemes.

On-demand autocalibration determines and applies error correction for all input channels, and a selftest input switching network permits board integrity to be verified by the host. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

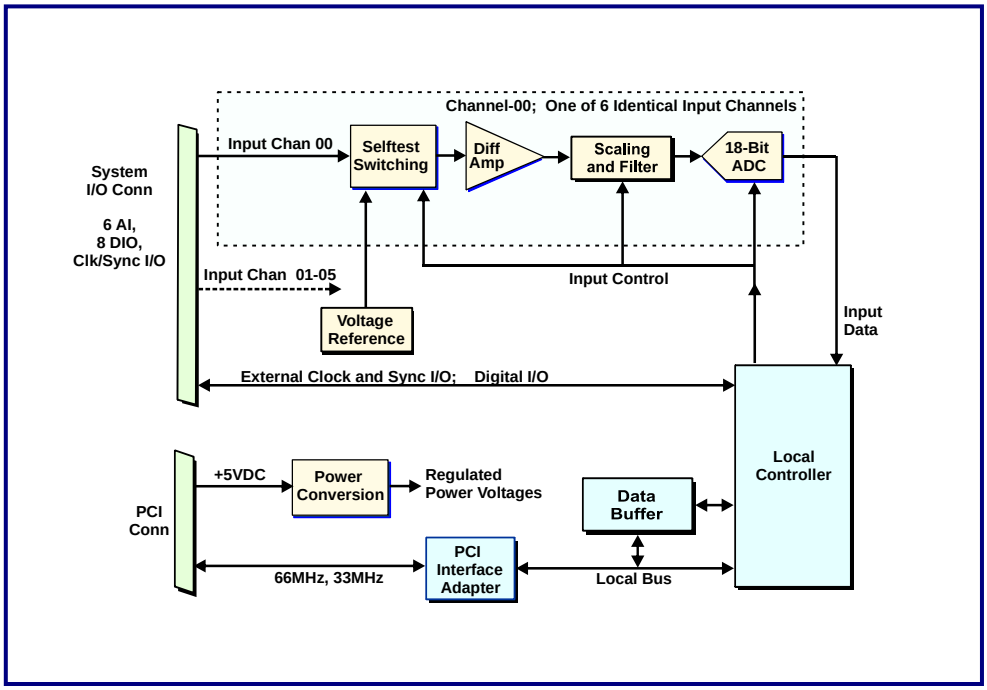

Figure 1.1-1. Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density dual-ribbon 68-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

[1] Input range is defined here as the entire active range of voltage differences between the two conductors in a differential HI/LO input pair. 'Equal to ±Vpk, or ±1/2*Vpp.

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SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping package. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping package, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping package, position the board with the two PCI connectors facing the mating connectors J1, J2 on the host board (Figure 2.2-1). Then carefully press the board into position on the host. Verify that the mezzanine connectors have mated completely and that the board is seated firmly against the host board. Attach the board to the host with 2.5 x 6.5mm panhead screws. Pass the screws through the host board into the corresponding mounting holes in the standoffs and front-panel bezel. Tighten the screws carefully to complete the installation. Do not overtighten.

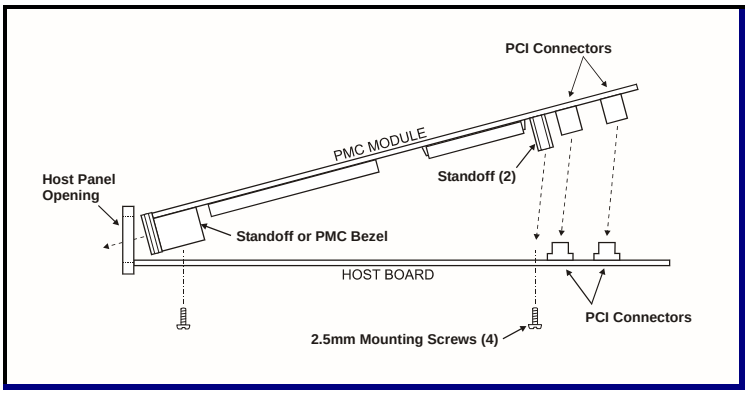

Figure 2.2-1. Mechanical Installation

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with a 68-pin dual-ribbon connector equivalent to AMP #749621-7. The AMP insulation-displacement connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-2. A second connector, listed in Table 2.2-2, makes multiboard synchronization signals available within the system enclosure. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connections

ROW-A	
PIN	SIGNAL
1	INPUT RTN
2	INPUT RTN
3	INPUT 00 LO
4	INPUT 00 HI
5	INPUT RTN
6	INPUT RTN
7	INPUT 01 LO
8	INPUT 01 HI
9	INPUT RTN
10	INPUT RTN
11	INPUT 02 LO
12	INPUT 02 HI
13	INPUT RTN
14	INPUT RTN
15	INPUT 03 LO
16	INPUT 03 HI
17	INPUT RTN
18	INPUT RTN
19	INPUT 04 LO
20	INPUT 04 HI
21	INPUT RTN
22	INPUT RTN
23	INPUT 05 LO
24	INPUT 05 HI
25	INPUT RTN
26	INPUT RTN
27	VTEST LO
28	VTEST HI
29	INPUT RTN
30	INPUT RTN
31	INPUT RTN
32	INPUT RTN
33	INPUT RTN
34	INPUT RTN

ROW-B	
PIN	SIGNAL
1	DIGITAL RTN
2	DIGITAL RTN
3	DIGITAL RTN
4	DIGITAL RTN
5	DIGITAL RTN
6	DIGITAL RTN
7	DIGITAL RTN
8	DIGITAL RTN
9	DIGITAL RTN
10	DIGIO 00
11	DIGITAL RTN
12	DIGIO 01
13	DIGITAL RTN
14	DIGIO 02
15	DIGITAL RTN
16	DIGIO 03
17	DIGITAL RTN
18	DIGIO 04
19	DIGITAL RTN
20	DIGIO 05
21	DIGITAL RTN
22	DIGIO 06
23	DIGITAL RTN
24	DIGIO 07
25	DIGITAL RTN
26	INP TRIG OUT *
27	DIGITAL RTN
28	INP TRIG INP *
29	DIGITAL RTN
30	INP CLK OUT *
31	DIGITAL RTN
32	INP CLK INP *
33	DIGITAL RTN
34	DIGITAL RTN

* TTL, asserted LOW.

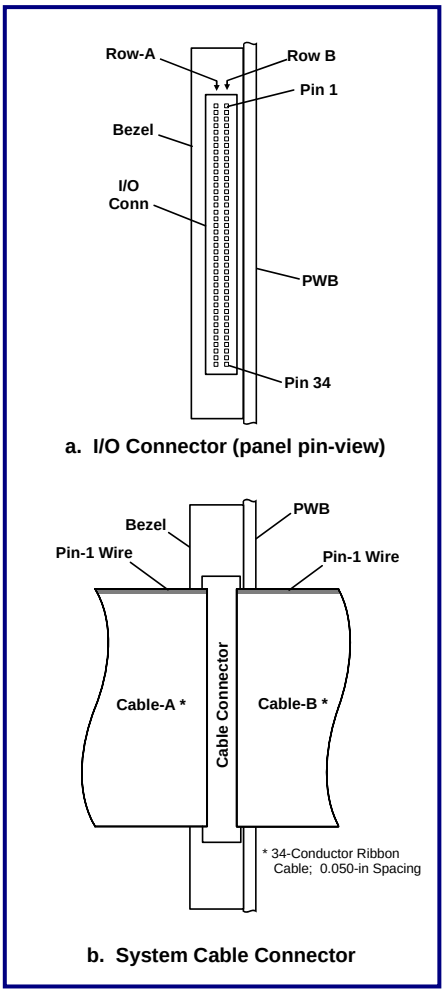

Figure 2.2-2. System I/O Connector

Table 2.2-2. Sync-I/O Connector (Side-2)

PIN	SIGNAL
1	DIGITAL RTN
2	AUX CLOCK I/O
3	DIGITAL RTN
4	AUX SYNC I/O
5	DIGITAL RTN
6	(No internal connection)

Recommended Sync-I/O mating cable connector is:
Molex# 51146-0600.

System Cable Mating Connector:
68-pin 0.050" Subminiature connector
with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**
Amp # 787170-7.

2.3 System Configuration

2.3.1 Analog Inputs

The six analog input channels can be externally configured for either differential or single-ended operation.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials.

This operating mode also offers the highest rejection of the common mode noise, which is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode (Figure 2.3-1b), the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a remote ground point that ensures that both the HI and LO inputs remain within the specified maximum input level. Ground current through the INPUT RTN pins must be limited in order to avoid damage to the cable or to the input board.

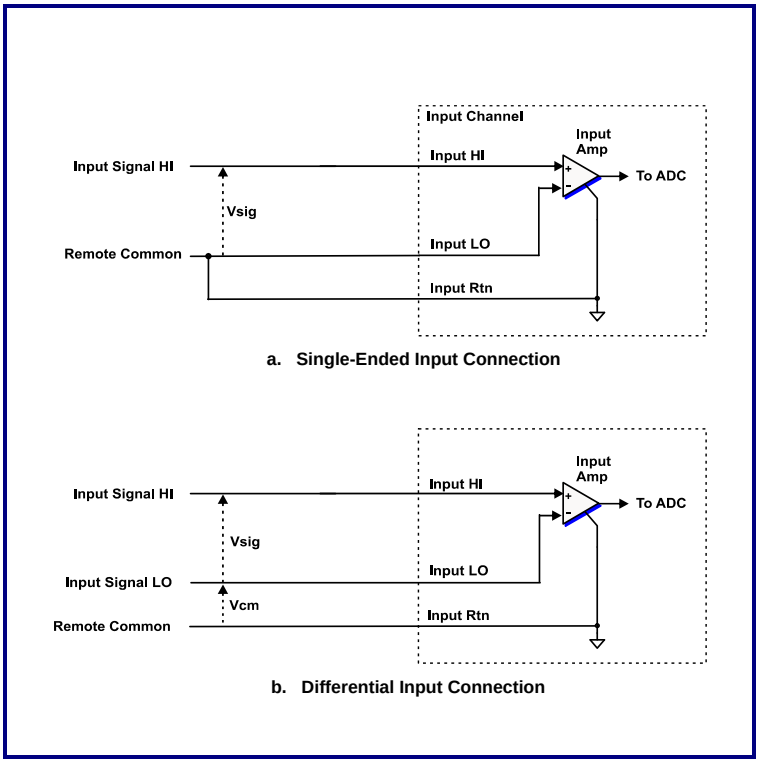

Figure 2.3-1. Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1a) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. Single-ended inputs usually are more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or could generate potentially destructive ground current.

2.3.2 Multiboard Synchronization

If multiple boards are to be synchronized together, the clock and/or trigger lines can be interconnected between boards in either a 'multidrop' configuration (Figure 2.3-2), or in a daisy-chained sequence (Figure 2.3-3). The multidrop arrangement eliminates the approximately 100ns delay incurred when passing through each board in a daisy-chain sequence, but limits the number of target boards to approximately four-six, depending upon the relative locations and separation of the synchronized boards. The number of target boards in a daisy-chain sequence is limited only by the number of slots available in a backplane and the maximum acceptable total delay through the targets.

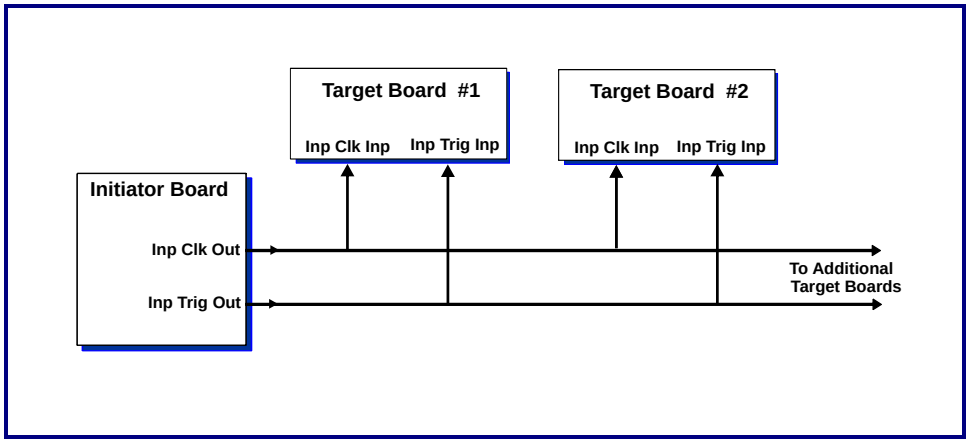

Figure 2.3-2. Multidrop Multiboard Synchronization

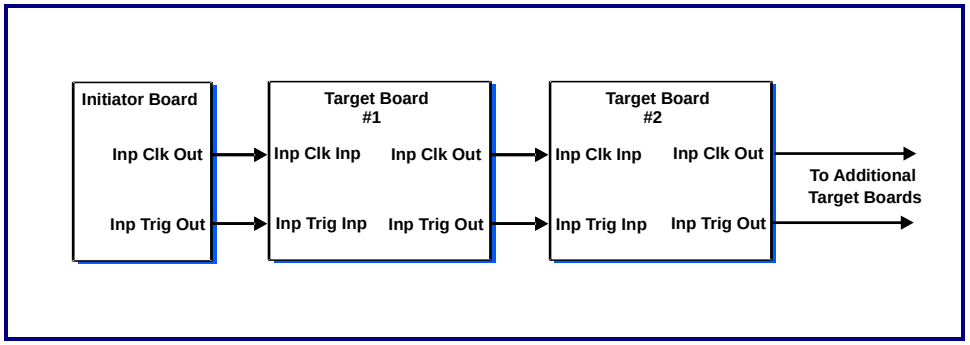

Figure 2.3-3. Daisy-Chain Multiboard Synchronization

The board that initiates the clock and trigger signals is software-designated as the **initiator**, and the clock and trigger receivers are designated as **targets**. The initiator and all targets should all reside in the same backplane. Standard TTL levels are used for all clock and trigger signaling.

2.3.3 External Sync I/O

An initiator can be replaced with an external source of synchronization signals if the following conventions are observed:

- Logic levels are TTL. Input loading is less than 0.2ma. Maximum output loading is 10mA.
- Clocks and triggers are edge-detected and are asserted LOW (i.e.: falling edge).
- Minimum input pulse width is 120ns.

External devices can be synchronized to an initiator board by recognizing a clock or trigger event as a TTL logic-LOW pulse with a minimum width of 150ns.

2.4 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the range references. The optimum verification interval will vary with the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog channels are calibrated to internal voltage references by an embedded autocalibration utility. The references are scaled for each of two basic input ranges, and a separate adjustment is provided for each range. The procedure presented here describes the verification and adjustment of the range references.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter, 5-1/2 digit, 0.001% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host board with available PMC site	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to the system I/O connector.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the two internal range references. Adjustment of the references, if necessary, is performed with two internal trimmers, RT1 and RT2, which are located as shown in Figure 2.5-1.

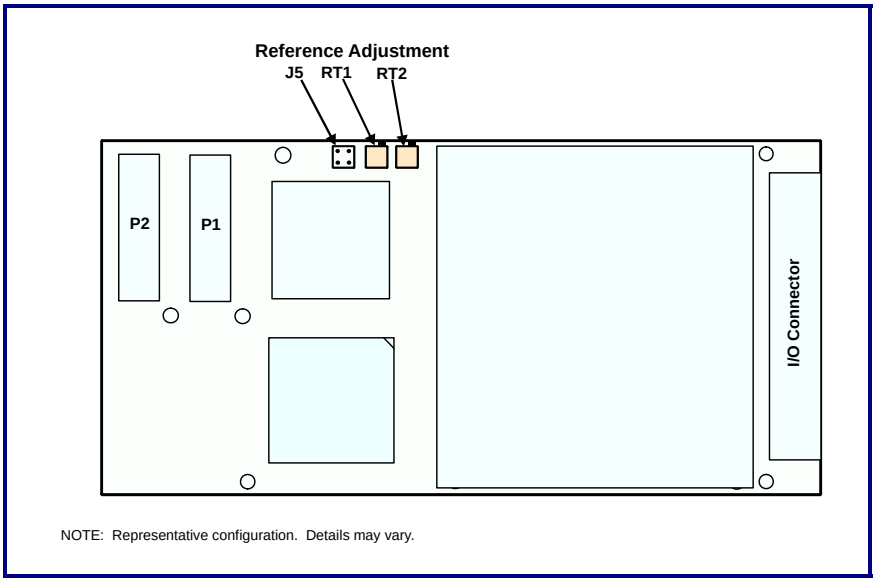

Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the board under test is installed in an operational PCI host.

1. Connect the digital multimeter between the VTEST HI(+) pin and the VTEST LO (-) pin in the system I/O connector (Table 2.2-1). Alternatively, use internal test connector J5 Pin-1(+) and J5 Pin-2(-) shown in Figure 2.5-1.

   NOTE: Neither of these pins is connected to ground, and the digital multimeter inputs must be both differential and ungrounded.

2. If power has been removed from the board, apply power now. Wait at least 15 minutes after power is applied before proceeding.

3. Select the High input range in the Input Configuration register.

   NOTE: If the board is factory-configured with the High-Range set, then the high range is ±20V and the low range is ±10V. If configured for the Low-Range set, the high range is ±10V and the low range is ±5V. The available range set is identified in the **Assembly Configuration Register described in Section-3.**

4. If the digital multimeter indicates a voltage that is outside the corresponding range listed in Table 2.5-2, then adjust trimmer RT1 (Figure 2.5-1) until the voltage is within the indicated tolerance range.

5. Select the Low input range in the Input Configuration register, and repeat Step-4, using RT2 to make any necessary adjustments.

5. Verification and adjustment is completed. Remove all test connections.

Table 2.5-2. Range Reference Voltages

		Adjustment Trimmer	
Input Range	**Range Reference**	**High-Range Set**	**Low-Range Set**
±20V	+19.8000VDC ±0.0018VDC	RT1	
±10V	+9.9000VDC ±0.0009VDC	RT2	RT1
±5V	+4.9500VDC ±0.0005VDC		RT2

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SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-18AISS6C is compatible with the PCI Local Bus specification Revision 2.3, and a PLX™ PCI-9056 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All data transfers are long-word D32. DMA access is supported for data transfers from the analog input buffer. To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero).

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	0022 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	000X 000Xh	Digital I/O port data.	3.8
0008	(Reserved)	RO	0000 0000h	---	---
000C	(Reserved)	RO	0000 0000h	---	---
0010	AUXILIARY SYNC IO	RW	0000 0000h	Auxiliary external clock and trigger I/O.	3.13
0014	INPUT CONFIGURATION	RW	0010 003Fh	Analog input configuration.	3.4
0018	INPUT DATA BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0000 01C2h	Rate-A generator divider; 24 bits.	3.6
0020	RATE GENERATOR B	RW	0000 2BF2h	Rate-B generator divider; 24 bits.	3.6
0024	INPUT BURST BLOCK SIZE	RW	0000 0400h	Analog input burst size.	3.4.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h`	Number of data values in the input buffer.	3.4.5.2
002C	INPUT BUFFER THRESHOLD	RW	0003 FFFEh	Input buffer status flag threshold.	3.4.5.2
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register	3.10
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.12
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

3.2 Board Control Register (BCR)

Basic board functions such as initialization and autocalibration are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Read-only status flags indicate the states of specific operational functions.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. The INITIALIZE control bit remains HIGH during the initialization sequence. Initialization requires less than one millisecond for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked. (Paragraph 3.2).
- All analog input channels are active. (3.4.2).
- Analog input range is the highest available range. (3.4.3).
- Clock and trigger sources are internal. (3.4.4.3, 3.13),
- The input buffer is reset to empty. (3.4.5.1),
- Analog input data coding is offset binary. (3.5).
- The digital I/O port is configured as eight input lines. (3.8).
- Sample clocking is from the Rate-A generator; Bursting is disabled. (3.4.4).
- The board is configured as a clock and trigger initiator. (3.4.4.3).
- Burst block size is 1024 (0400h). (3.4.4.2).
- The analog input buffer is reset to empty; buffer threshold is 3FFFEh. (3.4.5).
- The Rate-A generator is adjusted to 100 kHz, and is disabled. (3.6),
- The Rate-B generator is adjusted to 4 kHz, and is disabled. (3.6),

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0022 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D07	RW	(Reserved)	0	---	---
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	3.4.4.2
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	3.4.4.2
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	3.4.5.1
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16	RW	INPUT BUFFER UNDERFLOW	0	Set HIGH if the input buffer underflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D17	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.5
D18	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator.	3.6
D19	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator.	3.6
D20	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.9
D21	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.9
D22	R/W	ANALOG INPUT WARP MODE	0	Selects the analog input warp mode **required for sample rates greater than 500KSPS.**	3.6
D23	R/W	(Reserved diagnostic control bit)	0	Production diagnostic. Always write LOW.	---
D24-D30	RW	(Reserved)	0h	---	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults. Remains HIGH during the initialization sequence.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	1 ms

3.4 Analog Inputs

Each of six analog input channels can be digitized with 18-bit resolution at rates from DC to 550 Kilosamples per second. Data from any combination of inputs can be acquired in a 256K-sample buffer, and the associated channel number is attached to each active channel data value. Two selectable input voltage ranges are available.

All active inputs are sampled simultaneously at each occurrence of the sample clock, which can be derived: (a) from an internal rate generator, (b) from an external hardware clock input, or (c) directly from the bus.

To illustrate the requirements for initiating analog input acquisition directly after board initialization, setting the following control bits HIGH simultaneously in the BCR would start a 6-channel acquisition using the Rate-A generator operating at the default sample rate:

- ENABLE INPUT BUFFER: Enables the analog input buffer.
- ENABLE RATE-A GENERATOR: Enables the Rate-A generator; Starts acquisition.

3.4.1 Input Modes

An input switching network routes either the system input signals or internal test signals through the input channels, and is controlled by the INPUT CONFIG control field in the Input Configuration register (Table 3.4-1). External system inputs are ignored while internal signals are monitored.

3.4.1.1 System Inputs

If 'External system Inputs' are selected, the signal present between the HI and LO inputs in each active channel (3.4.2) is acquired.

3.4.1.2 Test Modes

Internal analog nodes can be monitored to verify the functional integrity of the board. The selected input ranges apply in all input modes, including test modes. The following signals are present in *all input channels* when the indicated test modes are selected:

Zero Selftest:	Ideally equal to 0.0000 VDC,
VREF Selftest:	Internal voltage reference, ideally equal to +99.0000 percent of the *selected analog input range*.

The actual values obtained are subject to the accuracy limitations tabulated in the product specification.

3.4.2 Active Channels Selection

Input channels are designated as active by setting the corresponding INPUT XX control bits HIGH in the Analog Input Configuration register (Table 3.4-1), or as inactive by clearing the bits LOW. All active inputs are sampled simultaneously when a sample clock occurs. Inactive channels produce no data in the input buffer.

Table 3.4-1. Input Configuration Register

Offset: 0014h **Default: 0010 003Fh**

BIT	MODE	DESIGNATION	DEF	DEF	REF
D00	RW	INPUT 00	1	Analog input Active Channel selection mask.	3.4.2
D01	RW	INPUT 01	1	HIGH to enable.	
D02	RW	INPUT 02	1		
D03	RW	INPUT 03	1		
D04	RW	INPUT 04	1		
D05	RW	INPUT 05	1		
D06-D07	RW	(Reserved)	0h	---	---
D08-D09	RW	CLOCK SOURCE	0	Analog Input clock source: 0 => Rate-A Generator. 1 => Rate-B Generator. 2 => External Clock input 3 => (Reserved).	3.4.4
D10-D11	RW	(Reserved)	0h	---	---
D12-D13	RW	TRIGGER SOURCE	0	Analog Input trigger source: 0 => Rate-B Generator. 1 => Rate-A Generator. 2 => External Trigger input 3 => (Reserved).	3.4.4.2
D14-D15	RW	(Reserved)	0h	---	---
D16-D17	RW	INPUT CONFIG	0	Analog Input Mode: 0 => External system inputs. 1 => (Reserved). 2 => ZERO Selftest. 3 => +VREF Selftest.	3.4.1
D18-D19	RW	(Reserved)	0h	---	---
D20	RW	INPUT HIGH RANGE	1	Selects the highest available input range if HIGH, or the Low range if LOW.: High-Range Option: Low-Range Option: HIGH => ±20V ±10V. LOW => ±10V ±5V.	3.4.3
D21-D23	RW	(Reserved)	0h	---	---
D24	RW	INPUT FILTER	0	Selects the analog input filter if HIGH, or no filter if LOW:	3.4.6
D25-D31	RO	(Reserved)	0h	---	---

3.4.3 Input Ranges

If the board is factory-configured with the High-Range set, an input voltage range of ±20V or ±10V is selected by the INPUT HIGH RANGE control bit in the Input Configuration register. If configured for the LOW-Range set, the available ranges are ±10V or ±5V. The available range set is identified in the Assembly Configuration register shown in Table 3.12-1.

Note: Voltage levels outside the selected ranges will produce saturation codes of plus or minus fullscale, but will not damage the inputs if they are within the range indicated in the product specification for overvoltage protection.

3.4.4 Sampling Modes

All active channels are sampled at each occurrence of the analog input sample clock. The source of the input sampling clock is controlled by the CLOCK SOURCE control field in the Input Configuration register, and the default source is the internal Rate-A generator. A software clock can be applied at any time by setting the INPUT S/W CLOCK control bit HIGH in the BCR. This bit overrides the existing CLOCK SOURCE selection, and clears automatically.

3.4.4.1 Continuous

During continuous sampling, all active input channels are sampled continuously as long as a clock source is present and the input buffer is not full. Continuous sampling is selected when the ENABLE INPUT BURST control bit is LOW in the BCR.

3.4.4.2 Burst Sampling

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, an input trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired. Sampling then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit Input Burst Block Size control register (Table 3.1-1). The number of samples acquired in a burst *for each active channe*l equals the value contained in this register. The total number of samples acquired equals this value *times* the number of active channels.

Note: If a BURST BLOCK SIZE of zero is selected, a trigger initiates a nonterminating burst that continues as long as bursting is enabled and a sample clock is present.

The INPUT BURST BUSY status flag in the BCR is set HIGH by the initiating trigger, and is maintained HIGH throughout the burst. INPUT BURST BUSY is LOW unless a burst is in progress. *Input triggers are ignored when INPUT BURST BUSY is HIGH, of if the buffer is disabled (3.4.5.1).*

The source of the input trigger is controlled by the TRIGGER SOURCE control field in the Analog Input Configuration register, and the default source is the internal Rate-B generator. A software trigger can be applied at any time by setting the INPUT S/W TRIGGER control bit HIGH in the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically.

The END OF BURST status bit in the input buffer (3.4.5) is set HIGH for the last input value acquired in a burst.

3.4.4.3 Analog Inputs External Clock and Trigger

Selection of the External Clock Input configures the board as an ***Clock Target***, and sample clocks are supplied externally through the INP CLK INP pin in the system I/O connector. For any other clock selection, the board is designated a ***Clock Initiator***.

Selection of the External Trigger Input configures the board as an ***Trigger Target***, and burst triggers are supplied externally through the INP TRIG INP pin in the system I/O connector For any other trigger selection, the board is designated a ***Trigger Initiator***.

The INP CLK OUT and INP TRIG OUT pins in the I/O connector generate an output pulse when the corresponding internal clock or trigger occurs.

3.4.5 Input Data Buffer

3.4.5.1 Organization

Analog input data accumulates in the input data FIFO buffer until extracted through the PCI bus. The buffer has a capacity of 256K total samples, and contains an 18-bit data field, an END OF BURST status bit, and a 3-Bit INPUT CHANNEL NUMBER field (Table 3.4-2). Analog input data is right-justified to the LSB, and occupies bit positions D00 through D17.

The END OF BURST (EOB) status bit identifies the last data value in an input burst (3.4.4.2), and the INPUT CHANNEL NUMBER identifies the input channel associated with each value in the buffer.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant bit (LSB)
D01-D16	DATA01 - DATA16	Data value intermediate bits
D17	DATA17	Data value most significant bit (MSB)
D18	END OF BURST (EOB)	Identifies the last input value in a burst.
D19	(Reserved)	Returns zero.
D20-D22	INPUT CHANNEL NUMBER	Analog input channel number.
D23-D31	(Reserved)	Always zero.

NOTE: The input buffer capacity of 256K-samples is distributed among all active input channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 256K / Number of active channels.

In order for the input buffer to acquire input data, the ENABLE INPUT BUFFER control bit must be set HIGH in the BCR. The buffer can be cleared, or emptied, by writing a "one" to the CLEAR INPUT BUFFER control bit in the BCR. The CLEAR INPUT BUFFER bit clears automatically. An empty buffer returns an indeterminate value.

NOTE: To ensure that all input data is flushed from the data pipeline, a cleared buffer is held in a reset state for approximately 4 microseconds. During this interval, the CLEAR INPUT BUFFER control bit remains HIGH and the input clock is disabled.

The INPUT BUFFER OVERFLOW status bit in the BCR is set HIGH if the buffer overflows, thereby indicating data loss. Likewise, The UNDERFLOW flag is asserted if the buffer is read while empty. Either flag remains HIGH until cleared, either directly from the bus, by the CLEAR INPUT BUFFER control bit, or by a board reset.

3.4.5.2 Buffer Size and Threshold Registers

The Input Buffer Size control register listed in Table 3.1-1 contains the total number of data values present in the input buffer. The Input Buffer Threshold register (Table 3.4-3) specifies the buffer size value above which the INPUT BUFFER THRESHOLD FLAG is asserted HIGH. The threshold flag is duplicated in the BCR.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0003 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	INPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the input buffer, above which the threshold flag is asserted HIGH.
D19	RW	(Reserved)	0	---
D20	RO	INPUT BUFFER THRESHOLD FLAG [1]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D21-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

3.4.6 Input Filters

The INPUT FILTER control bit in the Input Configuration register inserts a lowpass analog input filter into all input channels if set HIGH. If INPUT FILTER is LOW, the filters are disabled and the input signals use the full bandwidth of the input channels. The characteristics of the analog input filter are described in the product specification.

3.5 Data Coding Formats

Analog input data is arranged as 18 right-justified data bits with the coding conventions shown in Figure 3.5-1. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

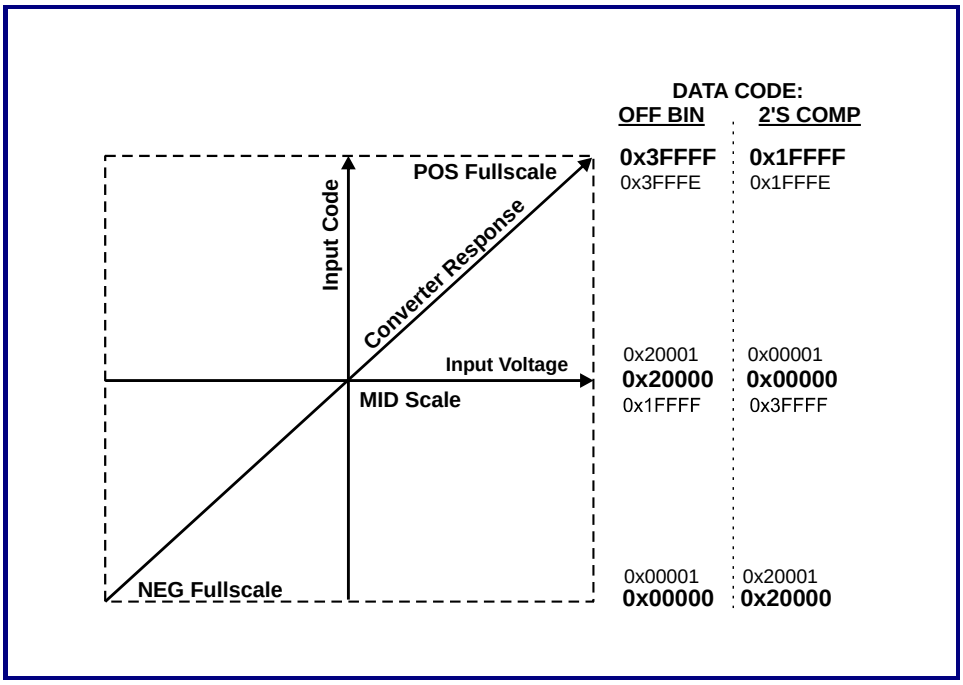

Figure 3.5-1. Analog Data Coding Formats; 18 Bit Data

3.6 Rate Generators

Two rate generators supply independent clock frequencies for ADC clocking and burst control. Rate-A Generator, shown in Table 3.6-1, generates an internal sample clock for the analog inputs, and the Rate-B generator output can be used as a trigger source for input burst acquisition. The roles of these rate generators can be reversed through the CLOCK SOURCE and TRIGGER SOURCE control fields in the Input Configuration register.

Each generator is enabled by setting the associated ENABLE RATE-A/B GENERATOR control bit HIGH in the BCR. The generators are disabled when these bits are LOW.

Table 3.6-1. Rate Generator Registers (Rate-A,B)

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 01C2 (Rate-A), 0000 2BF2h (Rate-B)**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

The frequency **Fgen** (Table 3.6-2) of each generator is calculated as:

Fgen = Fclk / Ndiv,

where **Fclk** is the master clock frequency for the board, and **Ndiv** is the value written to the Rate-A/B Generator register. **Fgen** and **Fclk** are both expressed in the same frequency units. **Fclk** is assumed here to be 45.000MHz, but custom frequencies are available. If the master clock is provided with a custom frequency, **Fclk** equals the custom frequency. For an external clock or trigger input frequency, **Fclk** equals the external frequency, *Exceeding the maximum sampling rate listed in the product specification by more than 2 percent may result in dropped samples.*

Table 3.6-2. Rate Generator Frequency Selection Example

Ndiv		FREQUENCY Fgen (45.000 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
81	0051	555,556
82	0052	548,780
83	0053	542,169
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv **

* ±0.005 percent. ** Fclk = master clock frequency; e.g.: 45.000MHz.

NOTE: For analog input sampling rates greater than 500KSPS, the ANALOG INPUT WARP MODE control bit must be set HIGH in the BCR. When operating in warp mode, the minimum sample rate is 1 KSPS, and the first sample acquired from all active channels after a lapse of 1 millisecond or longer should be discarded.

3.7 Multiboard Synchronization

Analog input clocking and triggering can be synchronized among multiple boards by designating one of the boards as an ***initiator***, and the remaining boards as ***targets*** (3.4.4.3). In order to implement this function, the boards must be interconnected as described in Paragraph 2.3.2.

When multiple boards are configured as an initiator with multiple targets, the analog input clock and the analog input trigger generated in the initiator board are duplicated in the target boards with delays of less than 100 nanoseconds.

The board defaults to the analog input initiator mode.

3.8 Digital I/O Port

The digital I/O port consists of eight bidirectional TTL I/O lines, with the corresponding data bits shown in Table 3.8-1. The DIO lines are arranged as two 4-bit nibbles, with the direction of each nibble controlled independently of the other. A nibble is an input to the board if the associated DIO 00 03 OUTPUT control bit is LOW, or is an output if the bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the register. All digital I/O lines default to inputs.

Table 3.8-1. Digital I/O Port Register

Offset: 0004h **Default: 000X 000Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

3.9 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Initial stabilization after power is applied,
- PCI bus reset,
- Analog input range change (3.4.3),
- Selection or deselection of the input filters (3.4.6).

Analog inputs are autocalibrated on the currently selected range.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the completion of autocalibration. Autocalibration can be invoked at any time, and has a typical duration of **4 seconds** for a 6-channel board when operating with the input filters disabled (3.4.6). Selecting the input filters extends the autocal duration to approximately **7 seconds** in order to provide the required increased settling times. Two-channel and four-channel boards have proportionately shorter autocalibration durations.

Completion of autocalibration can be detected either by monitoring the "Autocal completed" status flag in the Primary Status register (Table 3.11-1), or by simply waiting for a time interval sufficient to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

Autocalibration correction values are stored in volatile RAM and are retained throughout a software initialization (3.3.2), but are discarded if the system is reset or powered down

3.10 Primary Status Register

Critical status flags are consolidated into a single Primary Status register (Table 3.10-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit, *or by clearing the associated selection bit*.

NOTE: Response status bits can *only* be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The response bit for an event indicated as 'edge-detected' is set HIGH when that event transitions from false to true, and remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

Real-time access to an edge-detected signal is available by reading the source of the edge-driven response bit (e.g.: INPUT BURST BUSY in the BCR is the signal that drives the "Analog Input Burst Initiated/Completed" response bits in the PSR).

Table 3.10-1 Primary Status Register

Offset 0x0030 **Default 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed	D16	3.9
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18	
D03	Input Buffer Overflow or Underflow	D19	3.4.5.1
D04	Analog Input Burst Initiated (BURST BUSY LO-HI)	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO)	D21	
D06	Analog input clock	D22	3.4.4
D07	Digital I/O Port DIO 00 LOW-to-HIGH transition	D23	3.8
D08-D15	(Reserved)	D24-D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Level-detected event. All other events are Edge-detected.

3.11 Buffer DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master, in either DMA Channel 00 or Channel 01. Set bit D[02] in the PCI Command register HIGH to select the bus mastering mode. Also, clear D[15] LOW in the PCI-9056 DMA Mode register to select *slow-terminate* operation. Refer to the PCI-9056 reference manual for a detailed description of DMA configuration registers.

3.11.1 Block Mode

Table 3.11-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.11-1. Typical DMA Registers; Block Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	(Note 2)
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

3.11.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.11-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.11-2. Typical DMA Registers; Demand Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0018h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

When operating in demand mode, DMA data transfer from the input buffer is requested continuously by the local controller as long as the buffer contains data.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained in the buffer until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

3.12 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.16-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.12-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved for firmware revision extension)
D16-D17	Number of analog input channels: 0 => 2 Input channels. 1 => 4 input channels. 2 => 6 input channels. 3 => (Reserved)
D18-D19	Analog Input filter frequency: 0 => Filter Type-F1: 200kHz Chebyshev, 5th Order, 0.5dB. 1 => Filter Type-F2: 100kHz Chebyshev, 5th Order, 0.5dB 2 => (Reserved) 3 => (Reserved)
D20-D21	Master Clock frequency: 0 => 45.000 MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D22-D23	Input Range Set: 0 => High-Range set: ±20V (40Vp-p), ±10V. 1 => Low-Range set: ±10V (20Vp-p), ±5V 2 => (Reserved) 3 => (Reserved)
D24-D31	(Reserved bit field; returns all-zero).

3.13 Auxiliary External Clock and Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking and burst triggering to external events. These bidirectional TTL connections are available as AUX CLOCK I/O and AUX SYNC I/O (Table 2.2-2), and when active *as inputs*, replace the corresponding external INP CLK INP/OUT and INP TRIG INP/OUT signals in the system I/O connector. The AUX I/O signals are accessible through a 6-Pin connector on the back (Side-2) of the board.

AUX clock and sync signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.13-1. When an AUX signal is designated as an ***input***, the signal replaces the corresponding CLOCK I/O or SYNC IO input from the system connector. In order for the input to be acknowledged, ***target mode*** *(i.e.: external input)* must be selected in the corresponding clock or trigger source control field in the Input Configuration register (Table 3.4-1). The AUX I/O pins are pulled up internally to +5VDC through 33K.

Active AUX ***outputs*** produce an output pulse for each internal ADC sample clock or burst trigger, and are active in both target and initiator clock and sync modes.

AUX *inputs* are edge-detected as LOW-to-HIGH transitions if the INVERT INPUTS control bit is LOW, or as HIGH-to-LOW transitions if the bit is HIGH. Minimum HIGH and LOW level durations are typically 100ns if the NOISE SUPPRESSION control bit is LOW, or 1.5us if the bit is HIGH. AUX *output pulses* are positive (i.e.: baseline level is LOW) if the INVERT OUTPUTS control bit is LOW, or negative (baseline HIGH) if the control bit is HIGH. Output pulse width is typically 130ns if the NOISE SUPPRESSION control bit is LOW, or 2.0us if the bit is HIGH.

To increase the reliability of external triggering in high-noise environments, selectable noise suppression increases the debounce or detection interval for active inputs, and increases the pulse width of active outputs.

Table 3.13-1. Auxiliary Sync I/O Control

Offset: 0000 0010h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 400ns, and output pulse width is 800ns.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as the AUX CLOCK I/O control mode.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of six analog input channels contains a selftest input switching network, a differential amplifier, a scaling network, a selectable filter, and an 18-Bit ADC (Figure 4.1-1). Input ranges are software-selectable as ±20V or ±10V for a High-Range option, or as ±10V or ±5V for a Low-Range option. A 256K-sample FIFO buffer accumulates analog input data for subsequent retrieval through the PCI bus.

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller, and supports universal signaling. +5 VDC power from the PCI bus is converted into regulated power voltages for the internal analog networks.

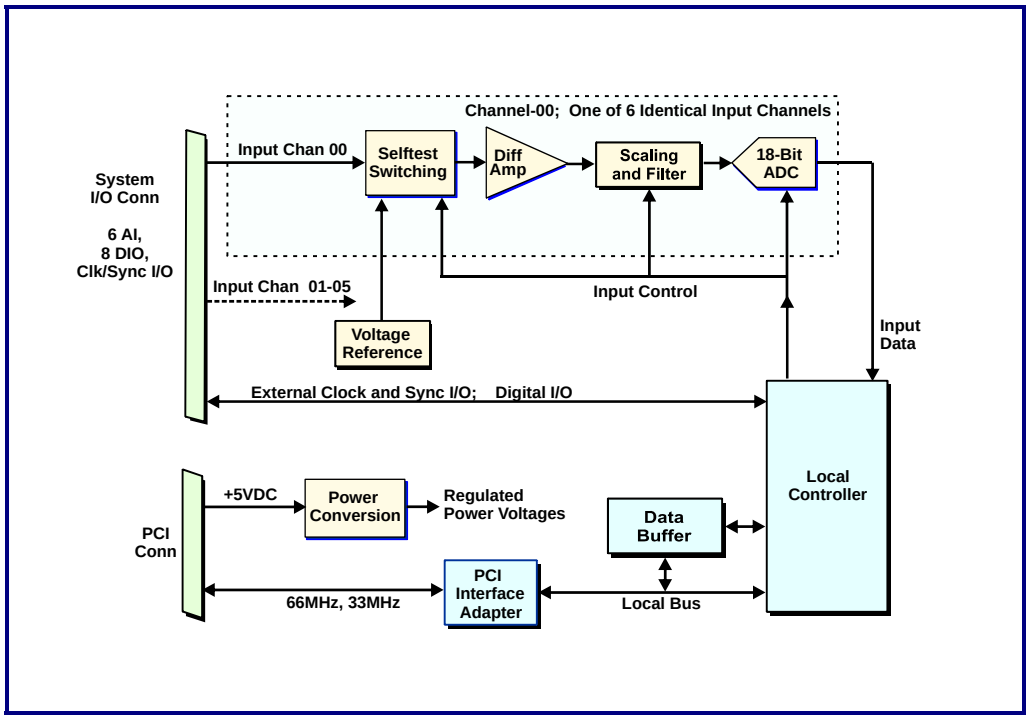

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input channels. Analog input sampling on multiple target boards can be synchronized to a single software-designated initiator board.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, six 18-bit successive-approximation ADC's receive differential system analog input signals from the system I/O connector. For integrity testing and autocalibration operations, internal voltage references can be routed through the selftest switches to the ADC's.

A 5th-order lowpass analog filter can be inserted into the input channels, to provide a degree of antialiasing for out-of-band signal components. Byte-serial data from each ADC is multiplexed into a continuous data stream within the local controller. The final formatted data is loaded into the analog input data buffer.

ADC clocking can be supplied either from an internal 24-Bit rate divider operating from the master clock, or from an external TTL source. Triggered bursts can be acquired by using a second internal rate generator or an external input as a trigger source. The burst block-size can be controlled by a 24-Bit counter, or sampling can be configured to operate continuously after a trigger.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to internal voltage references. The utility can be invoked at any time by the control software.

The internal voltage references are used to calibrate the span of each input channel, and a zero-reference is used to calibrate the offset value. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.4 Power Control

Regulated power voltages of +5 VDC, ±12V and ±14 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	0022 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	000X 000Xh	Digital I/O port data.	3.8
0008	(Reserved)	RO	0000 0000h	---	---
000C	(Reserved)	RO	0000 0000h	---	---
0010	AUXILIARY SYNC IO	RW	0000 0000h	Auxiliary external clock and trigger I/O.	3.13
0014	INPUT CONFIGURATION	RW	0010 003Fh	Analog input configuration.	3.4
0018	INPUT DATA BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0000 01C2h	Rate-A generator divider; 24 bits.	3.6
0020	RATE GENERATOR B	RW	0000 2BF2h	Rate-B generator divider; 24 bits.	3.6
0024	INPUT BURST BLOCK SIZE	RW	0000 0400h	Analog input burst size.	3.4.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h`	Number of data values in the input buffer.	3.4.5.2
002C	INPUT BUFFER THRESHOLD	RW	0003 FFFEh	Input buffer status flag threshold.	3.4.5.2
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register	3.10
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.12
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0022 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D07	RW	(Reserved)	0	---	---
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	3.4.4.2
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	3.4.4.2
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	3.4.5.1
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16	RW	INPUT BUFFER UNDERFLOW	0	Set HIGH if the input buffer underflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D17	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.5
D18	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator.	3.6
D19	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator.	3.6
D20	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.9
D21	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.9
D22	R/W	ANALOG INPUT WARP MODE	0	Selects the analog input warp mode **required for sample rates greater than 500KSPS.**	3.6
D23	R/W	(Reserved diagnostic control bit)	0	Production diagnostic. Always write LOW.	---
D24-D30	RW	(Reserved)	0h	---	---
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults. Remains HIGH during the initialization sequence.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	1 ms

Table 3.4-1. Input Configuration Register

Offset: 0014h **Default: 0010 003Fh**

BIT	MODE	DESIGNATION	DEF	DEF	REF
D00	RW	INPUT 00	1	Analog input Active Channel selection mask.	3.4.2
D01	RW	INPUT 01	1	HIGH to enable.	
D02	RW	INPUT 02	1		
D03	RW	INPUT 03	1		
D04	RW	INPUT 04	1		
D05	RW	INPUT 05	1		
D06-D07	RW	(Reserved)	0h	---	---
D08-D09	RW	CLOCK SOURCE	0	Analog Input clock source: 0 => Rate-A Generator. 1 => Rate-B Generator. 2 => External Clock input 3 => (Reserved).	3.4.4
D10-D11	RW	(Reserved)	0h	---	---
D12-D13	RW	TRIGGER SOURCE	0	Analog Input trigger source: 0 => Rate-B Generator. 1 => Rate-A Generator. 2 => External Trigger input 3 => (Reserved).	3.4.4.2
D14-D15	RW	(Reserved)	0h	---	---
D16-D17	RW	INPUT CONFIG	0	Analog Input Mode: 0 => External system inputs. 1 => (Reserved). 2 => ZERO Selftest. 3 => +VREF Selftest.	3.4.1
D18-D19	RW	(Reserved)	0h	---	---
D20	RW	INPUT HIGH RANGE	1	Selects the highest available input range if HIGH, or the Low range if LOW.: High-Range Option: Low-Range Option: HIGH => ±20V ±10V. LOW => ±10V ±5V.	3.4.3
D21-D23	RW	(Reserved)	0h	---	---
D24	RW	INPUT FILTER	0	Selects the analog input filter if HIGH, or no filter if LOW:	3.4.6
D25-D31	RO	(Reserved)	0h	---	---

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant bit (LSB)
D01-D16	DATA01 - DATA16	Data value intermediate bits
D17	DATA17	Data value most significant bit (MSB)
D18	END OF BURST (EOB)	Identifies the last input value in a burst.
D19	(Reserved)	Returns zero.
D20-D22	INPUT CHANNEL NUMBER	Analog input channel number.
D23-D31	(Reserved)	Always zero.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0007 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RW	INPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the input buffer, above which the threshold flag is asserted HIGH.
D19	RW	(Reserved)	0	---
D20	RO	INPUT BUFFER THRESHOLD FLAG [1]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D21-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

Table 3.6-1. Rate Generator Registers (Rate-A,B)

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 01C2 (Rate-A), 0000 2BF2h (Rate-B)**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

Table 3.6-2. Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (45.000 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
81	0051	555,556
82	0052	548,780
83	0053	542,169
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv **

* ±0.005 percent. ** Fclk = master clock frequency; e.g.: 45.000MHz.

Table 3.8-1. Digital I/O Port Register

Offset: 0004h **Default: 000X 000Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.10-1 Primary Status Register

Offset 0x0030 **Default 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed	D16	3.9
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18	
D03	Input Buffer Overflow or Underflow	D19	3.4.5.1
D04	Analog Input Burst Initiated (BURST BUSY LO-HI)	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO)	D21	
D06	Analog input clock	D22	3.4.4
D07	Digital I/O Port DIO 00 LOW-to-HIGH transition	D23	3.8
D08-D15	(Reserved)	D24-D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Level-detected event. All other events are Edge-detected.

Table 3.11-1. Typical DMA Registers; Block Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	(Note 2)
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

Table 3.11-2. Typical DMA Registers; Demand Mode

PCI Offset [1]	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	(Note 2)
88h	DMA Local Address	Initial (constant) local address	0000 0018h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

[1] From the PCI base address for Memory or I/O access to DMA registers. [2] Determined by specific transfer requirements.

Table 3.12-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved for firmware revision extension)
D16-D17	Number of analog input channels: 0 => 2 Input channels. 1 => 4 input channels. 2 => 6 input channels. 3 => (Reserved)
D18-D19	Analog Input filter frequency: 0 => Filter Type-F1: 200kHz Chebyshev, 5th Order, 0.5dB. 1 => Filter Type-F2: 100kHz Chebyshev, 5th Order, 0.5dB. 2 => (Reserved) 3 => (Reserved)
D20-D21	Master Clock frequency: 0 => 45.000 MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D22-D23	Input Range Set: 0 => High-Range set: ±20V (40Vp-p), ±10V. 1 => Low-Range set: ±10V (20Vp-p), ±5V 2 => (Reserved) 3 => (Reserved)
D24-D31	(Reserved bit field; returns all-zero).

Table 3.13-1. Auxiliary Sync I/O Control

Offset: 0000 0010h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 400ns, and output pulse width is 800ns.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as the AUX CLOCK I/O control mode.

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APPENDIX B

COMPARISON of PMC66-18AISS6C and PMC66-16AISS16AO2

Appendix B

Comparison of PMC66-18AISS6C and PMC66-16AISS16AO2

Operation of the PMC66-18AISS6C is similar to that of the PMC66-16AISS16AO2. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a comprehensive list of requirements.

B.1. Comparison of Features

Table B.1 compares principal PMC66-18AISS6C and PMC66-16AISS16AO2 features. Significant differences are shown in bold type.

Table B.1. PMC66-16AISS16AO2, PMC66-18AISS6C Comparison

Feature	PMC66-16AISS16AO2	PMC66-18AISS6C
Input Channels	**Sixteen 16-Bit ADC's; SAR**	**Six 18-Bit ADC's; SAR**
Input Sample Rates	**Zero to 1.0MSPS/Chan**	**Zero to 550KSPS/Chan**
Selectable Input Ranges	**±10V, ±5V, ±2.5V**	**±20V, ±10V; or optionally ±10V, ±5V**
Lowpass Filter	**Single-pole R-C**	**5th Order Chebyshev, 0.5dB**
Rate Generators	**Three, with 24-Bit dividers**	**Two, with 24-Bit dividers**
Data Buffer DMA	**Block mode**	**Block mode and Demand mode**
Output Channels	**Two 16-Bit DAC channels**	**None**
Digital I/O Port	**6-Bit Bidirectional TTL; Bit-oriented.**	**8-Bit Bidirectional TTL; Nibble-oriented.**
Auxiliary Sync I/O	**No**	**Yes**
Input Buffer	256K-Sample FIFO	256K-Sample FIFO
PCI Adapter	PCI-9056 (66MHz PCI)	PCI-9056 (66MHz PCI)
Interrupt	Primary status register	Primary status register
PCI Interface	PCI 2.3; 33MHz/66MHz	PCI 2.3; 33MHz/66MHz
Local Clock	40-45 MHz	45-48 MHz

B.2. Migration from PMC66-16AISS16AO2:

Para 2.2.2. Input/Output Cable Connections:

- The system I/O connector has changed from 80 pins to 68 pins.

Para 2.3. System Configurations:

- Analog inputs are differential only.
- Analog outputs have been deleted.
- Two reference adjustments are now required for calibration.

Table 3.1-1. Control and Data Registers:

- Control registers "Analog Output Chan 00" and "Analog Output Chan 01" have been deleted.
- Control register "Active Input Channels" has been replaced with new register "Analog Input Config."

Table 3.2-1. Board Control Register (BCR):

- "Analog Input Mode" and "Input Range" fields have moved to the new "Analog Input Configuration" register.

Table 3.4-1. Analog Input Configuration Register:

- New register contains the "Active Input Channels" mask, as well as "High Range", "Clock Source", "Trigger Source", "Input Config" and "Input Filter" control fields.

Table 3.4-2. Input Data Buffer:

- Control field "Input Channel Number" replaces "First-Channel Tag."

Table 3.4-3. Input Buffer Threshold Register:

- Control field "Input Buffer Threshold" has been extended to 19 bits.

Table 3.6-1. Rate Generator Registers (A,B):

- Renamed table, which now combines all rate control registers.

Table 3.8-1. Digital I/O Port Register:

- The original 6-Bit DIO port has been replaced with an 8-bit port.

Paragraph 3.9. Autocalibration:

- A synchronous sampling option has been added for autocalibration.

Table 3.12-1. Assembly Configuration Register:

- Options have been modified per new configuration requirements.

Paragraph 3.13. Auxiliary External Clock and Sync I/O:

- New section, describing auxiliary clock/sync I/O.

****

Original Sections 3.12 through 3.15 referring to analog outputs have been deleted.

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Revision History:

03-25-2010: Origination. Preliminary draft.

06-05-2011: Table 3.2-1: Revised Warp-mode threshold sample rate from 400ksps to 500ksps..

11-29-2011: Table 3.12-1: Added filter option F2.

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