General Standards Corporation
High Performance Bus Interface Solutions

PC104P-16AIO168

16-BIT ANALOG INPUT/OUTPUT PC/104-PLUS BOARD
WITH 16 INPUT CHANNELS AND 8 OUTPUT CHANNELS
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REFERENCE MANUAL

PC104P-16AIO168

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PC104P-16AIO168 board is a standard PC/104-Plus module that provides high-speed 16-bit analog input/output capability. 16 analog input lines can be configured either as 16 single-ended input channels or as eight differential channels, and are digitized at rates up to 300,000 conversions per second. Eight single-ended analog outputs can be clocked at up to 300KSPS per channel. The voltage range for analog inputs and outputs is software controlled as ±2.5V, ±5V or ±10V. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and the PC/104-Plus Specification, Version 1.1. A PCI interface adapter supports the "plug-n-play" initialization concept.

Power requirements consist of +5 VDC from the PCI bus in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PC104P-16AIO168 product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.
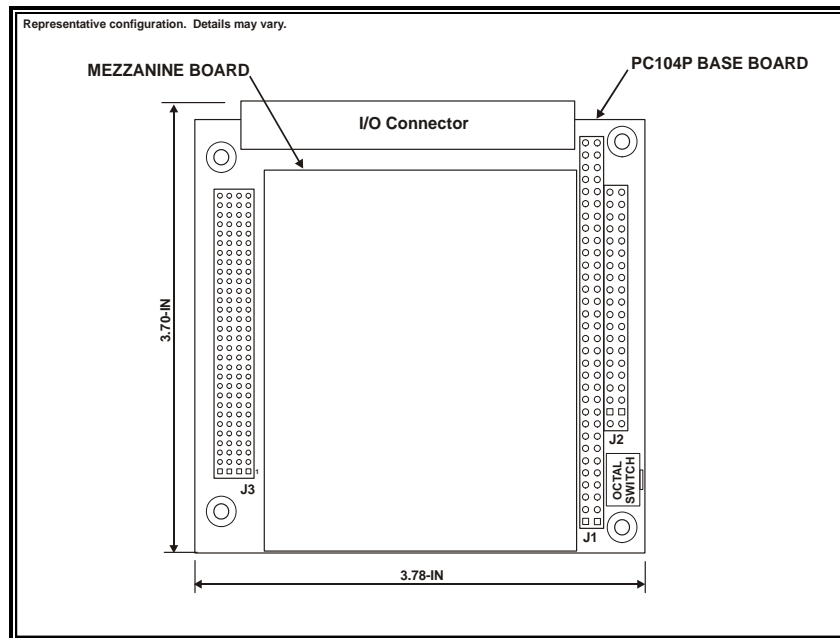
Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 50-pin I/O connector. The analog outputs are set to zero-level (midrange) during initialization.

1.2 Functional Overview

Principal capabilities of the PC104P-16AIO168 board are summarized in the following list of features:

❑ 16 Single-Ended or 8 Differential 16-Bit Scanned Analog Input Channels
❑ Eight Analog Output Channels, 16-Bit D/A Converter per Channel
❑ Software-Selectable Analog Input/Output Ranges of ±10V, ±5V or ±2.5V
❑ Independent 32K-Sample Analog Input and Output FIFO Buffers
❑ 300K Samples per Second Aggregate Analog Input Sample Rate
❑ Multiple-Channel and Single-Channel Input Scanning Modes
❑ 300K Samples per Second per Channel Analog Output Clocking Rate
❑ Supports Waveform and Arbitrary Function Generation
❑ Continuous and One-shot Output Modes
❑ Two Independent Internal Rate Generators
❑ Four Auxiliary Digital Output Lines
❑ Supports Multiboard Synchronization of Analog Inputs and Outputs
❑ Internal Autocalibration of Analog Input and Output Channels
❑ DMA Engine Minimizes Host I/O Overhead

The PC104P-16AIO168 board contains eight 16-Bit D/A converters and a 16-bit scanning A/D converter. A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller (Figure 1.2-1). Gain and offset correction of the analog input and output channels is performed by calibration DAC's that are loaded with channel correction values during autocalibration
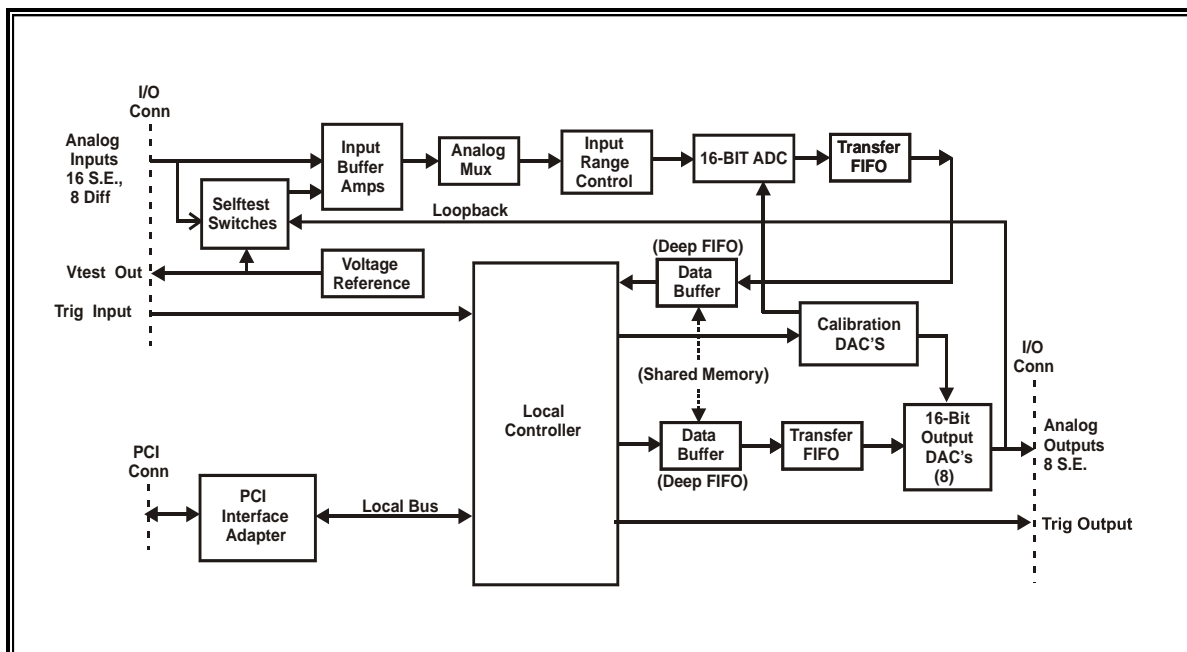
Figure 1.2-1. Functional Organization

The analog inputs are software-configurable either as 16 single-ended channels or as eight differential signal pairs. Buffer amplifiers on all input lines eliminate multiplexer input switching noise, and minimize crosstalk and input bias currents. A selftest switching network routes a precision reference to the A/D converter during autocalibration, and also provides loopback monitoring of all analog output channels. Analog input data accumulates in a 32K-sample buffer until retrieved by the PCI bus.

Each of the eight analog output channels contains a dedicated 16-bit D/A converter, offset and gain calibration DAC's, and an output range control network. The board receives analog output data from the PCI bus through a 32K-sample FIFO buffer.

Analog input scanning can be synchronized to the analog output sample clock, or the inputs and outputs can be operated independently. Both the analog inputs and outputs can be synchronized externally, and a hardware output permits multiple boards to be synchronized together. An interrupt request can be generated in response to selected conditions, including the status of the analog input and output data buffers.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the module should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

    CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the module from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the module from the antistatic shipping container, align the PCI and ISA connector pins with the corresponding receptacles on either the host board if the module is the first module in the stack, or on the preceding module in the stack. Press the module carefully but firmly downward into position, and verify that the PCI and ISA connectors have mated completely and that the spacers are seated against the host or preceding module.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The system input/output connector is designed to mate with a standard 0.1x0.1-inch 50-pin connector, Amp type 1-746288-0 or equivalent, with strain-relief 499252-4. The insulation displacement (IDC) AMP cable connector accepts standard 0.050-inch ribbon cable, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. "Twist and flat" cable is recommended for long cables (greater than five feet). Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connector Pin Functions

PIN	FUNCTION (Differential analog Inputs)	FUNCTION (Single-ended Analog Inputs)	PIN	FUNCTION
1	INPUT RTN	INPUT RTN	26	ANA OUT 02
2	INPUT RTN	INPUT RTN	27	ANA OUT 01
3	ANA INP 00 HI	ANA INP 00	28	ANA OUT 00
4	ANA INP 00 LO	ANA INP 01	29	OUTPUT RTN
5	ANA INP 02 HI	ANA INP 02	30	OUTPUT RTN
6	ANA INP 02 LO	ANA INP 03	31	VTEST
7	ANA INP 04 HI	ANA INP 04	32	DIFF TRIG IN LO
8	ANA INP 04 LO	ANA INP 05	33	VTEST RETURN
9	ANA INP 06 HI	ANA INP 06	34	DIFF TRIG IN HI
10	ANA INP 06 LO	ANA INP 07	35	INPUT RTN
11	ANA INP 08 HI	ANA INP 08	36	INPUT RTN
12	ANA INP 08 LO	ANA INP 09	37	INPUT RTN
13	ANA INP 10 HI	ANA INP 10	38	DIFF TRIG OUT HI
14	ANA INP 10 LO	ANA INP 11	39	TTL TRIG OUT
15	ANA INP 12 HI	ANA INP 12	40	DIFF TRIG OUT LO
16	ANA INP 12 LO	ANA INP 13	41	OUTPUT RTN
17	ANA INP 14 HI	ANA INP 14	42	DIG OUT 00
18	ANA INP 14 LO	ANA INP 15	43	TTL TRIG IN
19	INPUT RTN	INPUT RTN	44	DIG OUT 01
20	INPUT RTN	INPUT RTN	45	OUTPUT RTN
21	ANA OUT 07	ANA OUT 07	46	DIG OUT 02
22	ANA OUT 06	ANA OUT 06	47	OUTPUT RTN
23	ANA OUT 05	ANA OUT 05	48	DIG OUT 03
24	ANA OUT 04	ANA OUT 04	49	OUTPUT RTN
25	ANA OUT 03	ANA OUT 03	50	DIGITAL RTN
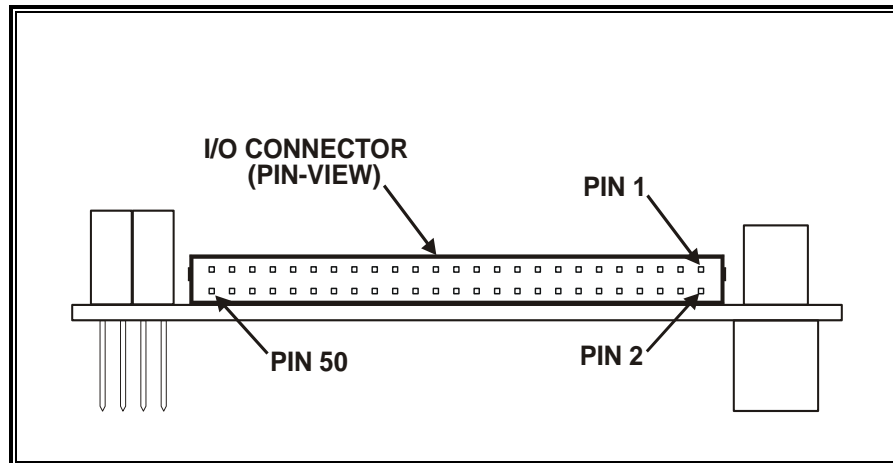
Figure 2.2-1. Input/Output Connector

2.3 System Configuration

2.3.1 Analog Inputs

2.3.1.1 Single-Ended Inputs

Analog inputs can be configured either as 16 single-ended channels or as eight differential channels. The hardware input configuration must be acknowledged by the control software, which configures the controller for either single-ended or differential operation. Pull-down resistors are provided on all analog inputs. Table 2.2-1 provides separate pin assignment columns for differential and single-ended input configurations.

Single-ended operation (Figure 2.3-1a) offers the maximum number of input channels, but generally provides optimum performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or may generate excessive ground current and damage the board.

a. **Single-ended Analog Input**

b. **Differential Analog Input**
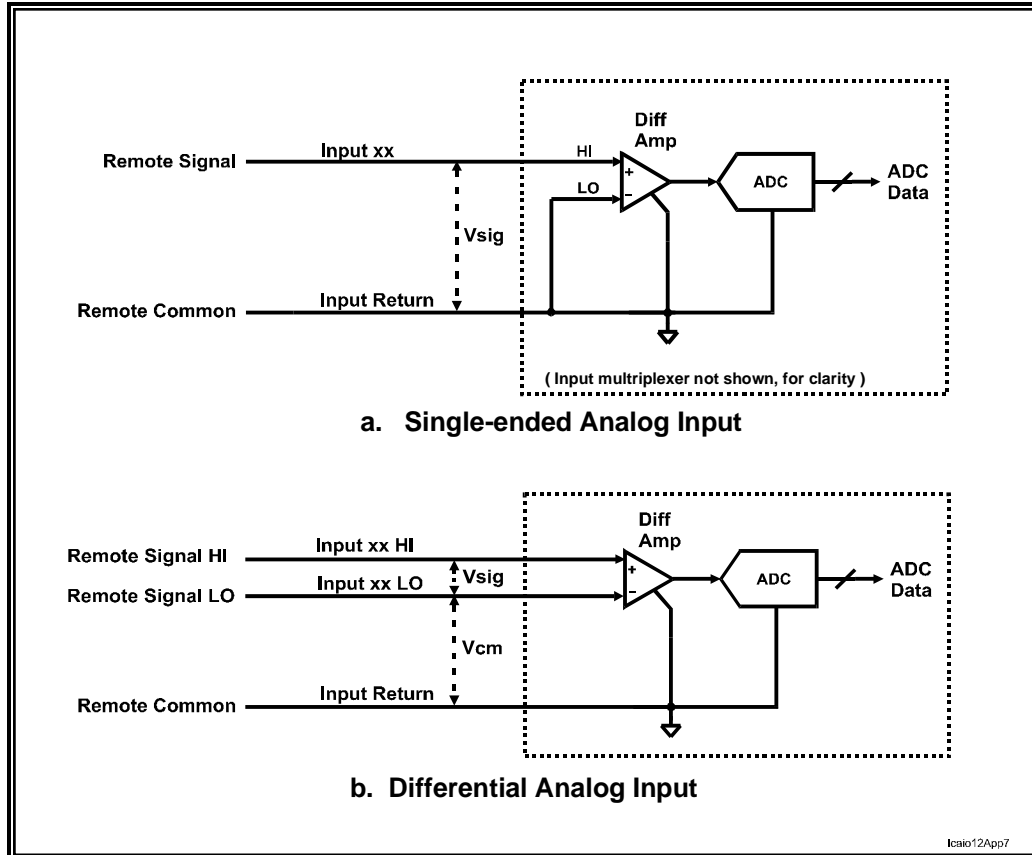
Figure 2.3-1. Analog Input Configurations

2.3.1.2 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other and have returns that are at significantly different potentials.   A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

This operating mode also offers the highest rejection of the common mode noise that is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode, shown in Figure 2.3-1b, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1)   is connected to a ground point that will ensure that the common mode voltage of all signals remains within the range specified for the board, and that will not produce potentially destructive ground currents.

2.3.2 Analog Outputs

2.3.2.1 Output Configuration

The eight analog output channels are single-ended and have a common signal return that is referred to in Table 2.2-1 as OUTPUT RTN. In general, single-ended outputs should drive only loads that are isolated from, or have a high impedance to, system ground. The best results are obtained when the loads also are isolated from each other.

Figure 2.3-2 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2.3.1-2a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads with a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

If the load return is connected to a remote system ground (Figure 2.3-2b), the potential difference V_{gnd} between the system ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current I_{gnd} developed in the return line is limited essentially only by R_{gnd}, and may damage the cable or the board if not controlled.
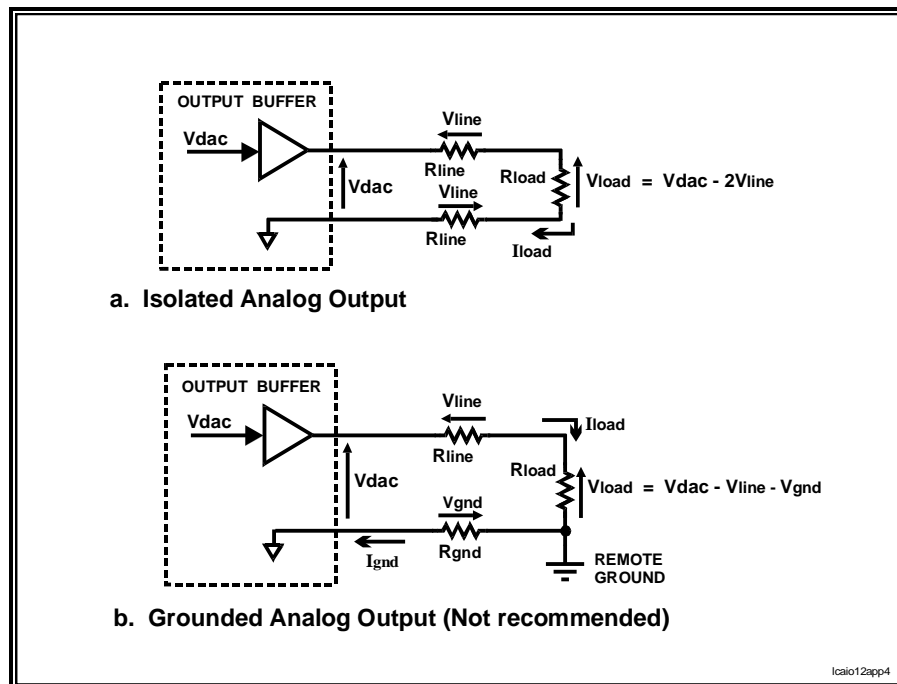
Figure 2.3-2. Output Configurations

2.3.2.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate loads.   Figure 2.3-3 shows the effect of load current on the voltage drop in copper wire of various sizes.   A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line also is considered.   Several feet of

ribbon cable therefore can produce unacceptable errors with high load current, especially in a 16-bit system, in which 1 LSB may represent only 76 microvolts (±2.5 Volt range). High impedance loads however, generally do not produce significant DC line loss errors.
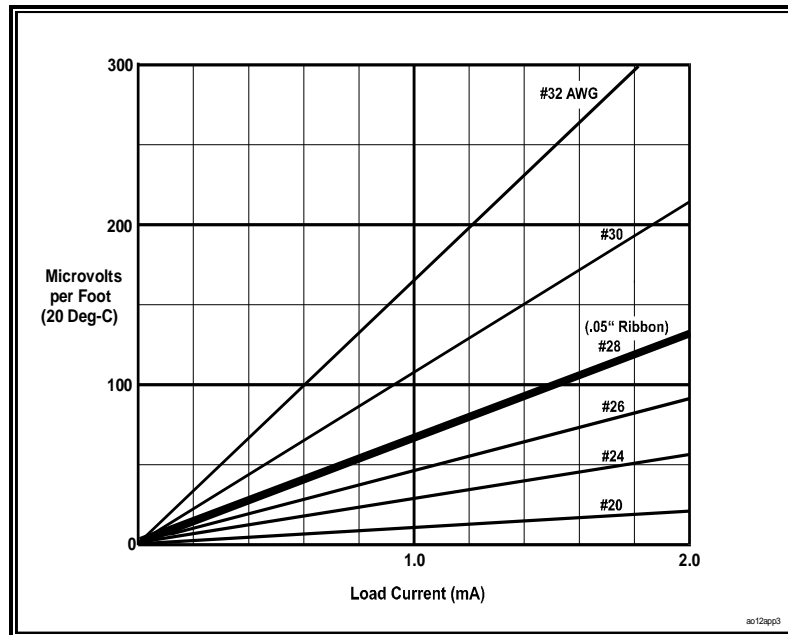
Figure 2.3-3. Line Loss versus Load Current

2.3.3 External Triggering

The TTL TRIG IN pin provides a TTL input that can be used to control the timing of the analog inputs or outputs. This input is asserted LOW, and is pulled HIGH internally through a 4.7 KOhm resistor that is connected to +5 Volts. The TRIG OUT signal is a TTL level that is available for synchronizing the operation of multiple target boards to a single initiator board.   Like the TRIG IN line, the TRIG OUT signal is asserted LOW. Loading of TRIG OUT should be limited to 15 milliamps or less.

The DIFF TRIG IN HI/LO and DIFF TRIG OUT HI/LO pins provide control functions identical to those of TTL TRIG IN and TTL TRIG OUT, but implement differential LVDS logic levels.

Unused trigger inputs should be shorted to digital return.

Note: Triggered analog output bursting is specified as an ordering option.

2.3.4 Multiboard Synchronization

If multiple boards are to be synchronized together, the TRIG OUT signal from one board, the *initiator*, is connected to TRIG IN at the first of a group *target* boards (Figure 2.3-4). The target boards are daisy chained together, with TRIG OUT from each target connected to TRIG IN of the next board in the chain. TRIG OUT from the last board in the chain is left disconnected.   The controlling software determines specific synchronization functions, which may affect analog inputs, analog outputs, or both inputs and outputs.
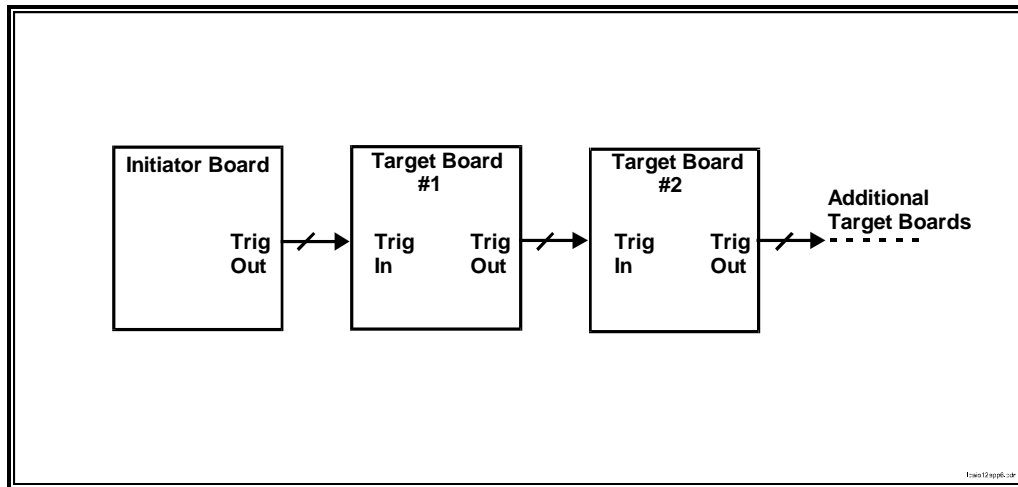
Figure 2.3-4. Multiboard Synchronization

NOTE: The terms "sync" and "trigger" are used interchangeably in this text.

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that is suspected to be defective should be returned to the factory for detailed problem analysis and repair.

2.5   Reference Verification

All analog input and output channels are software-calibrated to a single internal voltage reference by an embedded autocalibration software utility.   The procedure presented here describes the verification and adjustment of the internal reference.   For applications in which the system must not be interrupted or powered down, verification can be performed while the board is installed on the existing host board, without interrupting system operation.

To eliminate the requirement for a special test connector, the two test points required for monitoring the reference, VTEST and VTEST RTN, can be made available at a system breakout connector or test panel.   This arrangement also eliminates the necessity of disconnecting the system input/output cable for reference verification.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with PC104-*Plus* site	---	---
System interface cable (Section 2.2.2)	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the single reference voltage that ensures conformance to the product specification.   Adjustment of the internal reference, if necessary, is performed with an internal trimpot that is accessible from the side of the module.

This procedure assumes that the board is installed on a host board, and that the host is installed in an operating system.   The board can be operating in any mode while the adjustment is performed.

1. Connect the digital multimeter between the VTEST (+) and VTEST RTN (-) pins in the system I/O connector. Refer to Table 2.2-1 for pin assignments.

2. If power has been removed from the board, apply power now. Wait at least 15 minutes after power is applied before proceeding..

3. Verify that the digital multimeter indication is +9.6150 VDC ±0.0009 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer until the digital multimeter indication is within the specified range.

4. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PC104P-16AIO168 board is compatible with the PCI Local Bus specification, and supports auto configuration at the time of power-up. The PCI interface is controlled by a PLX^{TM} PCI-9080 PCI adapter. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space. After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer and to the analog output data buffer.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	ACTIVE BITS	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	16	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	12	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	17	---	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	17	000X 7FFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	17	0001 09C4h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	17	0000 0064h	Rate-B generator freq selection
0018	OUTPUT DATA BUFFER	WO	21	---	Analog output data buffer
001C	OUTPUT BUFFER CONTROL	R/W	17	000X 7FFEh	Output buffer threshold and control
0020	SCAN AND SYNC CONTROL	R/W	17	0000 02D1h	Channels per scan; Clocking and Sync sources.
0024	DIGITAL OUTPUT CONTROL	R/W	4	0000 0000h	Digital output control register
0028	FIRMWARE REVISION *	---	---	---	---
002C	AUTOCAL VALUES *	---	---	---	---
0030-3F	(Reserved)	---	---	---	Inactive

R/W = Read/Write, RO = Read-Only, WO = Write-Only.   * Maintenance register; shown for reference only.

3.2 Board Control Register (BCR)

As Table 3.2-1 indicates, the BCR consists of 16 control bits and status flags. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h   Default: 0000 4060h

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D03	R/W	AIM0	0	Analog input mode. Selects input configuration or selftest mode. Defaults to differential input mode
D04	R/W	RANGE0	0	Analog input/output range. Defaults to ±10V range.
D05	R/W	RANGE1	1	
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.
D07	R/W	(Reserved)	0	---
D08	R/W	SIMULTANEOUS OUTPUTS	0	Selects simultaneous or channel-sequential output mode. Defaults LOW to channel-sequential output mode.
D09	R/W	ENABLE OUTPUT BURST	0	Enables output bursting (one-shot) mode when HIGH.
D10	R/W	ENABLE OUTPUT LOOPING	0	Enables output function looping when HIGH.
D11	R/W	*OUTPUT SYNC	0	Initiates a single output burst, when enabled by ENABLE OUTPUT BURST. Clears automatically upon burst completion,
D12	R/W	*INPUT SYNC	0	Initiates a single input scan, when selected in the Scan and Sync Control Register. Clears automatically upon scan completion,
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets defaults for all registers.
D16-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.   *Clears automatically when operation is completed

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's.   Configuration operations are executed in the sequence shown in Table 3.3.1-1.

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted as described in Section 3.9.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI bus reset, and should be required only once after the initial application of power. During this interval, the response to PCI target accesses is RETRYs. PCI register configuration terminates with the PCI interrupts disabled (Paragraph 3.9).

3.3.2 Initialization

Internal control logic is initialized, without invoking configuration, by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all defaults are invoked.
- Calibration D/A converters are initialized to midrange.

- Analog input/output voltage range is ±10 Volts.
- Analog input/output data coding format is offset binary.
- Both the analog input and output buffers are reset to empty.
- Both rate generators are disabled (Rate Generator Register D16 = HI).

- Analog inputs are configured for eight differential channels.
- Input scan clocking is from the Rate-A generator at 12,000 scans per second.

- All analog output levels are set to zero (midrange).
- Output clocking is from Rate-B generator at 300kHz.
- Output clocking and sync mode is sequential and continuous.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input/Output Parameters

3.4.1 Analog Voltage Range

The analog inputs and outputs share a common voltage range that is selected by BCR control bit field D04-D05, as shown in Table 3.4-1.

Table 3.4-1.   Analog Voltage Range Selection (BCR field D04-D05)

RANGE[1:0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±5 Volts
2	±10 Volts
3	±10 Volts

3.4.2 Timing Organization

Figure 3.4-1 illustrates the manner in which timing signals are organized within the board. The two BCR control bits provide direct software control of clocking and sync operations, and the external sync input and output lines permit external control.   Two rate generators operate directly from the master clock, which has a frequency of 30 MHz on the PC104P-16AIO168 board.

Each Input Scan Clock initiates a complete scan of all active input channels at the maximum conversion rate.   An input scan can contain from 2 to 16 channels, or any single channel can be digitized at the maximum conversion rate.   Each multiple-channel scan commences with Channel 00, and proceeds upward through consecutive channels until the selected number of channels has been digitized.

The Output Sample Clock serves as the output strobe for the analog output channels, and the Output Burst Sync initiates the clocking of a function burst. An External Sync Output line can be used to synchronize the operation of multiple boards.
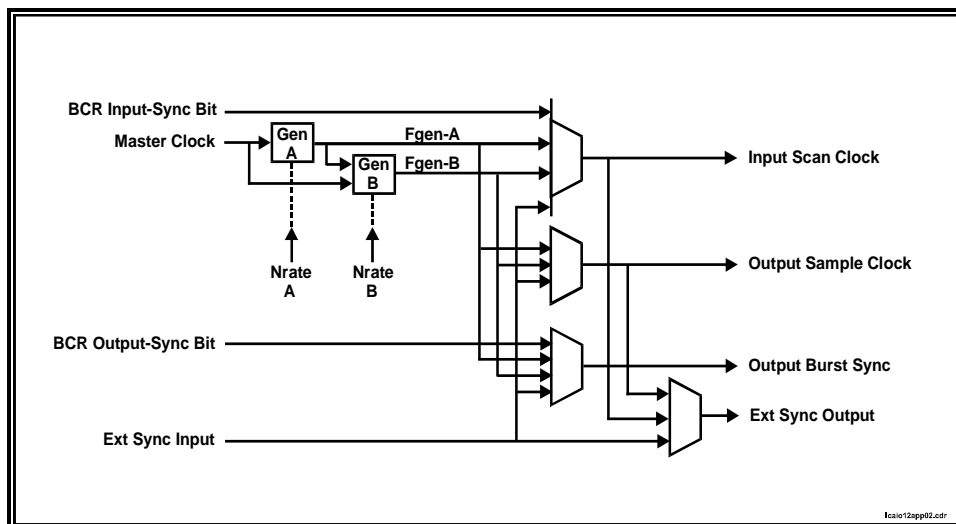
Figure 3.4-1. Clock and Sync Organization

3.4.3 Scan and Sync Control Register

The configuration of internal timing signals is controlled by the Scan and Sync control register (Table 3.4-2).   Bits D00,D01 select the number of channels in an input scan, from 4 channels to 16 channels. The remaining register bits control timing parameters that are described in those sections that pertain to the indicated board functions.

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h   Default: 0000 02D1h

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D01	R/W	ANALOG INPUT SCAN SIZE	1	Number of input channels per scan when operating in the Multiple-Channel scanning mode. 0 => 4 channels per scan 1 => 8 channels per scan 2 => 16 channels per scan (single-ended mode only) 3 => (Reserved) Ignored in the Single-Channel and Two-Channel scanning modes described below:
D02-D03	R/W	ANALOG INPUTS SCAN CLOCK	0	Selects the analog input scan clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line 3 => BCR Input Sync control bit.
D04-D05	R/W	ANALOG OUTPUTS CLOCK	1	Selects the analog output channel clocking source. 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync Input line 3 => Disabled
D06-D07	R/W	ANALOG OUTPUTS SYNC	3	Selects the burst sync source for the analog outputs. 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync Input line 3 => BCR Output Sync control bit .
D08-D09	R/W	EXT SYNC OUTPUT SOURCE	2	Selects the signal source for the External Sync output line: 0 => Analog Inputs Scan Clock 1 => Analog Outputs Sync 2 => External Sync Input line (passthru mode) 3 => Disabled
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	INPUT SCANNING MODE	0	Selects the input scanning mode. Ignored if Two-Channel scanning is selected (See TWO-CHANNEL SCAN below). 0 => Multiple-Channel Mode 1 => Single-Channel Mode
D12-16	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode. Ignored in the Multiple-Channel and Two-Channel scanning modes.
D17	R/W	TWO-CHANNEL SCAN	0	Invokes a 2-Channel scan size when HIGH. Overides the selected Input Scanning Mode
D18-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

NOTE: The terms "sync" and "trigger" are used interchangeably in this text.

3.4.4 Rate Generators

Each of the two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate register. The two rate registers are organized as shown in Table 3.4-3. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. To prevent the input buffer from filling with extraneous data at power-up, and to avoid unexpected signal levels from appearing at the outputs, D16 defaults to the HIGH state in both registers.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014Ch (Rate-B)   Default: 0001 09C4 (Rate-A), 0000 0064h (Rate-B)

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

3.4.4.1 Scan Rate Control

Each rate generator contains a divisor that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of 30 MHz, the output frequency **Fgen** of each generator is determined as:

$$\text{Fgen (Hz)} = 30{,}000{,}000 / \text{Nrate,}$$

where **Nrate** is the decimal equivalent of D00-D15 in the rate generator register.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		FREQUENCY Fgen *
(Dec)	(Hex)	(Hz)
100	0064	300,000
101	0065	297,030
---	---	Fgen (Hz) = 30,000,000 / Nrate
65534	FFFE	457.778
65535	FFFF	457.771

* ±0.015 percent.

For analog inputs, **Fgen** is the scanning trigger frequency, and establishes the rate at which complete scans are initiated. The maximum permissible scanning frequency **Fgen-max** equals the maximum conversion rate, divided by the number of channels in a scan.

$$\text{Fgen-max (analog inputs)} =   \text{Fconv} / \text{Nchan,}$$

where **Fconv** is 300,000 Hz (i.e.: 300,000 conversions per second). For example, if a 16-Channel scan is selected in the Scan and Sync control register, the maximum allowed value for **Fgen** is 18,750 Hz (300,000 divided by 16). Values for **Fgen** higher than **Fgen-max** will produce unpredictable results, and are not recommended.

For analog outputs, **Fgen-max** is the maximum output clocking rate, or 300 kHz.

3.4.4.2 Generator Cascading

To provide very low clocking frequencies, and to permit input and output clocking to be synchronized in integral clocking ratios, the Rate-B generator can be configured to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

$$\text{Fgen-B (Hz)} = 30{,}000{,}000 / (\text{Nrate-A} * \text{Nrate-B}) ,$$

which can produce clocking rates as low as 0.007 Hz.
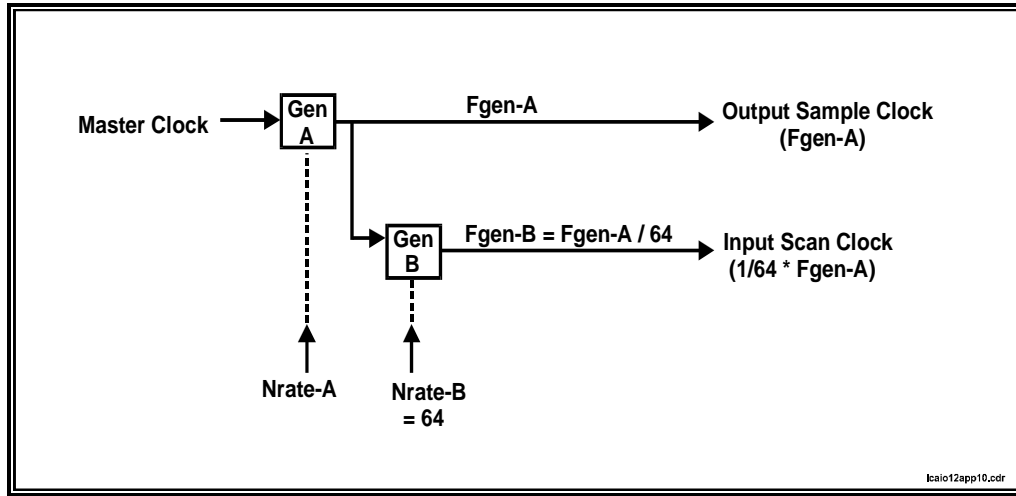
Figure 3.4-2. Cascaded Rate Generator Example

3.4.5 Multiboard Synchronization

Multiple boards can be externally interconnected to produce analog input scans or analog output bursts simultaneously. A variety of hardware and software configurations can be used to produce synchronous operation of multiple boards. Figure 3.5-1 uses one method to illustrate the principles involved.   In this approach, external sync inputs and outputs are daisy-chained from a "sync initiator" board to a number of "target" boards, and the Scan and Sync control register on each board is configured to pass the sync signal down the chain. The original sync signal can originate either on the initiator board itself, or externally as an input to the initiator.

Synchronized operations on the target boards can be analog input scans, analog output bursts, or both functions simultaneously.
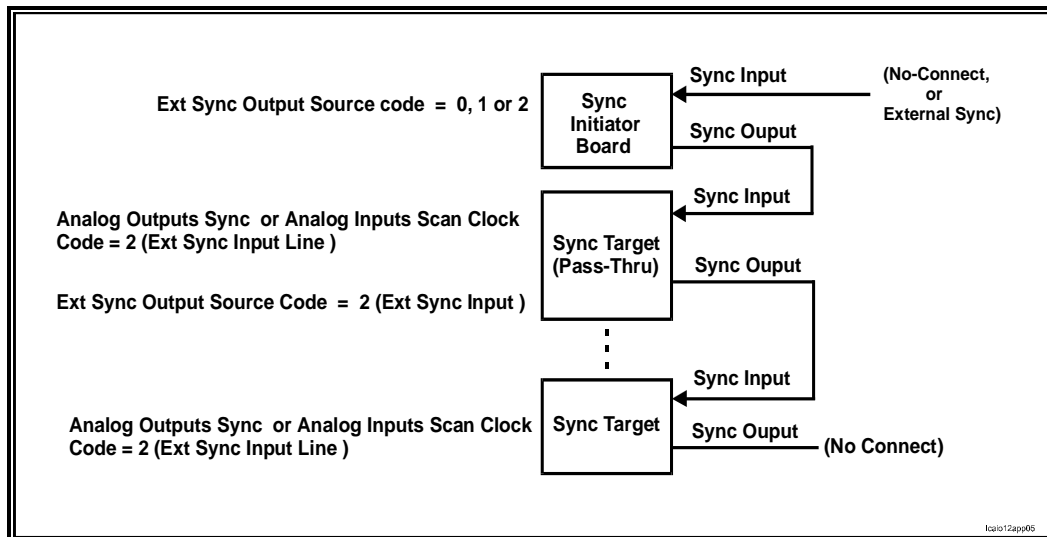
Figure 3.5-1. Multiboard Synchronization

3.5 Analog Input Control

3.5.1 Input Data Organization

Conversion data from the analog-to-digital converter (ADC) flows through a 256-word transfer FIFO into the analog input data buffer, and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

3.5.1.1 Input Data Buffer

Analog input data is read from the Analog Input Data Buffer in longword-serial format, as shown in Table 3.5-1. Each value is right-justified to the LSB, and occupies bit positions D00 through D15. D17-D31 are always returned as zero's.   The capacity of the input data buffer is 32K-samples.

D16 in the input data buffer is set HIGH when the associated data field D00-D15 contains Channel 00 data. D16 is LOW for all channels other than Channel 00.

Table 3.5-1.   Input Data Buffer

Offset: 0008h   Default: N/A

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16	RO	CHANNEL 00 TAG	Indicates Channel 00.
D17-D31	RO	(Inactive)	---

* RO indicates read-only access.   Write-data is ignored.

3.5.1.2 Data Coding Format

Analog input and analog output data is arranged as 16 active right-justified data bits with the coding conventions shown in Table 3.5-2.   The default format is offset binary.   Two's complement format is selected by clearing the Offset Binary control bit LOW in the BCR.

Note: Unless indicated otherwise, offset binary coding is assumed throughout this document.

Table 3.5-2.   Input/Output Data Coding; 16-Bit Data

ANAOG OUTPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	XXXX FFFF	XXXX 7FFF
Zero plus 1 LSB	XXXX 8001	XXXX 0001
Zero	XXXX 8000	XXXX 0000
Zero minus 1 LSB	XXXX 7FFF	XXXX FFFF
Negative Full Scale plus 1 LSB	XXXX 0001	XXXX 8001
Negative Full Scale	XXXX 0000	XXXX 8000

3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-3 controls and monitors the flow of data through the analog input data buffer. Asserting the Clear Buffer control bit HIGH clears, or empties, the buffer, and also aborts any input scan that might be in progress. The Threshold Flag is HIGH when the number of values in the input data buffer and the 256-Word input transfer FIFO exceeds the input threshold value defined by bits D00-D14, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.9) can be programmed to occur on either the rising or falling edge of the threshold flag.

Note: The threshold flag does not respond to samples queued in the transfer FIFO.

Table 3.5-3.   Input Data Buffer Control Register

Offset: 000Ch   **Default: 0000 7FFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-14	R/W	THRESHOLD VALUE	7FFEh	Input buffer threshold value.
D15	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer when asserted HIGH. Aborts current input scan.
D16	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D17-D31	RO	(Inactive)	0	---

 *Clears automatically when operation is completed

3.5.3 Analog Input Function Modes

BCR control bits D00-D03 (AIM0-AIM3) control the analog input configuration, and provide selftest modes for monitoring the integrity of the analog input and output networks. Table 3.5-4 summarizes the input scanning modes.

Table 3.5-4.   Analog Input Function Selection (BCR field D00-D03)

AIM[3:0]	FUNCTION OR MODE
0	Differential analog input mode (Default mode).
1	Single-Ended analog input mode.
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4	Monitor Output Channel 00
5	Monitor Output Channel 01
6	Monitor Output Channel 02
7	Monitor Output Channel 03
8	Monitor Output Channel 04
9	Monitor Output Channel 05
10	Monitor Output Channel 06
11	Monitor Output Channel 07
12-15	(Reserved)

3.5.3.1 Differential Inputs

The analog inputs default to the differential configuration when power is applied, or after initialization. In this mode, the 16 analog input lines are arranged as eight differential pairs, with each pair representing a single input channel. Differential channels are even-numbered from 00 through 14; as 00, 02,...12, 14.

3.5.3.2 Single-ended Inputs

With the single-ended input mode selected, each of the 16 analog input lines is measured in reference to a common *Input Return*, and represents an individual input channel. Single-ended input channels are numbered from 00 through 15; as 00, 01,...14, 15.

3.5.3.3 Selftest Modes

In each of the six selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on the selftest results. Specified board accuracy applies to all selftest measurements, and for critical measurements the average value of multiple readings should be used.

The ZERO selftest measures a dead-zero reference signal and should produce a midscale reading of 0000 8000h. For the +VREF test, a precision reference voltage equal to 96.15% of fullscale is applied as an analog input, and should produce a reading of 0000 FB12h.

Each of the eight analog outputs also can be monitored, and should provide a reading equal to the value written to the associated output DAC (within specified board accuracy).

3.5.4 Input Scan Timing

For each analog input scan clock, all selected analog inputs are scanned once at the maximum conversion rate, with one conversion performed per channel. The number of channels included in each scan is controlled from 2-16 channels by the Scan Size control bit field in the Scan and Sync control register, or any single channel can be selected. Each scan commences with Channel 00 and proceeds upward through successive input channels until the selected number of channels has been digitized.

3.5.4.1 Conversion Rate

During each input scan, the selected channels are scanned and digitized at a fixed conversion rate that is slightly higher than 300,000 conversions per second. The analog input scan clocking rate has no effect on the conversion rate.

3.5.4.2 Scan Rate

To ensure that all scan clocks are acknowledged, the analog input clock frequency **Finput** should not exceed:

$$\textbf{Finput-max (Hz) = 300,000 / Nchan,}$$

where **Nchan** is the number of channels in a scan. For example, an 8-channel scan should not be clocked at a frequency higher than 300,000/8 = 37,500Hz. At higher clock frequencies the duration of each scan exceeds the clocking period, and some clocks will be ignored.

3.5.4.3 Scan Clocking Source

The Scan and Sync control register (Section 3.4.2) provides four sources for analog input scan clocks. The clock can be provided by (a) either of the two rate generators on the board, (b) the External Sync hardware input line, or (c) the Input Sync control bit in the BCR.

If the BCR Input Sync bit is selected as the analog input clock source, an input scan occurs each time the control bit is set HIGH. The Input Sync bit remains HIGH until the scan is completed, after which the bit is cleared automatically.

If the External Sync input line is the analog input clock source, each HIGH-to-LOW transition of the input line initiates an input scan.

3.5.5 Scanning Modes

The analog inputs can be scanned in groups of 4, 8 or 16 channels, or any single channel can be selected for digitizing. If the INPUT SCANNING MODE control bit in the Scan and Sync control register is LOW, the multiple-channel mode is selected, and the number of channels in a scan is selected by the SCAN SIZE control field. An input scan begins with Channel-00, and proceeds upward through successive channels until the selected number of channels has been digitized and stored in the input data buffer.

A 2-channel scan mode overrides all other input mode selections, and digitizes input Channels 00 and 01.

If the INPUT SCANNING MODE control bit is HIGH, the single-channel mode is selected, and the channel to be digitized is selected by the SINGLE_CHANNEL SELECT control field.

3.6 Analog Output Control

3.6.1 Output Data Organization

The Analog Output Data buffer is a FIFO input port that appears to the PCI bus as a single write-only register. Analog output data from the PCI bus flows through the output data buffer into a 256-word transfer FIFO, and through the transfer FIFO to the analog output DAC's.

Two control flags and a channel tag accompany each output data value (Table 3.6-1).   The Output Channel Tag is a three-bit field that identifies the output channel to which the data value is assigned. The Group End Flag is used during simultaneous clocking to identify the last channel in an output group. For function burst operations, the Burst End Flag indicates that the associated data value is the last value in an output burst.

Each analog output value must be accompanied by a channel tag. The group-end and burst-end flags are required only for specific output clocking and synchronization modes.

3.6.1.1 Output Data Buffer

Analog output data is written to the Analog Output Data Buffer in longword-serial format, as shown in Table 3.6-1. Each output value is right-justified to the LSB, and occupies bit positions D00 through D20. A read-access to the output buffer returns an all-zero value. The capacity of the output data buffer is 32K-samples.

Table 3.6-1. Output Data Buffer

Offset: 0018h   **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA00	Least significant data bit
D01-D14	WO	DATA01 - DATA14	Intermediate data bits
D15	WO	DATA15	Most significant data bit
D16-D18	WO	OUTPUT CHANNEL TAG	Output channel identification, 00-07
D19	WO	GROUP END FLAG	Identifies the last channel in an output channel group.
D20	WO	BURST END FLAG (Optional)	Identifies the last channel in an output function.
D21-D31	RO	(Inactive)	Inactive. Data is ignored.

* WO indicates write-only access. Read-access produces all-zero value.

3.6.1.2 Data Coding Format

Analog input and output data can be configured in either offset binary or two's complement format, as shown earlier in Table 3.5-2. The default format is offset binary. Two's complement format is selected by clearing the Offset Binary control bit LOW in the BCR.

3.6.2 Output Data Buffer Control

The Output Buffer control register shown in Table 3.6-2 controls and monitors the flow of data through the analog output data buffer. Asserting the Clear Buffer control bit HIGH clears, or empties, the buffer. The Threshold Flag is HIGH when the number of values in the output data buffer and the 256-word transfer FIFO exceeds the output threshold value defined by bits D00-D14, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.9) can be programmed to occur on either the rising or falling edge of the threshold flag.

Note: The threshold flag does not respond to samples queued in the transfer FIFO.

Table 3.6-2. Output Data Buffer Control Register

Offset: 001Ch   **Default: 0000 7FFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-14	R/W	THRESHOLD VALUE	7FFEh	Output buffer threshold value.
D15	R/W	CLEAR BUFFER *	0	Clears (empties) the output buffer when asserted HIGH.
D16	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the output buffer exceeds the THRESHOLD VALUE.
D17-D31	RO	(Inactive)	0	---

*Clears automatically when operation is completed

3.6.3 Output Clocking Modes

Depending upon which analog output clocking mode is selected, each analog output clock can update a single specific output channel (sequential clocking), or can update a group of output channels simultaneously (simultaneous clocking). The clocking mode is controlled by the Simultaneous Outputs control bit in the BCR.

3.6.3.1 Sequential Clocking

This is the default output clocking mode, and is selected by clearing the Simultaneous Outputs control bit LOW in the BCR.   In this mode, each output clock writes a single value from the output data buffer to the output DAC channel assigned by the channel tag.   This process continues until either: (a) output clocking ceases, (b) the output buffer becomes empty, or (c) the end of a data burst is detected (Section 3.6.4).

3.6.3.2 Simultaneous Clocking

The simultaneous output clocking mode is selected by setting the Simultaneous Outputs control bit HIGH in the BCR, and updates a *group* of analog outputs simultaneously when an output clock occurs.   Each channel group is identified by setting the Group End flag HIGH when writing the last channel in the group to the output buffer.

In the simultaneous clocking mode, output values are transferred continuously from the analog output buffer into an intermediate buffer until a Group End flag is encountered. When the Group End flag occurs, the transfer of data from the output buffer to the intermediate buffer ceases, and the controller waits for an output clock. When an output clock occurs, all values in the intermediate buffer are written simultaneously to their assigned analog output DAC channels, and the flow of data from the data buffer to the intermediate buffer resumes.

This process continues until either: (a) output clocking ceases, (b) the output buffer becomes empty, or (c) the end of a data burst is detected (Section 3.6.4).

3.6.3.3 Output Clock Source

The Scan and Sync control register (Section 3.4.2) provides three sources for analog output clocks. Either of the two rate generators on the board can be selected to provide the clock, or the clock can be supplied through the External Sync hardware input line.

3.6.4 Output Sync Modes

The analog outputs can be configured to operate in either a *continuous* sync mode or in a *burst* sync mode.

3.6.4.1 Continuous Outputs

In the *continuous* sync mode, the outputs are clocked according to the selected clocking mode (Section 3.6.3) until either output clocking ceases or the output buffer becomes empty. The continuous sync mode is the default output sync mode, and is selected by clearing the Enable Output Burst control bit LOW in the BCR.

3.6.4.2 Data Bursts (Ordering option)

The optional burst output sync mode is selected by setting the Enable Output Burst control bit HIGH in the BCR. In this mode, output clocking is initiated by a *sync* input, and terminates when a Burst End flag is encountered in the analog output buffer (Section 3.6.1). Clocking also terminates if either output clocking ceases or the output buffer becomes empty. Multiple burst functions can exist simultaneously within the data buffer, with the last channel value of each function identified by a Burst End flag. Figure 3.6-1 illustrates the flow of data through the output data buffer before and during a data burst.
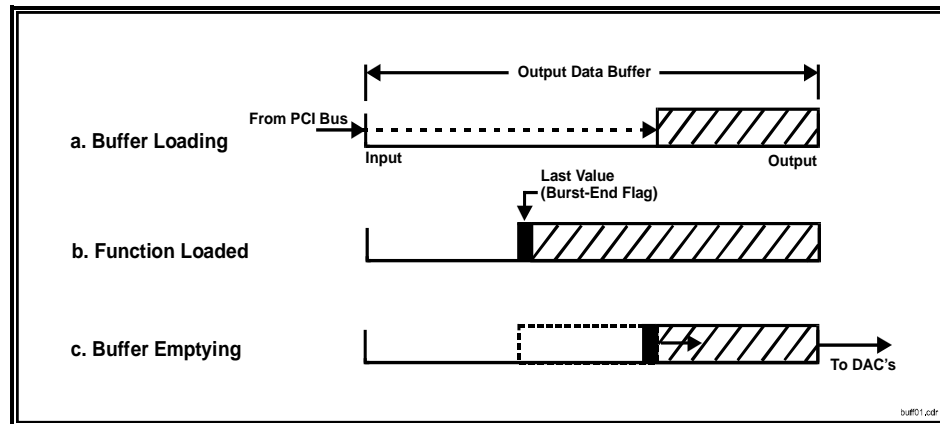
Figure 3.6-1. Function Burst; Output Buffer Data Flow

3.6.4.3 Output Sync Source

The Scan and Sync control register (Section 3.4.2) provides four sources for analog output sync inputs. The sync input can be provided by: (a) either of the two rate generators on the board, (b) the External Trigger hardware input line, or (c) the Output Sync control bit in the BCR.

If the BCR Output Sync bit is selected as the analog output sync clock source, an output burst is initiated each time the control bit is set HIGH. The Output Sync bit remains HIGH until the burst is completed, after which the bit is cleared automatically. If the External Trigger input line is the analog input clock source, each HIGH-to-LOW transition of the input line initiates an output burst.

NOTE: The terms "sync" and "trigger" are used interchangeably in this text.

3.6.5 Function Looping

The analog output data buffer can be closed to operate as a circular buffer in which data recirculates, or loops, indefinitely.

3.6.5.1 Periodic Function Generation

The looping feature permits the generation of periodic functions by: (a) loading a function into the buffer, (b) closing the buffer, and (c) initiating clocking to drive the analog outputs while the function recirculates within the buffer. Figure 3.6.2 illustrates the flow of data within the output buffer while looping. The End Burst flag shown in the figure is not required for looping, but is used for one-shot operations.
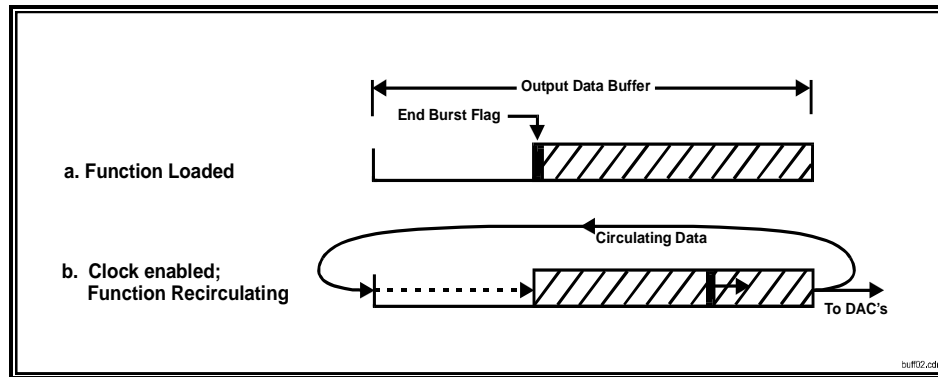
Figure 3.6-2. Periodic Function; Output Buffer Data Flow

3.6.5.2 One-Shot Functions

If the optional Burst End flag in the output buffer is set HIGH at the end of a periodic function, the function operates as described for a data burst, but is not be discarded as it would be if the buffer were open, or non-looping. In this configuration, a burst function in the closed output data buffer can be initiated repeatedly by successive trigger inputs.

3.6.5.3 Multiple Burst Queue

By loading a group of burst functions into the output data buffer, the functions can be queued to generate a sequence of discrete bursts. Each burst is terminated by a Burst End flag, and each sync input initiates the next burst in the queue. The sequence can be repeated indefinitely, and the number of functions that can be queued in this manner is limited only by the 32K-sample capacity of the buffer.

3.7 Autocalibration

To obtain maximum accuracy from the PC104P-16AIO168 board, autocalibration should be performed after power warmup and after each initialization. Autocalibration uses current settings for the analog input/output voltage range, and ignores all other control parameters such as input configuration, clocking rates, etc. No control settings are altered during autocalibration, and existing analog input signals are ignored.

Autocalibration is invoked by setting the Autocal control bit HIGH in the BCR. The control bit returns LOW (normal operation) automatically at the end of autocalibration. Autocalibration can be invoked at any time. Autocalibration has a duration of approximately 2-3 seconds. Completion of the operation can be detected either by polling the Autocal control bit in the BCR for a LOW (zero) state, or by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.9) and waiting for the interrupt request.

Note: The analog outputs are active during autocalibration.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in calibration DAC's. If a board is defective, the autocalibration process may be unable to successfully calibrate all channels. If this situation occurs, the AUTOCAL PASS status bit in the BCR will be cleared LOW at the end of the

autocalibration interval, and will remain LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.8 Digital Control Outputs

Four digital output control lines are controlled through the Digital Output Control register shown in Table 3.8-1. Each output level is HIGH when the corresponding control bit is HIGH, or is LOW when the bit is LOW.

Table 3.8-1. Digital Output Control Register

Offset: 0024h   Default: 0000 0000h

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	DIGITAL OUTPUT 00	0	Digital output line control bits. Noninverted at output.
D01	R/W	DIGITAL OUTPUT 01	0	
D02	R/W	DIGITAL OUTPUT 02	0	
D03	R/W	DIGITAL OUTPUT 03	0	
D04-D31	RO	(Inactive)	0	---

3.9 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.9.1)
b. The *PCI interrupt* must be enabled (Section3.9.2).

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.9.2.

3.9.1 Local Interrupt Request

The single local interrupt request line is controlled by the Interrupt Control Register shown in Table 3.9-1. Three simultaneous source conditions (IRQ 0,1 and 2) are available for the request, with multiple conditions available for each source. IRQ 0,1 and 2 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for any of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.9-1. Interrupt Control Register

Offset: 0000 0004h   **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT CONDITION
D00-02	R/W	IRQ0 A0,1,2	0	0	Idle. Interrupt disabled unless initializing. Default state after reset.
				1	Autocalibration operation completed
				2	(Reserved)
				3	(Reserved)
				4	(Reserved)
				5	(Reserved)
				6	(Reserved)
				7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	(Reserved)
				4	(Reserved)
				5	(Reserved)
				6	(Reserved)
				7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-10	R/W	IRQ2 A0,1	0	0	Idle; no interrupt condition selected.
				1	Output buffer threshold LOW-HIGH transition
				2	Output buffer threshold HIGH-LOW transition
				3	Output burst completed
				4	(Reserved)
				5	(Reserved)
				6	(Reserved)
				7	(Reserved)
D11	R/W	IRQ2 REQUEST	0	---	Group 2 interrupt request flag. See D03.
D12-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only.   * HIGH after reset.

3.9.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled or disabled by setting the control bits shown in Table 3.9-2 to the indicated states in the *Runtime Interrupt Control/Status Register.*

The address of the interrupt control/status register is obtained by adding 68h to the base address that is located in the PCI configuration register space.

Table 3.9-2. PCI Interrupt Control

Interrupt Control/Status Register Bit	Interrupt Enabled	Interrupt Disabled (Default)
Bit 08	1	0
Bit 11	1	0
Bit 16	1	0

3.10 DMA Operation

DMA transfers to the analog output FIFO buffer are supported with the board operating as bus master and with local bursting disabled. Table 3.10-1 illustrates a typical PCI register configuration that would control a non-chaining, non-incrementing DMA transfer, and in which a PCI interrupt is generated when the transfer has been completed. Bit 02 in the PCI Command register (04h) must be set HIGH to select the bus mastering mode. Refer to the PCI-9080 data manual for a detailed description of these registers.

Table 3.10-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial Analog Input Buffer local address (Analog input buffer)	0000 0008h
		Initial Analog Output Buffer local address (Analog output buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
		Transfer direction; PCI bus to Local bus (Analog outputs)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status Register (A8h) should be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

3.11 Periodic Function Looping Examples

The examples presented in this section illustrate the principles involved in using the looping feature to generate periodic functions, and can be modified or combined for more complex operations. Specific operating modes and procedures will vary widely according to the unique requirements of each application.

Table 3.11-1. Summary of Periodic Function Examples

Example	Description	Comments
1	Continuous Periodic Function; Sequential Clocking	Each output clock writes the value for only a single channel to the associated analog output. Sync events and both the Group-End and Burst-End flags in the output data buffer are ignored.
2	Continuous Periodic Function; Simultaneous Clocking	Data values accumulate in an intermediate buffer until an entire channel group has been loaded, as indicated by the Group-End flag in the output data buffer. When the Group-End flag is detected, all output channels in the group update simultaneously at the next output clock. Sync events and the Burst-End flag in the output data buffer are ignored.
3	Burst Periodic Function; Simultaneous Clocking	Identical to Example 2, except: a. The last value in the function has the Burst-End flag set HIGH. Generation of the function starts when a sync input event occurs, and terminates when the Burst-End flag is encountered in the output data buffer. b. Multiple functions can be concatenated within the output data buffer. Each sync input event initiates the next function in the sequence.
4	Burst Periodic Function; Sequential Clocking	Identical to Example 3, except that each output clock writes the value for only a single channel to the associated analog output, and the Group-End flag is ignored.

Table 3.11-2. Continuous Periodic Function; Sequential Clocking

STEP	OPERATION	REGISTER DESCRIPTION	OFFSET	EXAMPLE
1	Disable output clock.	Scan and Sync	0020h	0000 02F2h
2	Disable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0001 07D0h 0001 0050h
3	Load output function.	Output Data Buffer	0018h	---
4	Select : Looping buffer mode Sequential clocking mode Continuous sync mode.	BCR	0000h	0000 4460h
5	Select output clock and sync sources.	Scan and Sync	0020h	0000 02D2h
6	Enable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0000 07D0h 0000 0050h

Table 3.11-3. Continuous Periodic Function; Simultaneous Clocking

STEP	OPERATION	REGISTER DESCRIPTION	OFFSET	EXAMPLE
1	Disable output clock.	Scan and Sync	0020h	0000 02F2h
2	Disable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0001 07D0h 0001 0050h
3	Load output function.	Output Data Buffer	0018h	---
4	Select : Looping buffer mode Simultaneous clocking mode Continuous sync mode.	BCR	0000h	0000 4560h
5	Select output clock and sync sources.	Scan and Sync	0020h	0000 02D2h
6	Enable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0000 07D0h 0000 0050h

Table 3.11-4. Burst Periodic Function; Simultaneous Clocking

STEP	OPERATION	REGISTER DESCRIPTION	OFFSET	EXAMPLE
1	Disable output clock.	Scan and Sync	0020h	0000 02F2h
2	Disable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0001 07D0h 0001 0050h
3	Load output function(s).	Output Data Buffer	0018h	---
4	Select : Looping buffer mode Simultaneous clocking mode Burst sync mode.	BCR	0000h	0000 4760h
5	Select output clock and sync sources.	Scan and Sync	0020h	0000 02D2h
6	If using the interrupt to detect burst completion, select Output Burst Completed	Interrupt Control	0004h	0000 0300h
7	Enable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0000 07D0h 0000 0050h
8	Apply a burst sync input event (through the BCR in this example).	BCR	0000h	0000 4F60h
9	Wait for burst completion (interrupt IRQ2; or BCR Output Sync bit clears LOW.	(BCR)	0000h	(0000 4760h)
10	Repeat Steps 8 and 9 for successive bursts.	---	---	---

Table 3.11-5. Burst Periodic Function; Sequential Clocking

STEP	OPERATION	REGISTER DESCRIPTION	OFFSET	EXAMPLE
1	Disable output clock.	Scan and Sync	0020h	0000 02F2h
2	Disable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0001 07D0h 0001 0050h
3	Load output function(s).	Output Data Buffer	0018h	---
4	Select : Looping buffer mode Sequential clocking mode Burst sync mode.	BCR	0000h	0000 4660h
5	Select output clock and sync sources.	Scan and Sync	0020h	0000 02D2h
6	If using the interrupt to detect burst completion, select Output Burst Completed	Interrupt Control	0004h	0000 0300h
7	Enable rate generator(s) if used for output clocking.	Rate-A Generator Rate-B Generator	0010h 0014h	0000 07D0h 0000 0050h
8	Apply a burst sync input event (through the BCR in this example).	BCR	0000h	0000 4F60h
9	Wait for burst completion (interrupt IRQ2; or BCR Output Sync bit clears LOW.	(BCR)	0000h	(0000 4760h)
10	Repeat Steps 8 and 9 for successive bursts.	---	---	---

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PC104P-16AIO168 board contains eight 16-Bit D/A converters and a 16-bit scanning A/D converter. A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller (Figure 4.1-1). Gain and offset corrections of the analog input and output channels are performed by calibration DAC's that are loaded with channel correction values during autocalibration

The analog inputs are software-configurable either as 16 single-ended channels, or as eight differential signal pairs. Buffer amplifiers on all input lines eliminate multiplexer input switching noise, and minimize crosstalk and input bias currents. A selftest switching network routes a precision reference to the A/D converter during autocalibration, and also provides loopback monitoring of all analog output channels. Analog input data accumulates in a 32K-sample buffer until retrieved by the PCI bus.
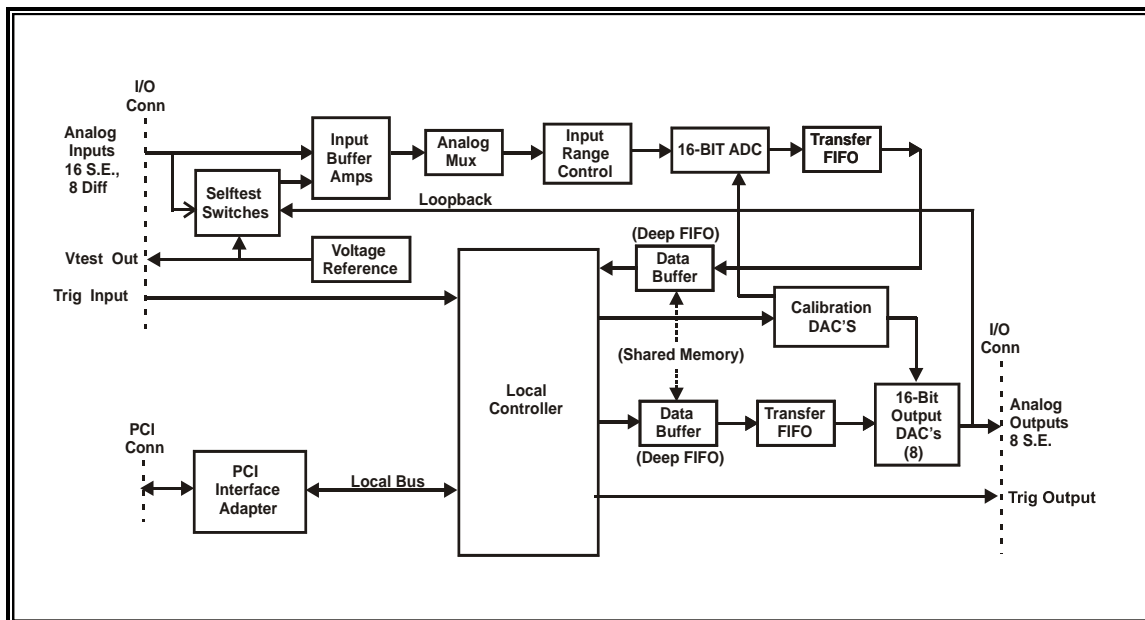
Figure 4.1-1. Functional Block Diagram

Each of the eight analog output channels contains a dedicated 16-bit D/A converter, offset and gain calibration DAC's, and an output range control network. The board receives analog output data from the PCI bus through a 32K-sample FIFO buffer.

Analog input scanning can be synchronized to the analog output sample clock, or the inputs and outputs can be operated independently. Both the analog inputs and outputs can be synchronized externally, and a hardware output permits multiple boards to be synchronized together.

An interrupt request can be generated in response to selected conditions, including the status of the analog input and output data buffers. The analog inputs and outputs share a common software-selectable voltage range of ±2.5V, ±5V or ±10V.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches and analog multiplexer shown in Figure 4.1-1. During normal operation, analog input channels from the input/output connector are scanned and digitized. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC, or the analog output channels can be monitored by selecting the loopback selftest mode. The analog multiplexer establishes the input configuration as either single-ended or differential, in response to software control.

The selected input signals pass through input buffer amplifiers, and subsequently are sorted by an analog multiplexer for digitizing by the 16-bit ADC. The buffer amplifiers provide the fast response necessary to drive the analog multiplexer, and also serve to minimize interchannel crosstalk and to prevent charge coupling from the multiplexer back to the signal source. By routing all inputs through the same signal path, the errors introduced by all components in that path are accounted for during autocalibration. Final selection of the input signal is provided by the analog multiplexer.

The output of the multiplexer is buffered by a differential amplifier in the input range control functional block, and finally is converted by the ADC into a 16-bit digital code. Data is extracted from the ADC in parallel format, and passes through a 256-sample transfer FIFO into the main analog input data buffer. Offset and gain trimming of the ADC is provided by a pair of 10-bit DAC's that are loaded with trim values determined during autocalibration.

Analog channels from the input/output connector are scanned in a pipeline sequence, in which the subsequent channel in the scanning sequence is selected and allowed to settle, while the current sample is being digitized. This approach increases the effective scan rate without requiring shorter settling or conversion times. Digitizing always occurs at the maximum conversion rate, and a single scan of all selected input channels commences at the beginning of each scan interval. The input scan rate can be controlled from: (a) either of two internal rate generators, (b) software, through a control register, or (c) an external hardware sync source.

4.3 Analog Outputs

Each of the eight analog output channels consists of a 16-bit output DAC and two 10-bit calibration DAC's. Output data values from the PCI bus pass through the main output data buffer into a 256-sample transfer FIFO. The local controller reads the 16-bit channel data value for each channel from the transfer FIFO, and sends the value serially to in an intermediate buffer in the associated output DAC.

If the *sequential* clocking mode is selected, the controller then transfers the intermediate value to the DAC's output register at the next occurrence of the selected output clock. If simultaneous clocking is selected, however, output values accumulate in the intermediate DAC registers until an entire predetermined group of channels has been loaded into the assigned DAC's. At the next occurrence of the output clock then, the output registers of all DAC's are updated simultaneously.

Clocking of the output channels can be controlled from the same sources that are available to the analog inputs. The analog outputs support the generation of continuous, periodic and burst (one-shot) functions, or can be controlled individually in a sequential mode.

The two calibration DAC's in each output channel provide offset and gain trimming of the associated 16-bit output DAC, using trim values that are determined during autocalibration.

4.4 Rate Generators

The local controller contains two independent rate generators, each of which divides a master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a clocking source for the analog inputs or outputs, and the generators can be cascaded to produce very long clocking intervals or synchronized input/output clocking ratios.

4.5 Data Buffers and Transfer FIFO's

The analog input and output data buffers share a common memory element that is arbitrated to produce effectively independent buffer functions. To avoid the data loss that might otherwise occur during arbitration cycles, data to the input buffer and from the output buffer pass through dedicated, nonarbitrated transfer FIFO's. Each transfer FIFO has a capacity of 256 data values, and ensures an uninterrupted flow of data in the critical input and output data paths. Operation of the transfer FIFO's is transparent to control software and drivers.

4.6 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input and output channels to a single internal voltage reference. The utility can be invoked at any time by the control software, and has a duration of less than one second.

An internal voltage reference is used to calibrate the span of each channel, and a dead-zero ground reference is used to calibrate the offset value. Each of the ten 10-bit calibration DAC's is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit initially is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response from the channel, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 10 bits have been tested and adjusted. The final value in the calibration DAC remains in the DAC until the autocalibration sequence is repeated, or until power is removed.

4.7 Power Control

Regulated supply voltages of ±5 Volts and ±14 Volts are required by the analog networks, and are derived from the +5-Volt input provided by the PCI bus. A DC/DC converter produces preregulated voltages that are subsequently series-regulated to the required output levels. Series regulation ensures minimum noise and optimum performance of the power supply outputs.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	ACTIVE BITS	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	16	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	12	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	17	---	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	17	000X 7FFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	17	0001 09C4h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	17	0000 0064h	Rate-B generator freq selection
0018	OUTPUT DATA BUFFER	WO	21	---	Analog output data buffer
001C	OUTPUT BUFFER CONTROL	R/W	17	000X 7FFEh	Output buffer threshold and control
0020	SCAN AND SYNC CONTROL	R/W	17	0000 02D1h	Channels per scan; Clocking and Sync sources.
0024	DIGITAL OUTPUT CONTROL	R/W	4	0000 0000h	Digital output control register
0028	FIRMWARE REVISION *	---	---	---	---
002C	AUTOCAL VALUES *	---	---	---	---
0030-3F	(Reserved)	---	---	---	Inactive

R/W = Read/Write, RO = Read-Only, WO = Write-Only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h   **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D03	R/W	AIM0	0	Analog input mode. Selects input configuration or selftest mode. Defaults to differential input mode
D04	R/W	RANGE0	0	Analog input/output range. Defaults to ±10V range.
D05	R/W	RANGE1	1	
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.
D07	R/W	(Reserved)	0	---
D08	R/W	SIMULTANEOUS OUTPUTS	0	Selects simultaneous or channel-sequential output mode. Defaults LOW to channel-sequential output mode.
D09	R/W	ENABLE OUTPUT BURST	0	Enables output bursting (one-shot) mode when HIGH.
D10	R/W	ENABLE OUTPUT LOOPING	0	Enables output function looping when HIGH.
D11	R/W	*OUTPUT SYNC	0	Initiates a single output burst, when enabled by ENABLE OUTPUT BURST. Clears automatically upon burst completion,
D12	R/W	*INPUT SYNC	0	Initiates a single input scan, when selected in the Scan and Sync Control Register. Clears automatically upon scan completion,
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets defaults for all registers.
D16-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.   *Clears automatically when operation is completed

Table 3.4-1. Analog Voltage Range Selection (BCR field)

RANGE[1:0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±5 Volts
2	±10 Volts
3	±10 Volts

Table 3.4-2.   Scan and Sync Control Register

Offset: 0020h   **Default: 0000 02D1h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D01	R/W	ANALOG INPUT SCAN SIZE	1	Number of input channels per scan when operating in the Multiple-Channel scanning mode. 0 => 4 channels per scan 1 => 8 channels per scan 2 => 16 channels per scan (single-ended mode only) 3 => (Reserved) Ignored in the Single-Channel and Two-Channel scanning modes described below:
D02-D03	R/W	ANALOG INPUTS SCAN CLOCK	0	Selects the analog input scan clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line 3 => BCR Input Sync control bit.
D04-D05	R/W	ANALOG OUTPUTS CLOCK	1	Selects the analog output channel clocking source. 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync Input line 3 => Disabled
D06-D07	R/W	ANALOG OUTPUTS SYNC	3	Selects the burst sync source for the analog outputs. 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync Input line 3 => BCR Output Sync control bit .
D08-D09	R/W	EXT SYNC OUTPUT SOURCE	2	Selects the signal source for the External Sync output line: 0 => Analog Inputs Scan Clock 1 => Analog Outputs Sync 2 => External Sync Input line (passthru mode) 3 => Disabled
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	INPUT SCANNING MODE	0	Selects the input scanning mode. Ignored if Two-Channel scanning is selected (See TWO-CHANNEL SCAN below). 0 => Multiple-Channel Mode 1 => Single-Channel Mode
D12-16	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode. Ignored in the Multiple-Channel and Two-Channel scanning modes.
D17	R/W	TWO-CHANNEL SCAN	0	Invokes a 2-Channel scan size when HIGH. Overides the selected Input Scanning Mode
D18-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-3.   Rate Generator Register

Offset: 0010h (Rate-A), 0014Ch (Rate-B)   Default: 0001 09C4 (Rate-A), 0000 0064h (Rate-B)

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		FREQUENCY Fgen *
(Dec)	**(Hex)**	**(Hz)**
100	0064	300,000
101	0065	297,030
---	---	Fgen (Hz) = 30,000,000 / Nrate
65534	FFFE	457.778
65535	FFFF	457.771

Table 3.5-1. Input Data Buffer

Offset: 0008h   **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16	RO	CHANNEL 00 TAG	Indicates Channel 00.
D17-D31	RO	(Inactive)	---

 * RO indicates read-only access.   Write-data is ignored.

Table 3.5-2. Input/Output Data Coding; 16-Bit Data

ANAOG OUTPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	XXXX FFFF	XXXX 7FFF
Zero plus 1 LSB	XXXX 8001	XXXX 0001
Zero	XXXX 8000	XXXX 0000
Zero minus 1 LSB	XXXX 7FFF	XXXX FFFF
Negative Full Scale plus 1 LSB	XXXX 0001	XXXX 8001
Negative Full Scale	XXXX 0000	XXXX 8000

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch   **Default: 0000 7FFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-14	R/W	THRESHOLD VALUE	7FFEh	Input buffer threshold value.
D15	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer when asserted HIGH. Aborts current input scan.
D16	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D17-D31	RO	(Inactive)	0	---

 *Clears automatically when operation is completed

Table 3.5-4. Analog Input Function Selection (BCR field D00-D02)

AIM[3:0]	FUNCTION OR MODE
0	Differential analog input mode (Default mode).
1	Single-Ended analog input mode.
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4	Monitor Output Channel 00
5	Monitor Output Channel 01
6	Monitor Output Channel 02
7	Monitor Output Channel 03
8	Monitor Output Channel 04
9	Monitor Output Channel 05
10	Monitor Output Channel 06
11	Monitor Output Channel 07
12-15	(Reserved)

Table 3.6-1. Output Data Buffer

Offset: 0018h   **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA00	Least significant data bit
D01-D14	WO	DATA01 - DATA14	Intermediate data bits
D15	WO	DATA15	Most significant data bit
D16-D18	WO	OUTPUT CHANNEL TAG	Output channel identification, 00-07
D19	WO	GROUP END FLAG	Identifies the last channel in an output channel group.
D20	WO	BURST END FLAG (Optional)	Identifies the last channel in an output function.
D21-D31	RO	(Inactive)	Inactive. Data is ignored.

 * WO indicates write-only access. Read-access produces all-zero value.

Table 3.6-2. Output Data Buffer Control Register

Offset: 001Ch   **Default: 0000 7FFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-14	R/W	THRESHOLD VALUE	7FFEh	Output buffer threshold value.
D15	R/W	CLEAR BUFFER *	0	Clears (empties) the output buffer when asserted HIGH.
D16	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the output buffer exceeds the THRESHOLD VALUE.
D17-D31	RO	(Inactive)	0	---

*Clears automatically when operation is completed

Table 3.8-1. Digital Output Control Register

Offset: 0024h   **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	DIGITAL OUTPUT 00	0	Digital output line control bits. Noninverted at output.
D01	R/W	DIGITAL OUTPUT 01	0	
D02	R/W	DIGITAL OUTPUT 02	0	
D03	R/W	DIGITAL OUTPUT 03	0	
D04-D31	RO	(Inactive)	0	---

Table 3.9-1. Interrupt Control Register

Offset: 0000 0004h   **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT CONDITION
D00-02	R/W	IRQ0 A0,1,2	0	0	Idle. Interrupt disabled unless initializing. Default state after reset.
				1	Autocalibration operation completed
				2	(Reserved)
				3	(Reserved)
				4	(Reserved)
				5	(Reserved)
				6	(Reserved)
				7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	(Reserved)
				4	(Reserved)
				5	(Reserved)
				6	(Reserved)
				7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-10	R/W	IRQ2 A0,1	0	0	Idle; no interrupt condition selected.
				1	Output buffer threshold LOW-HIGH transition
				2	Output buffer threshold HIGH-LOW transition
				3	Output burst completed
				4	(Reserved)
				5	(Reserved)
				6	(Reserved)
				7	(Reserved)
D11	R/W	IRQ2 REQUEST	0	---	Group 2 interrupt request flag. See D03.
D12-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only.   * HIGH after reset.

Table 3.9-2. PCI Interrupt Control

Interrupt Control/Status Register Bit	Interrupt Enabled	Interrupt Disabled (Default)
Bit 08	1	0
Bit 11	1	0
Bit 16	1	0

Table 3.10-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial Analog Input Buffer local address (Analog input buffer)	0000 0008h
		Initial Analog Output Buffer local address (Analog output buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
		Transfer direction; PCI bus to Local bus (Analog outputs)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Revision History:

08-07-2002:   Origination.

09-04-2006:   Table 3.1-1:   Added revision and autocal registers to 'quick-ref' Table 3.1-1.
                Table 3.5-4:   Changed hex aim[] to decimal.
                General: Added sync/trigger equivalency notes.
                General: Revised for mclk change from 24MHz to 30MHz.

07-03-2010:   Removed references to the PMC form factor.

03-27-2013:   2.3, 3.6.4, 3.6.5:   Clarified the optional nature of triggered output bursts.
                Table 3.6-1:   Revised context of the burst-end flag to 'optional'.