General Standards Corporation

High Performance Bus Interface Solutions

Rev: 053007

PCI66-18AISS8AO8

8-Input, 8-Output 18-Bit Precision Wideband 500KSPS PCI Analog Input/Output Board

With Selectable Current-Loop Input Terminators

REFERENCE MANUAL

PRELIMINARY

TABLE OF CONTENTS

`TABLE OF CONTENTS (Continued)

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TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1.0

INTRODUCTION

The PCI66-18AISS8AO8 is a precision 18-Bit analog I/O PCI product that provides eight simultaneously sampled input channels and eight simultaneously clocked output channels. Inputs and outputs can be clocked synchronously or independently at rates up to 500 KSPS per channel, and are supported by independent 512K-Sample FIFO data buffers. Both continuous and burst clocking modes are supported, and voltage ranges are independently software-selectable as ±10V, ±5V, ±2.5V, 0 to +10V or 0 to +5V for inputs and outputs. Clocking and triggering rates can be derived from internal rate generators, or from external clock and trigger sources to support the synchronous operation of multiple boards.

Input sampling employs successive-approximation (SAR) conversion, which avoids the high latency or minimum-rate limitations of delta-sigma and pipelined conversion schemes. Each analog input channel can be individually programmed to provide termination for current-loop instrumentation. The analog outputs use a weighted-DAC R-2R configuration which, like the analog inputs, minimizes latency and has no minimum clocking rate. The outputs can be software-configured for either single-ended or 3-wire differential operation.

On-demand autocalibration determines and applies error correction for all input and output channels, and a selftest input switching network permits board integrity to be verified by the host. Eight bidirectional digital I/O lines are programmable as inputs or outputs.

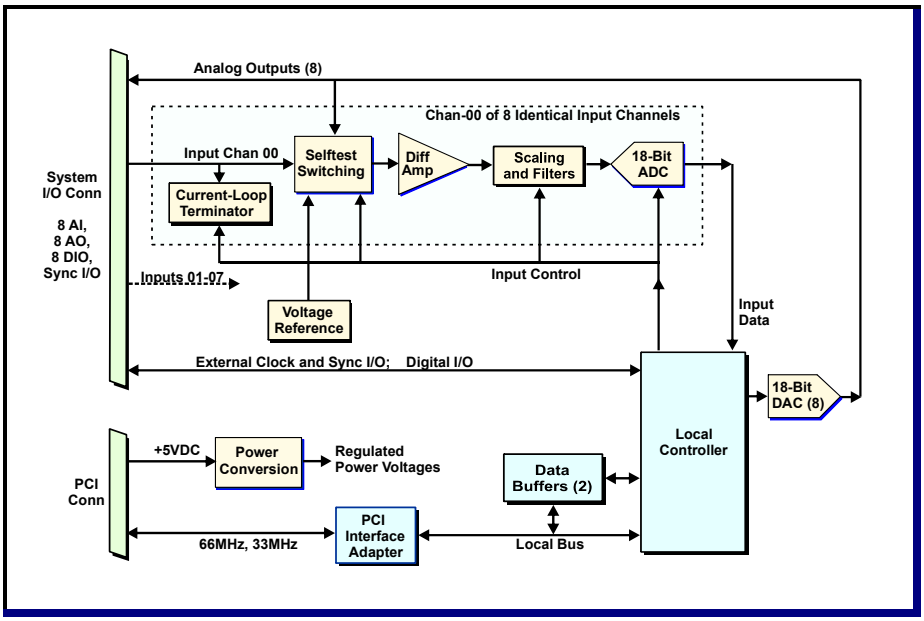

Figure 1.1-1. Functional Organization

This product complies with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density dual-ribbon 100-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. Operation over the specified temperature range is achieved with conventional air cooling.

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SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host system are adequately discharged to ground.

Before removing the board from the protective shipping envelope, select an empty PCI slot in the host computer and, if a blank panel bracket is located in the slot position, remove the bracket. Then remove the board from the shipping envelope and position the board with the panel bracket oriented toward the expansion panel opening. Align the board's PCI edge-connector with the mating connector on the motherboard, and carefully press the board into position. Verify that the PCI connector has mated completely, and that the panel bracket is seated against the fastener bracket above the panel opening. To complete the installation, secure the panel bracket and rear support bracket with appropriate fasteners. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with a 100-pin dual-ribbon connector, equivalent to AMP #749621-9. The AMP displacement connector accepts two 50-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connections

ROW-A	
PIN	SIGNAL
1	INPUT 00 LO
2	INPUT 00 HI
3	INPUT RTN
4	INPUT RTN
5	INPUT 01 LO
6	INPUT 01 HI
7	INPUT RTN
8	INPUT RTN
9	INPUT 02 LO
10	INPUT 02 HI
11	INPUT RTN
12	INPUT RTN
13	INPUT 03 LO
14	INPUT 03 HI
15	INPUT RTN
16	INPUT RTN
17	INPUT 04 LO
18	INPUT 04 HI
19	INPUT RTN
20	INPUT RTN
21	INPUT 05 LO
22	INPUT 05 HI
23	INPUT RTN
24	INPUT RTN
25	INPUT 06 LO
26	INPUT 06 HI
27	INPUT RTN
28	INPUT RTN
29	INPUT 07 LO
30	INPUT 07 HI
31	INPUT RTN
32	INPUT RTN
33	OUTPUT RTN 00
34	OUTPUT RTN 00
35	OUTPUT 00 LO
36	OUTPUT 00 HI
37	OUTPUT RTN 00
38	OUTPUT RTN 00
39	OUTPUT 01 LO
40	OUTPUT 01 HI
41	OUTPUT RTN 01
42	OUTPUT RTN 01
43	OUTPUT 02 LO
44	OUTPUT 02 HI
45	OUTPUT RTN 02
46	OUTPUT RTN 02
47	OUTPUT 03 LO
48	OUTPUT 03 HI
49	OUTPUT RTN 03
50	OUTPUT RTN 03

ROW-B	
PIN	SIGNAL
1	OUTPUT 04 LO
2	OUTPUT 04 HI
3	OUTPUT RTN 04
4	OUTPUT RTN 04
5	OUTPUT 05 LO
6	OUTPUT 05 HI
7	OUTPUT RTN 05
8	OUTPUT RTN 05
9	OUTPUT 06 LO
10	OUTPUT 06 HI
11	OUTPUT RTN 06
12	OUTPUT RTN 06
13	OUTPUT 07 LO
14	OUTPUT 07 HI
15	OUTPUT RTN 07
16	OUTPUT RTN 07
17	VTEST RTN
18	VTEST
19	DIGITAL RTN
20	DIGIO 00
21	DIGITAL RTN
22	DIGIO 01
23	DIGITAL RTN
24	DIGIO 02
25	DIGITAL RTN
26	DIGIO 03
27	DIGITAL RTN
28	DIGIO 04
29	DIGITAL RTN
30	DIGIO 05
31	DIGITAL RTN
32	DIGIO 06
33	DIGITAL RTN
34	DIGIO 07
35	DIGITAL RTN
36	OUTPUT CLK INP
37	DIGITAL RTN
38	OUTPUT CLK OUT
39	DIGITAL RTN
40	OUTPUT TRIG INP
41	DIGITAL RTN
42	OUTPUT TRIG OUT
43	DIGITAL RTN
44	INPUT CLK INP
45	DIGITAL RTN
46	INPUT CLK OUT
47	DIGITAL RTN
48	INPUT TRIG INP
49	DIGITAL RTN
50	INPUT TRIG OUT

The 4-channel configuration contains input/output Channels 00-03.

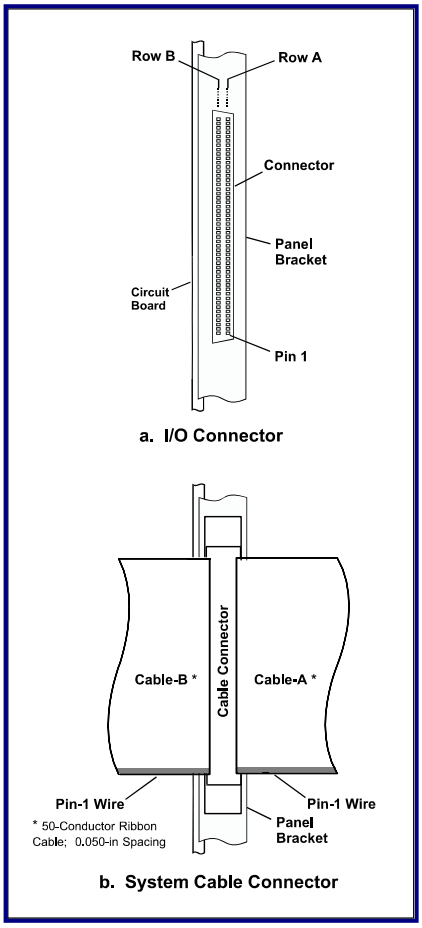

Figure 2.2-1. System I/O Connector

System Cable Mating Connector:
100-Pin 2-row 0.050" dual ribbon-cable connector: AMP # 749621-9.

I/O Connector Installed on Board (Ref)**:**
AMP # 787170-9

2.3 System Configuration

2.3.1 Analog Inputs

The eight analog input channels can be configured for either differential or single-ended operation. The hardware input configuration must be acknowledged by the control software.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials.

This operating mode also offers the highest rejection of the common mode noise, which is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode (Figure 2.3-1b), the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point which ensures that the sum of the signal level **(Vsig)** and the common mode voltage **(Vcm)** remains within the specified maximum input level. Ground current through the INPUT RTN pins must be limited in order to avoid damage to the cable or to the input board.

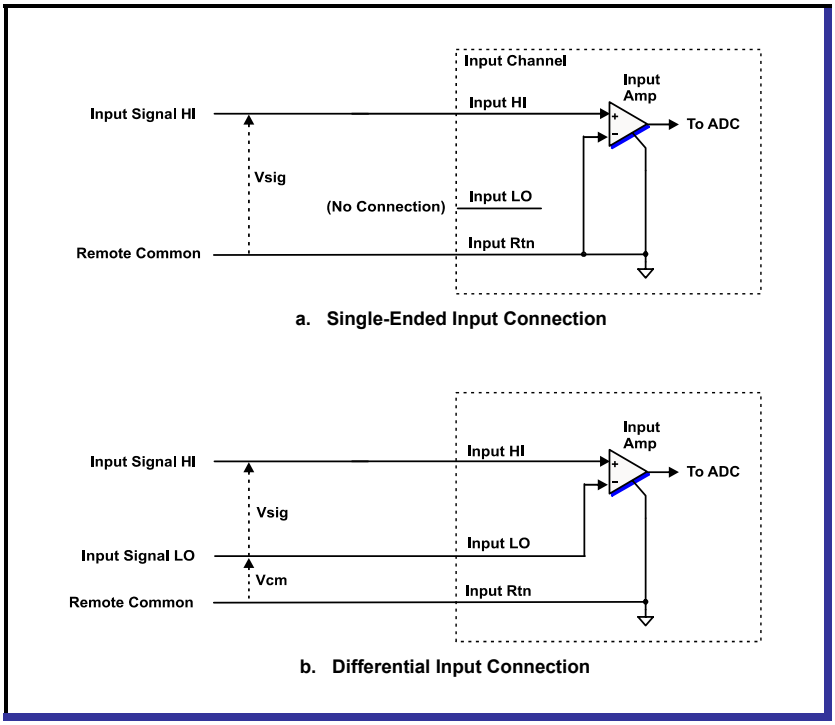

Figure 2.3-1. Voltage Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1a) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. A single-ended configuration usually is more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or could generate potentially destructive ground current.

2.3.1.3 Current-Loop Inputs

Each input channel can be software-configured with a current-loop termination resistance to support those instrumentation signal sources that use this method of communication. The standard value for termination resistance in this product is 500 Ohms.

When current-loop termination is enabled in a channel, the input configuration is as shown in Figure 2.3-2. The total internal resistance is the sum of the precision termination resistance plus other internal resistances, including the resistance of the enabling switch. The input amplifier however receives the input signal directly from the termination resistor, and the other internal resistances simply cause a minor increase (less than 100mV) in the voltage that appears at the input pins. Line resistances further increase the voltage required at the source.

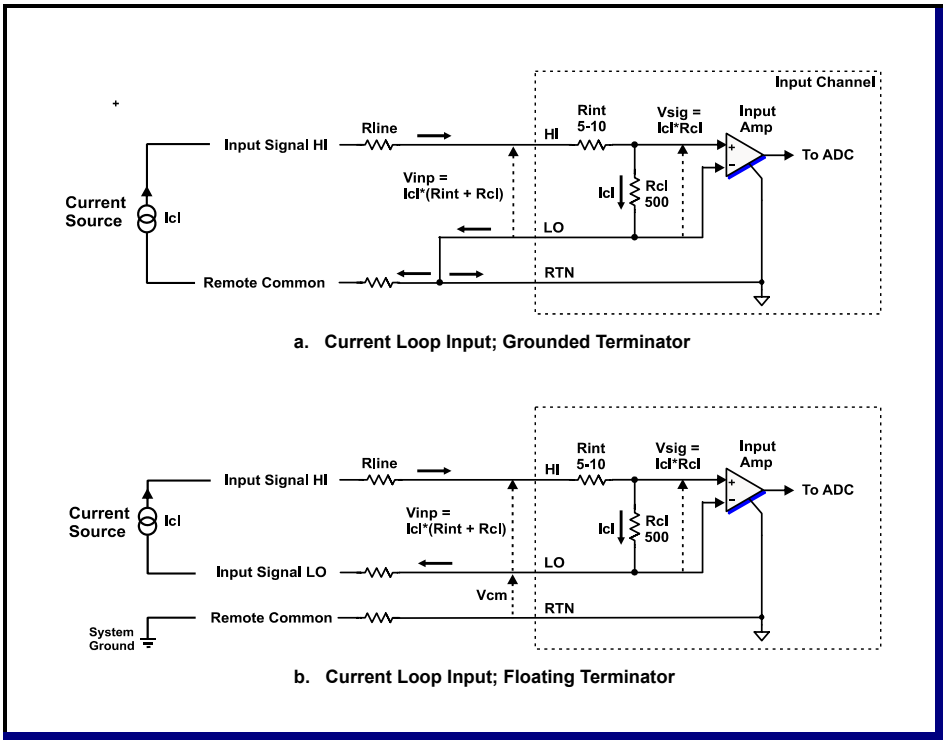

Figure 2.3-2. Current-Loop Input Configurations

A current-loop channel should be configured as a differential input, and usually is connected in one of two arrangements. Floating current sources can be connected in either configuration shown in Figure 2.3-2. Configuration 2.3-2b minimizes susceptibility to induced system noise in the instrumentation cables by routing return current away from the relatively noisy system ground. Current sources that are common to the same system ground as the input board should be connected in a 'floating terminator' configuration (Figure 2.3-2b), to ensure that all return current flows through the LO signal line.

To obtain specified performance In any input configuration, both the HI and LO inputs must be maintained within the voltage extremes specified as 'Input Voltage Limits' in the product specification.

2.3.2 Analog Outputs

2.3.2.1 Output Configurations

The eight analog output channels can be software-configured either as 3-wire balanced differential outputs or as single-ended outputs.

Balanced differential outputs (Figure 2.3-3a) provide the highest immunity to system noise and interference, and are recommended for systems in which the loads will accept differential inputs. Each of the HI and LO outputs carries one-half of the output signal, with the two halves operating as complementary signals of equal amplitude and opposite polarity. Since radiated interference usually affects both output lines simultaneously, the coupled interference appears as a common mode signal which will be attenuated in a differential load.

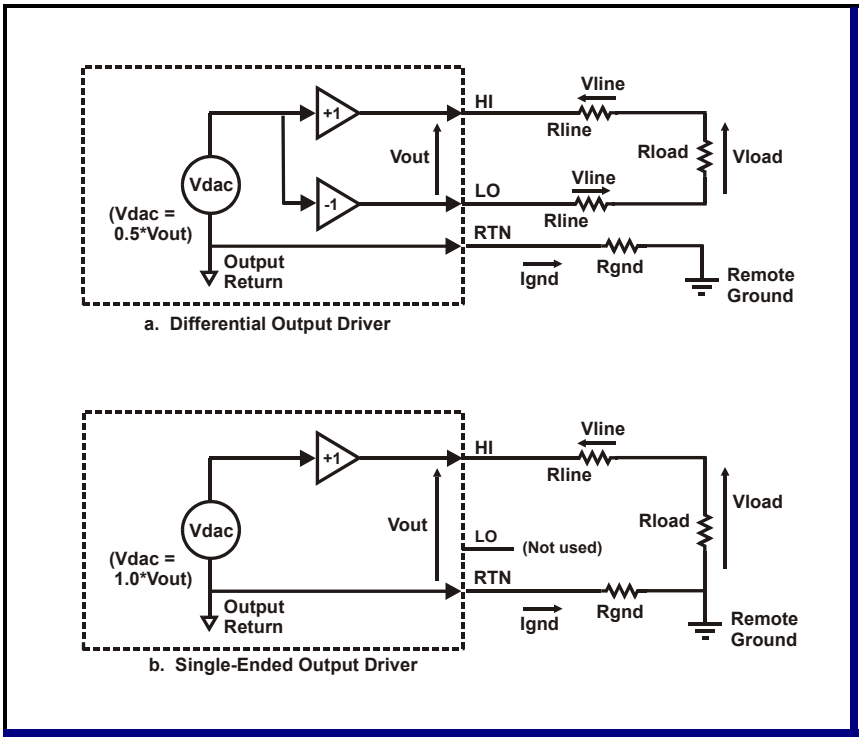

Figure 2.3-3. Output Configurations

For applications requiring single-ended outputs (Figure 2.3-3b), the output signal from each channel appears on the associated HI output pin, and is generated with reference to the output return pin. In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other

2.3.2.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate or heavy loads. Figure 2.3-4 shows the effect of load current on the voltage drop in copper wire of various sizes. A 4.0 milliamp load for example, inserts a voltage drop of more than 0.25 millivolt *per foot* in #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors with milliamp loads, especially in an 18-bit system, in which 1 LSB represents only 19 microvolts on a ±2.5 Volt range.

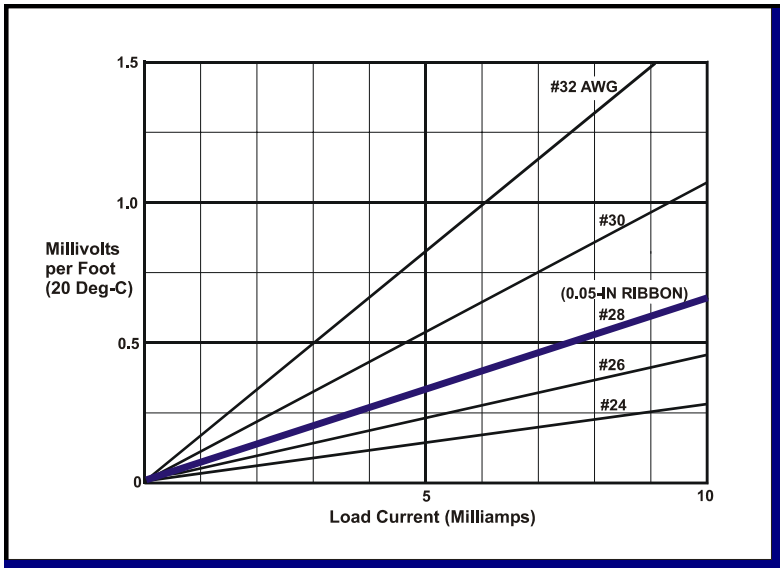

Figure 2.3-4. Line Loss versus Load Current

2.3.3 Multiboard Synchronization

If multiple boards are to be synchronized together, the input and output clock and/or trigger lines can be interconnected between boards in either a 'multidrop' configuration (Figure 2.3-5), or in a daisy-chained sequence (Figure 2.3-6). The multidrop arrangement eliminates the approximately 100ns delay incurred when passing through each board in a daisy-chain sequence, but limits the number of target boards to four. The number of target boards in a daisy-chain sequence is limited only by the number of slots available in a backplane and the maximum acceptable total delay through the targets.

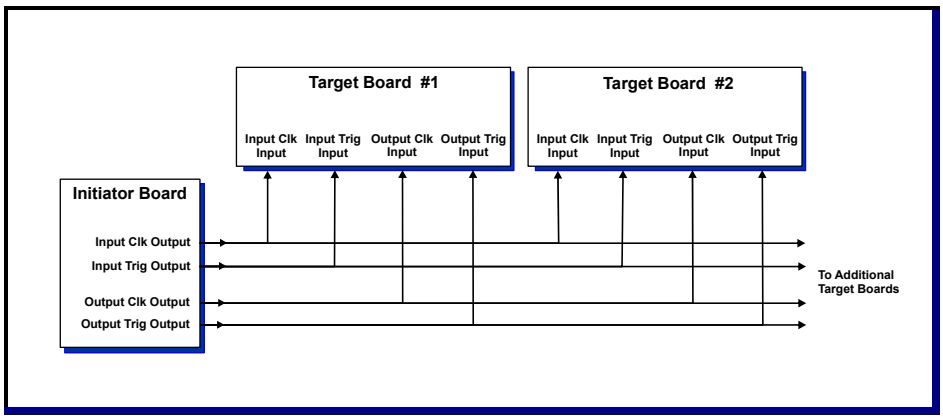

Figure 2.3-5. Multiboard Multidrop Synchronization

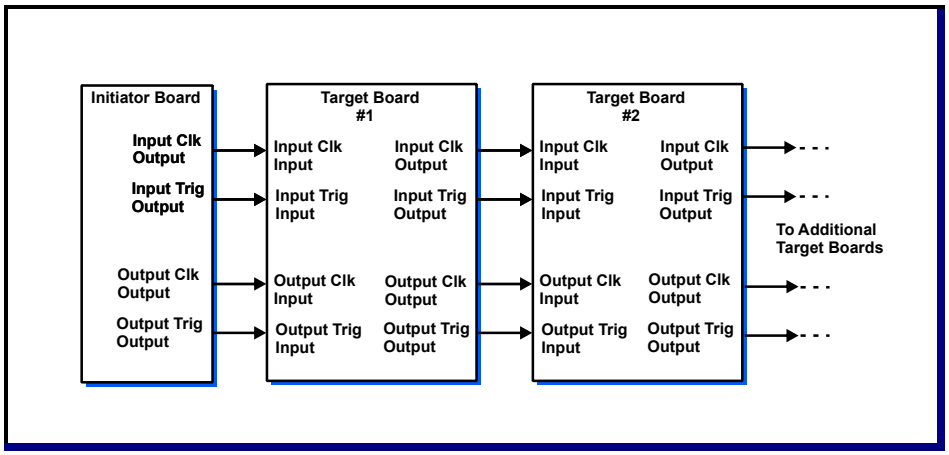

Figure 2.3-6. Multiboard Daisy-Chain Synchronization

The board that initiates the clock and trigger signals is software-designated as the **initiator**, and the clock and trigger receivers are designated as **targets**. The initiator and all targets should all reside in the same backplane. Standard TTL levels are used for all clock and trigger signaling.

2.3.4 External Sync I/O

An initiator (Paragraph 2.3.3) can be replaced with an external source of synchronization signals if the following conventions are observed:

- Logic levels are TTL. Input loading is less than 0.2ma. Maximum output loading is 10mA.
- Clocks and triggers are edge-detected and are asserted LOW (i.e.: falling edge).
- Minimum input pulse width is 120ns.

External devices can be synchronized to an initiator board by recognizing a clock or trigger event as a TTL logic-LOW pulse with a minimum width of 150ns.

2.4 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the range references. The optimum verification interval will vary with upon the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog channels are calibrated to a single internal voltage reference by an embedded autocalibration utility. The voltage reference is scaled for each of three basic input ranges, and a separate adjustment is provided for each range. The procedure presented here describes the verification and adjustment of the range references.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter, 5-1/2 digit, 0.002% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host board with available long PCI slot	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to the system I/O connector.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the three internal range references. Adjustment of the references, if necessary, is performed with three internal trimmer that are located as shown in Figure 2.5-1.

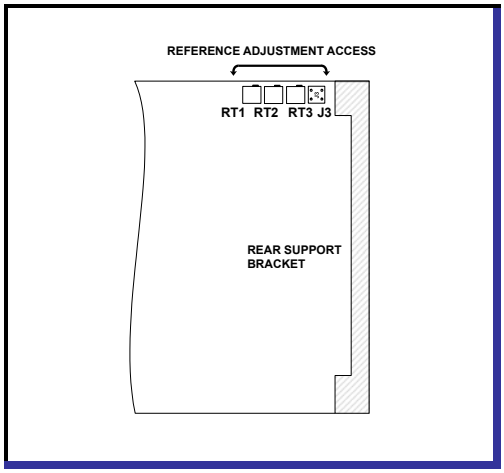

Figure 2.5-1. Reference Adjustment Access

This procedure assumes that the board under test is installed in an operational PCI host.

1. Connect the digital multimeter between the VTEST (+) pin and the VTEST RTN (-) pin in the system I/O connector (Table 2.2-1). Alternatively, use internal test connector J3 Pin-3(+) and J3 Pin-4(-).
2. If power has been removed from the board, apply power now. Wait at least 15 minutes after power is applied before proceeding.
3. Select the VREF Selftest input mode in the BCR.
4. For each input range listed in Table 2.5-2, select the input range in the Analog Input Configuration register (Table 3.4-1) and verify that the voltage displayed by the multimeter conforms to the Range Reference indicated for the range. If a reference does not conform to the table, adjust the associated trimmer to obtain a nominal in-range value.
5. Verification and adjustment is completed. Remove all test connections.

Table 2.5-2. Range Reference Voltages

Input Range	Range Reference	Adjustment Trimmer
±2.5V	+2.47500VDC ±0.00020VDC	RT1
±5V	+4.95000VDC ±0.00040VDC	RT2
±10V	+9.99000VDC ±0.00070VDC	RT3

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SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PCI66-18AISS8AO8 is compatible with the PCI Local Bus specification Revision 2.3, and supports auto configuration at the time of power-up. A PLX™ PCI-9056 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All data transfers are long-word D32. DMA access is supported for data transfers from the analog input buffer and to the analog output data buffers. To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero), and maintenance registers should not be modified.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2200 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	000X 000Xh	Digital I/O port data.	3.9
0008	(Reserved)	---	---	---	---
000C	CURRENT LOOP SELECT	RW	0000 0000h	Current loop selection mask.	3.5
0010	(Reserved)	---	---	---	---
0014	ANALOG INPUT CONFIG	RW	0000 02FFh	Analog input configuration.	3.4.1
0018	ANALOG INPUT BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0000 0180h	Rate-A generator divider; 24 bits.	3.7
0020	RATE GENERATOR B	RW	0000 2760h	Rate-B generator divider; 24 bits.	3.7
0024	AI BURST BLOCK SIZE	RW	0000 0400h	Analog input burst size.	3.4.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h`	Number of data values in the input buffer.	3.4.5
002C	INPUT BUFFER THRESHOLD	RW	0007 FFFEh	Input buffer status flag threshold.	3.4.5
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register	3.11
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.16
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1400h	Buffered Analog Outputs Control	3.14
0040	OUTPUT BUFFER THRESHOLD	RW	0007 FFFEh	Output buffer status flag threshold.	3.14.2.5
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.14.2.5
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.14.2
004C	RATE GENERATOR C	RW	0000 0180h	Rate-C generator divider; 24 bits.	3.7
0050	RATE GENERATOR D	RW	0000 2760h	Rate-D generator divider; 24 bits.	3.7
0054	ANALOG OUTPUT CONFIG	RW	0000 02FFh	Analog output configuration.	3.14.1
0054-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

3.2 Board Control Register (BCR)

Basic board functions such as initialization, autocalibration and input/output range selection are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Read-only status flags indicate the states of specific operational functions.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked. (Paragraph 3.3).
- All analog input and output channels are active. (3.4.2, 3.14.1.1).
- Analog input and output ranges are ±10V. (3.4.3, 3.14.1.2).
- Clock and trigger sources are internal. (3.4.4.3, 3.14.4, 3.14.5),
- The input and output buffers are reset to empty. (3.4.5.1, 3.14.2.5),
- Analog input and output data coding is offset binary. (3.6).
- The digital I/O port is configured as eight input lines. (3.9).
- Analog Inputs:
  - Input channels are differential. (3.4.1.1).
  - Sample clocking is from the Rate-A generator; Bursting is disabled. (3.4.4).
  - Burst block size is 1024 (0400h). (3.4.4.2).
  - The analog input buffer is reset to empty; buffer threshold is 3FFFEh. (3.4.5.2).
  - Current-loop terminators are disabled. (3.5)
  - The ADC Rate-A generator is adjusted to 105 kHz, and is disabled. (3.7),
  - The ADC Rate-B generator is adjusted to 4 kHz, and is disabled. (3.7),
- Analog Outputs:
  - Output configuration is single-ended. (3.7).
  - The DAC Rate-C generator is adjusted to 105 kHz, and is disabled. (3.7).
  - The DAC Rate-D generator is adjusted to 4 kHz, and is disabled. (3.7).
  - Analog outputs are at midrange (zero). (3.14.1.2).

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2200 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D07	RW	(Reserved)	0	---	---
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	3.4.4.2
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	3.4.4.2
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	3.4.5.1
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16-D17	RW	(Reserved)	0	---	---
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.14.4.2
D19	RW	(Reserved)	0	---	---
D20	RW	OUTPUT S/W CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.14.4.1
D21	RW	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.7
D22	R/W	ENABLE RATE-D GENERATOR	0	Enables the Rate-D generator for analog outputs.	3.7
D23	R/W	OUTPUT SW TRIGGER [3]	0	Output Burst S/W Trigger. See Table 3.14-2.	3.14.5.2
D24	RW	(Reserved)	0	---	---
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.6
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog inputs.	3.7
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for triggered bursts.	3.7
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.10
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.10
D30	R/W	ANALOG INPUT WARP MODE	0	Selects the analog input warp mode **required for sample rates greater than 400KSPS.**	3.7
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

3.4 Analog Inputs

Each of eight analog input channels can be digitized with 18-bit resolution at rates from DC to 500 Kilosamples per second. Data from any combination of inputs can be acquired in a 512K-sample buffer, and the associated channel number is attached to each active channel data value. Five input voltage ranges are available.

All active inputs are sampled simultaneously, and the sample clock can be derived: (a) from an internal rate generator, (b) from an external hardware clock input, or (c) directly from the bus.

To illustrate the requirements for initiating analog input acquisition directly after board initialization, setting the following control bits HIGH simultaneously in the BCR would start 8-channel acquisition using the Rate-A generator at the default sample rate:

- ENABLE INPUT BUFFER: Enables the analog input buffer.
- ENABLE RATE-A GENERATOR: Enables the Rate-A generator.

3.4.1 Input Modes

An input switching network routes either the system input signals or internal test signals through the input channels, and is controlled by the INPUT CONFIG control field in the Analog Input Configuration register (Table 3.4-1). The system inputs are disconnected when internal signals are monitored, and have no effect on test results.

3.4.1.1 System Inputs

Of the 16 possible input modes available through the INPUT CONFIG field, two are dedicated to system inputs. If differential system inputs are selected, the signal present between the HI and LO inputs in each channel is acquired. For a single-ended input, the input signal is measured between the HI input and the input return, and the LO input is ignored. The selected system input configuration must agree with the system wiring configuration (Section 2.3).

3.4.1.2 Test Modes

Internal analog nodes can be monitored to verify the functional integrity of the board. The selected input ranges apply in all input modes, including test modes. The following signals are present in *all input channels* when the indicated test modes are selected:

Zero Selftest:	Ideally equal to 0.000 VDC for bipolar ranges, or 86 (56h) counts for unipolar ranges,
VREF Selftest:	Internal voltage reference, ideally equal to +99.00 percent of the *selected analog input range*,
Output Channels:	Any single analog output channel. Differential outputs are developed between the HI(+) and LO(-) pins for any output channel.

3.4.2 Active Channels Selection

Input channels are designated as active by setting the corresponding INPUT XX control bit HIGH in the Analog Input Configuration register (Table 3.4-1), or as inactive by clearing the bit LOW. All active inputs are sampled simultaneously when a sample clock occurs. Inactive channels produce no data in the input buffer.

Table 3.4-1. Analog Input Configuration Register

Offset: 0014h **Default: 0000 02FFh**

BIT	MODE	DESIGNATION	DEF	DEF	REF
D00	RW	INPUT 00	1	Analog input Active Channel selection mask.	3.4.2
D01	RW	INPUT 01	1	HIGH to enable.	
D02	RW	INPUT 02	1		
D03	RW	INPUT 03	1		
D04	RW	INPUT 04	1		
D05	RW	INPUT 05	1		
D06	RW	INPUT 06	1		
D07	RW	INPUT 07	1		
D08-D10	RW	INPUT RANGE	2	Analog Input Range: 0 => ±2.5V. 1 => ±5V. 2 => ±10V 3 => 0 to +5V. 4 => 0 to +10V 5-7 => (Reserved).	3.4.3
D11	R/W	CLOCK TRIGGER OUT	0	Enables the Analog Input Clock and Trigger external outputs,	3.4.4.3
D12-D13	RW	CLOCK SOURCE	0	Analog Input clock source: 0 => Rate-A Generator. 1 => Rate-C Generator. 2 => Analog Input External Clock input 3 => (Reserved).	3.4.4
D14-D15	RW	TRIGGER SOURCE	0	Analog Input trigger source: 0 => Rate-B Generator. 1 => Rate-D Generator. 2 => Analog Input External Trigger input 3 => (Reserved).	3.4.4.2
D16-D20	RW	INPUT CONFIG	0	Analog Input Mode: 0 => Differential system inputs. 1 => Single-ended system inputs. 2 => ZERO Selftest. 3 => +VREF Selftest. 4-15 => (Reserved). 16 => Output Channel 00 HI (HI output pin) * 17 => Output Channel 01 HI 18 => Output Channel 02 HI 19 => Output Channel 03 HI 20 => Output Channel 04 HI 21 => Output Channel 05 HI 22 => Output Channel 06 HI 23 => Output Channel 07 HI 24 => Output Channel 00 LO (LO output pin) * 25 => Output Channel 01 LO 26 => Output Channel 02 LO 27 => Output Channel 03 LO 28 => Output Channel 04 LO 29 => Output Channel 05 LO 30 => Output Channel 06 LO 31 => Output Channel 07 LO	3.4.1.1 3.4.1.2
D21-D23	RW	(Reserved)	0	---	---
D24-D25	RW	GROUP-A FILTER	0	Group-A Input filter selection; Chan 00, 01, 04, 05: 0 => No filter. 1 => Select Filter-A. 2 => Select Filter-B. 3 => (Reserved)	3.4.6
D26-D27	RW	GROUP-B FILTER	0	Group-B Input filter selection: Same coding as Group-A; for Chan 02, 03, 06, 07.	3.4.6
D28-D31	RO	(Reserved)	0	---	---

* Differential outputs are developed between the HI(+) and LO(-) pins.

3.4.3 Input Ranges

An input voltage range of ±10V, ±5V, ±2.5V, 0/+10V or 0/+5V is assigned by the INPUT RANGE control field in the Analog Input Configuration register:

Note: Voltage levels outside the selected ranges will produce saturation codes of plus or minus fullscale, but will not damage the inputs if they are within the range indicated in the product specification for overvoltage protection.

3.4.4 Sampling Modes

All active channels are sampled at each occurrence of the analog input sample clock. The source of the input sampling clock is controlled by the CLOCK SOURCE control field in the Analog Input Configuration register, and the default source is the internal Rate-A generator. A software clock can be applied at any time by setting the INPUT S/W CLOCK control bit HIGH in the BCR. This bit overrides the existing CLOCK SOURCE selection, and clears automatically.

3.4.4.1 Continuous

During continuous sampling, all active input channels are sampled continuously as long as a clock source is present. Continuous sampling is selected when the ENABLE INPUT BURST control bit is LOW in the BCR.

3.4.4.2 Burst Sampling

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, an input trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired. Sampling then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit AI Burst Block Size control register (Table 3.1-1). The number of samples acquired in a burst *for each active channe*l equals the value contained in this register. The total number of samples acquired equals this value *times* the number of active channels.

Note: If a BURST BLOCK SIZE of zero is selected while bursting is enabled, a burst trigger initiates a nonterminating burst that continues until either the sample clock is disabled or the output buffer goes empty.

The END OF BURST status bit in the input buffer (Paragraph 3.4.5) is set HIGH for the last input value acquired in a burst. The INPUT BURST BUSY status flag in the BCR is HIGH during each triggered burst, and is LOW otherwise. *Input triggering cannot occur when INPUT BURST READY is LOW.*

The source of the input trigger is controlled by the TRIGGER SOURCE control field in the Analog Input Configuration register, and the default source is the internal Rate-B generator. A software trigger can be applied at any time by setting the INPUT S/W TRIGGER control bit HIGH in the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically.

3.4.4.3 Analog Inputs External Clock and Trigger

Selection of the External Clock Input configures the board as an ***Clock Target***, and sample clocks are supplied externally through the INPUT CLK INP pin in the system I/O connector. For any other clock selection, the board is designated a ***Clock Initiator***.

Selection of the External Trigger Input configures the board as an ***Trigger Target***, and burst triggers are supplied externally through the INPUT TRIG INP pin in the system I/O connector For any other trigger selection, the board is designated a ***Trigger Initiator***.

If the CLOCK TRIGGER OUT control bit is set HIGH, the INPUT CLK OUT and INPUT TRIG OUT pins in the I/O connector each generates an output pulse when the corresponding internal clock or trigger occurs. If this bit is LOW (default), the INPUT CLK OUT and INPUT TRIG OUT pins produce no output.

NOTE: For multiboard synchronization (3.8), an analog input clock or trigger initiator must have the CLOCK TRIGGER OUT control bit asserted. Likewise, all targets that drive other targets in a daisy-chain multiboard configuration (2.3.3) must have this bit asserted.

3.4.5 Input Data Buffer

3.4.5.1 Organization

Analog input data accumulates in the input data FIFO buffer until extracted by the PCI bus. The buffer has a capacity of 512K total samples, and contains an 18-bit data field, and an END OF BURST status bit and a 3-Bit INPUT CHANNEL NUMBER field (Table 3.4-2). Analog input data is right-justified to the LSB, and occupies bit positions D00 through D17.

The END OF BURST (EOB) status bit identifies the last data value in an input burst or function, and the INPUT CHANNEL NUMBER identifies the input channel associated with each value in the buffer.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant bit (LSB)
D01-D16	DATA01 - DATA16	Data value intermediate bits
D17	DATA17	Data value most significant bit (MSB)
D18	END OF BURST (EOB)	Identifies the last input value in a burst.
D19	(Reserved)	Returns zero.
D20-D22	INPUT CHANNEL NUMBER	Analog input channel number.
D23-D31	(Reserved)	Always zero.

NOTE: The input buffer capacity of 512K-samples is distributed among all active input channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 512K / Number of active channels.

In order for the input buffer to acquire input data, the ENABLE INPUT BUFFER control bit must be set HIGH in the BCR. The buffer can be cleared, or emptied, by writing a "one" to the CLEAR INPUT BUFFER control bit in the BCR. The CLEAR INPUT BUFFER bit clears automatically. An empty buffer returns an indeterminate value.

NOTE: To ensure that all input data is flushed from the data pipeline, a cleared buffer is held in a reset state for 4 microseconds. During this interval, the CLEAR INPUT BUFFER control bit remains HIGH and the input clock is disabled.

The INPUT BUFFER OVERFLOW status bit in the BCR is set HIGH if the buffer overflows, thereby indicating data loss. The status bit remains HIGH until cleared, either directly from the bus, by the CLEAR INPUT BUFFER control bit, or by a board reset.

3.4.5.2 Buffer Size and Threshold Registers

The Input Buffer Size control register listed in Table 3.1-1 contains the total number of data values present in the input buffer. The Input Buffer Threshold register (Table 3.4-3) specifies the buffer size value above which the INPUT BUFFER THRESHOLD FLAG is asserted HIGH. The threshold flag is duplicated in the BCR.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0007 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D19	RW	INPUT BUFFER THRESHOLD	7 FFFEh	Specifies the number of values in the input buffer, above which the threshold flag is asserted HIGH.
D20	RO	INPUT BUFFER THRESHOLD FLAG [1]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D21-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

3.4.6 Input Filters

The GROUP-A/B FILTER control fields in the Analog Input Configuration register select one of two 4th-order lowpass filters independently for each of two input channel groups. For each group, the options are "No filter", Filter-A or Filter-B. Filter types and frequencies are identified in the product specification, and standard frequencies are 80kHz for Filter-A and 200kHz for Filter-B. Group-A channels are 00, 01, 04, 05, and Group-B channels are 02, 03, 06, 07.

3.5 Current-Loop Analog Inputs

Each analog input channel can be configured to terminate an instrumentation current-loop with a loop termination resistor (Table 3.5-1).

Table 3.5-1. Current Loop Selection Register

Offset: 000Ch **Default: 0000 0000h**

BIT	MODE	DESIGNATION	DEF	DEF	REF
D00	RW	TERMINATOR 00	0	Analog input current-loop termination mask.	3.5
D01	RW	TERMINATOR 01	0	Terminator xx for input Channel xx.	
D02	RW	TERMINATOR 02	0	HIGH to enable (connect).	
D03	RW	TERMINATOR 03	0		
D04	RW	TERMINATOR 04	0		
D05	RW	TERMINATOR 05	0		
D06	RW	TERMINATOR 06	0		
D07	RW	TERMINATOR 07	0		
D08-D31	RW	(Reserved)	0	---	---

When selected, a termination resistor is connected directly across the associated analog input channel HI and LO input pins, and produces an input voltage equal to the resistor value times the loop current:

Input Voltage = Termination Resistance * Loop Current,

where resistance is expressed in Ohms and current in Amps. For example, a 0-20mA loop has a fullscale range of zero to 0.020 Amps. If the termination resistance is 500 Ohms (standard for this product), the corresponding input voltage range is 0V to +10V.

The absolute maximum safe input current for this product is determined by the termination resistor power rating (0.4 Watts), and the resistance:

Absolute Maximum Safe Loop Current = $\sqrt{}$ [0.4 Watt / resistance],

where **resistance** is in Ohms. For example, with a 500-Ohm termination resistance, the maximum safe loop current would be 28.3mA (square root of 0.4/500).

NOTE: Loop termination must not be enabled for input channels that might be exposed to voltages greater than ±15V unless the source current is limited to 30mA or less.

3.6 Data Coding Formats

Analog input and output data is arranged as 18 active right-justified data bits with the coding conventions shown in Figure 3.6-1. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

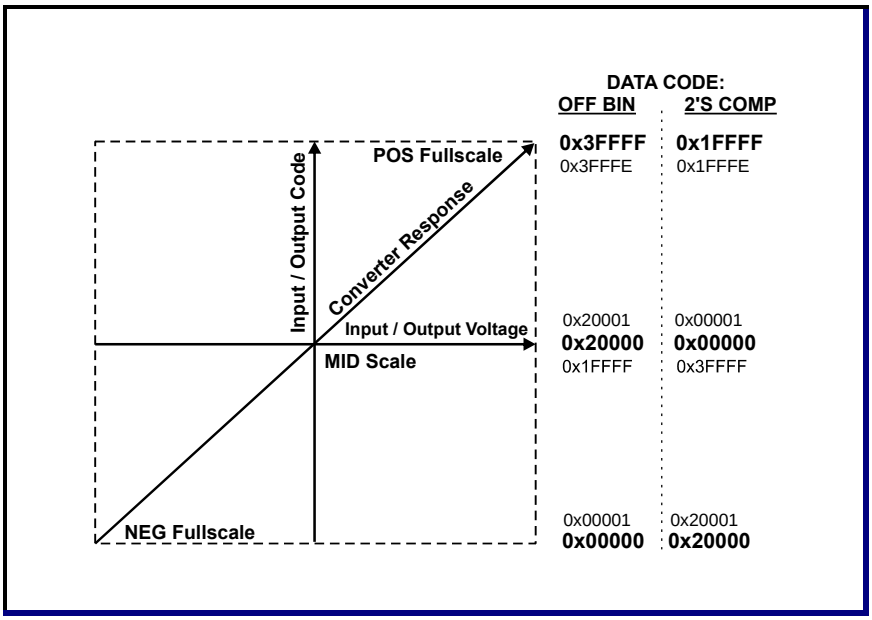

Figure 3.6-1. Analog Data Coding Formats; 18 Bit Data

3.7 Rate Generators

Four rate generators supply independent clock frequencies for ADC clocking and burst control. The Rate-A Generator shown in Table 3.7-1 generates an internal sample clock for the analog inputs. The Rate-B generator output can be used as a trigger source for input burst acquisition. Rate-C and Rate-D generators control analog output clocking and triggering.

Each generator is enabled by the associated ENABLE RATE-A/B/C/D GENERATOR control bit in the BCR. The generators are disabled when these bits are LOW.

Table 3.7-1. Rate Generator Registers (Rate-A,B,C,D)

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 0180 (Rate-A), 0000 2760h (Rate-B)**
Offset: 004Ch (Rate-C), 0050h (Rate-D) **Default: 0000 0180 (Rate-C), 0000 2760h (Rate-D)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

The frequency **Fgen** (Table 3.7-2) of each generator is calculated as:

Fgen = Fclk / Ndiv,

where **Fclk** is the master clock frequency for the board, and **Ndiv** is the value written to the Rate-A/B Generator register. **Fgen** and **Fclk** are both expressed in the same frequency units. **Fclk** is assumed here to be 40.320 MHz, but custom frequencies are available. If the master clock is provided with a custom frequency, **Fclk** equals the custom frequency. For an external clock or trigger input frequency, **Fclk** equals the external frequency, ***Fgen should not exceed the maximum sampling or clocking rate listed in the product specification.***

Table 3.7-2. Typical Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (40.320 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
126	007E	320,000
127	007F	317,480
128	0080	315,000
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv **

* ±0.003 percent. ** Fclk = master clock frequency; e.g.: 40.32MHz.

The maximum recommended analog input sample rate is 500,000 samples per second per channel, and the maximum recommended analog output clocking rate is 500,000 clocks per second.

NOTE: For analog input sampling rates greater than 400KSPS, the ANALOG INPUT WARP MODE control bit must be set HIGH in the BCR. When operating in warp mode, the minimum sample rate is 1 KSPS, and the first sample acquired from all active channels after a lapse of 1 millisecond or longer should be discarded.

3.8 Multiboard Synchronization

Analog input and output clocking and triggering can be synchronized among multiple boards by designating one of the boards as an ***initiator***, and the remaining boards as ***targets*** (Paragraphs 3.4.4.3, 3.14.4 and 3.14.5). In order to implement this function, the boards must be interconnected as described in Paragraph 2.3.3.

When multiple boards are configured as an initiator and multiple targets, the analog input clock, the analog input trigger, and the analog output clock generated in the initiator board are duplicated in the target boards with delays of less than 100 nanoseconds.

The board defaults to the analog input and output initiator modes, with the external clock and trigger outputs disabled (CLOCK TRIGGER OUT low in both the Analog Input and Output Configuration registers).

3.9 Digital I/O Port

The digital I/O port consists of eight bidirectional TTL I/O lines, with the corresponding data bits shown in Table 3.9-1. The DIO lines are arranged as two 4-bit nibbles, with the direction of each nibble controlled independently of the other. A nibble is an input to the board if the associated DIO 00 03 OUTPUT control bit is LOW, or is an output if the bit is HIGH. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the register. All digital I/O lines default to inputs.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 000X 000Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

3.10 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCI bus reset,
- Analog input or output range change.
- Changing the output configuration between single-ended and differential.
- Analog input or output clocking rate change of greater than 20-percent.

The analog inputs and outputs are autocalibrated on their selected ranges.

Note: Analog outputs are active during autocalibration, and vary between +fullscale and -fullscale during the calibration sequence.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a maximum duration of 8 seconds with single-ended outputs, or 15 seconds with differential outputs enabled (3.24.1.4). Completion of the operation can be detected either by monitoring the "Autocal completed" status flag in the Primary Status register (Table 3.11-1), or by simply waiting for a time interval sufficient to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.11 Primary Status Register

Critical status flags are consolidated into a single Primary Status register (Table 3.11-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit, *or by clearing the associated selection bit*.

NOTE: Response status bits can *only* be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

The response bit for an event indicated as 'edge-detected' is set HIGH when the event transitions from false to true. Once asserted, an edge-detected response bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

Real-time access to an edge-detected signal is available by reading the source of the edge-driven response bit (e.g.: INPUT BURST READY in the BCR is the signal that drives the "Analog Input Burst Initiated/Completed" response bits in the PSR).

Table 3.11-1 Primary Status Register

Offset 0x0030 **Default 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed [3]	D16	3.10
D01	Input Buffer threshold flag HIGH-to-LOW transition [3]	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition [3]	D18	
D03	Input Buffer Overflow [3]	D19	3.4.5.1
D04	Analog Input Burst Initiated (BURST BUSY LO-HI) [3]	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO) [3]	D21	
D06	Analog Input Clock [3]	D22	3.4.4
D07	Analog Output Clock [3]	D23	3.14.4
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition [3]	D24	3.9
D09	Output Buffer threshold flag HIGH-to-LOW transition [3]	D25	3.14.2.5
D10	Output Buffer threshold flag LOW-to-HIGH transition [3]	D26	
D11	Output Load-Ready Flag HIGH-to-LOW transition [3]	D27	3.14.3.3
D12	Output Load-Ready Flag LOW-to-HIGH transition [3]	D28	
D13	Analog Output Burst Ready [3]	D29	3.14.5.2
D14	Output Buffer Overflow or Frame Overflow [3]	D30	3.14.2.5 3.14.3.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Edge-detected event.

3.12 Buffer DMA Operation

2-Channel DMA transfers from the analog input buffer are supported with the board operating as a bus master. Table 3.12-1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9056 reference manual for a detailed description of these registers.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

The same register assignments apply to the analog output buffer, except the DMA Descriptor Counter value is revised to 0000 0000h to indicate a transfer direction from the PCI bus to the local bus.

Table 3.12-1. Typical Input Buffer DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

3.14 Analog Outputs

The eight analog output channels are controlled independently of the analog inputs, and are accessed through a dedicated analog output buffer. Once the outputs have been configured through the Analog Output Configuration register (Table 3.14-1), output operations are controlled through the Buffered Operations register (Table 3.14-3).

3.14.1 Output Configuration

3.14.1.1 Channel Selection

An output channel is selected as *active* by setting the corresponding OUTPUT_XX selection bit HIGH in the Analog Output Configuration register (Table 3.14-1) A channel is deselected to the *inactive* state by clearing the corresponding selection bit.

An active *channel group* consists of a single set of output values for all active channels. Only active output channels receive data from the output buffer. A channel that is deselected to the inactive state retains the last value that was received while the channel was still active. During initialization, all channels are designated as active and are set to an approximately zero output level.

3.14.1.2 Voltage Range Selection

An output voltage range of ±10V, ±5V, ±2.5V, 0/+10V or 0/+5V is assigned by the OUTPUT RANGE control field in the Analog Output Configuration register. The default output range is ±10V, and all ***outputs initialize to midrange (zero)***.

For maximum accuracy, autocalibration should be performed after a new output range is selected.

3.14.1.3 Clock and Trigger Sources

The clock and trigger source fields determine the origins of the analog output clock and trigger functions, and are described later in Sections 3.14.4 and 3.14.5, respectively.

3.14.1.4 Hardware Configuration

The analog outputs can be configured for either single-ended or balanced-differential operation, as selected in the OUTPUT CONFIG control field, and must agree with the system wiring configuration (Section 2.3.2.1).

Table 3.14-1. Analog Output Configuration Register

Offset: 0054h **Default: 0000 02FFh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	RW	OUTPUT 00	1	Analog output Active Channel selection mask. *	3.14.1.1
D01	RW	OUTPUT 01	1	HIGH to enable.	
D02	RW	OUTPUT 02	1		
D03	RW	OUTPUT 03	1		
D04	RW	OUTPUT 04	1		
D05	RW	OUTPUT 05	1		
D06	RW	OUTPUT 06	1		
D07	RW	OUTPUT 07	1		
D08-D10	RW	OUTPUT RANGE	2	Analog Output Range: 0 => ±2.5V. 1 => ±5V. 2 => ±10V 3 => 0 to +5V. 4 => 0 to +10V 5-7 => (Reserved).	3.14.1.2
D11	RW	CLOCK TRIGGER OUT	0	Enables the Analog Output Clock and Trigger external outputs,	3.14.4.1
D12-D13	RW	CLOCK SOURCE *	0	Analog Output clock source: 0 => Rate-C Generator. 1 => Rate-A Generator. 2 => Analog Output External Clock input 3 => (Reserved).	3.14.4
D14-D15	RW	TRIGGER SOURCE *	0	Analog Output trigger source: 0 => Rate-D Generator. 1 => Rate-B Generator. 2 => Analog Output External Trigger input 3 => (Reserved).	3.14.5
D16	RW	OUTPUT CONFIG	0	Analog Output Configuration: 0 => Single-ended outputs. 1 => Differential outputs.	3.14.1.4
D17	RW	(Reserved)	0	---	---
D18-D31	RO	(Reserved)	000h	---	---

3.14.2 Output Buffer

Analog output data from the PCI bus flows directly into the 512K-sample analog output FIFO data buffer (Table 3.14-2). From the buffer, the data passes through a short formatting pipeline to the analog output DAC channels.

NOTE: The output buffer capacity of 512 K-Samples is distributed among all active output channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 512K / Number of active channels.

3.14.2.1 Data Frame

A *data frame* consists of an integral number of channel groups. For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated as the *end-of-frame* (EOF) flag. The EOF designation is applied by setting the EOF flag HIGH when loading the last channel value into the buffer. Thereafter, the EOF flag follows the last channel value through the buffer.

Table 3.14-2. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only; Returns all-zero)**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D16	WO	DATA 01 - DATA 16	Intermediate data bits
D17	WO	DATA 17	Most significant data bit
D18	WO	EOF FLAG	End-of-frame (EOF) flag.
D19-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

3.14.2.2 Output Data Format

Analog output data values are written in 32-bit Lword-serial sequence from the PCI bus to the Analog Output Buffer. Bits D17..0 represent the output data value. Bit D18 designates the last value in a data frame, and is the end-of-frame (EOF) flag. The output buffer appears to the PCI bus as a 32-Bit single register, and a read-access to this register returns an all-zero value.

3.14.2.3 Output Data Coding

Analog output data coding is described in Paragraph 3.6.

Table 3.14-3. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_1400h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	R/W	(Reserved)	0h	---	---
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.14.4
D06	RO	OUTPUT CLOCK READY	0	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.14.4
D07	R/W	OUTPUT SW CLOCK *	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.14.4.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.14.2.7
D09	R/W	LOAD REQUEST *	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.14.3.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.14.3.3
D11	R/W	CLEAR OUTPUT BUFFER *	0	Resets the output buffer to empty.	3.14.2.5
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.14.2.5
D13	RO	OUTPUT BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.14.2.5
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.14.2.5
D16	R/W	AO BUFFER OVERFLOW	0	Set HIGH when data is written to a full buffer. **	3.14.2.5
D17	R/W	FRAME OVERFLOW	0	Set HIGH when data is written to a closed buffer. **	3.14.2.5
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.14.5.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.14.5.2
D20	R/W	OUTPUT SW TRIGGER *	0	Produces a single output trigger event when asserted. Clears LOW automatically when the clock event is completed. Independent of triggering mode. Duplicated in the BCR.	3.14.5.2
D21-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

* Clears LOW automatically when operation is completed.
** Remains HIGH until cleared by a direct write as LOW, or by initialization.

3.14.2.4 Buffer Loading

Channel data values are loaded into the output buffer in ascending order of the active channels. The channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Figure 3.14-1 illustrates a loading example that implements two output channels, with 100 values per channel. Each channel group in this example consists of active channels 0 and 5.

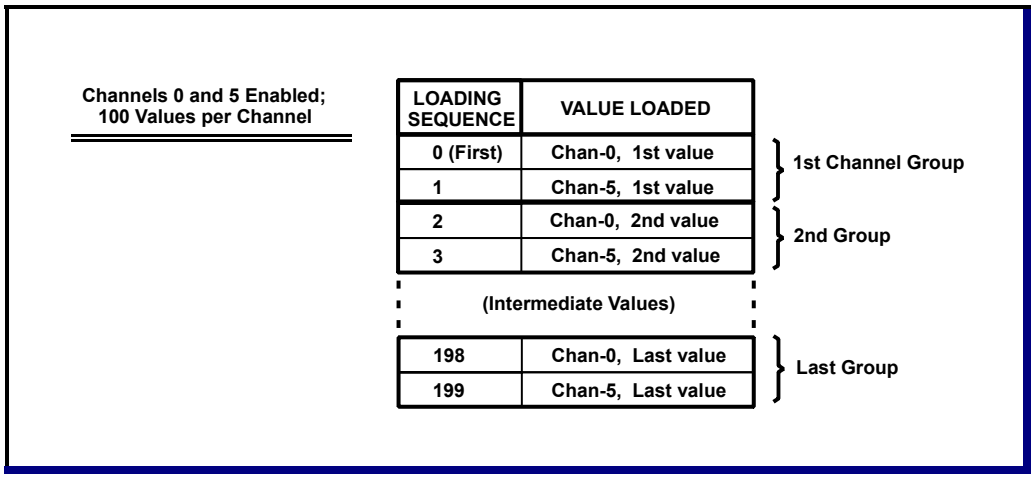

Figure 3.14-1. Typical Buffer Loading Sequence

NOTE: Data can be loaded from the PCI bus to the output buffer only if the buffer is open; that is, not circular or closed (3.14.2.4).

3.14.2.5 Output Buffer Control

The Buffered Output Operations register in Table 3.14-3 controls and monitors the flow of data through the analog output data buffer. Asserting the CLEAR OUTPUT BUFFER control bit HIGH clears, or empties, the buffer.

The AO BUFFER OVERFLOW flag is set HIGH if data is written to a full buffer, and the FRAME OVERFLOW flag indicates that an attempt was made to write data to a closed buffer. Both flags indicate data loss. Each of these flags, once set, remains HIGH until written LOW directly from the bus, or by initialization .

The AO BUFFER EMPTY flag indicates that the buffer contains no output data. The AO BUFFER FULL flag is asserted when the buffer is full. Data written to a full output buffer is discarded.

The Output Buffer Size register shown in Table 3.14-4 contains the number of output data values present in the buffer, and like the Input Buffer Size register, and is updated continuously.

Table 3.14-4. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D19	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D20-D31	RO	(Inactive)	0	---

The Output Buffer Threshold register in Table 3.14-5 specifies the buffer size value above which the OUTPUT BUFFER THRESHOLD FLAG is asserted HIGH. This status flag is duplicated in the Buffered Output Operations register.

Table 3.14-5. Output Buffer Threshold Register

Offset: 0040h **Default: 0007 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D19	RW	OUTPUT BUFFER THRESHOLD	7 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D20	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D21-D31	RO	Reserved	0	---

3.14.2.6 Open Buffer

If the CIRCULAR BUFFER control bit is LOW in the buffer operations register, the output buffer operates in the open mode. Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing, and will empty itself unless it is replenished from the PCI bus. This mode of operation permits the continuous flow of data from the PCI bus to the analog outputs.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.14-2 illustrates the movement of a single data frame through an open buffer.

3.14.2.7 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the PCI bus.

In Figure 3.14-3 a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

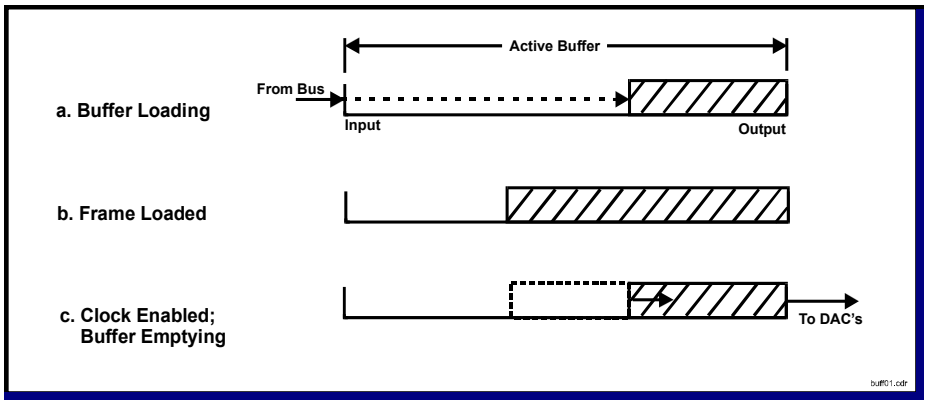

Figure 3.14-2. Open Buffer Data Flow

An end-of-frame (EOF) flag identifies the end-point, or last value in a data frame, and is set HIGH when the last value is loaded. Multiple contiguous burst functions, or frames, can reside in the buffer simultaneously.

NOTE: Disable output clocking before loading the buffer for circular operation.

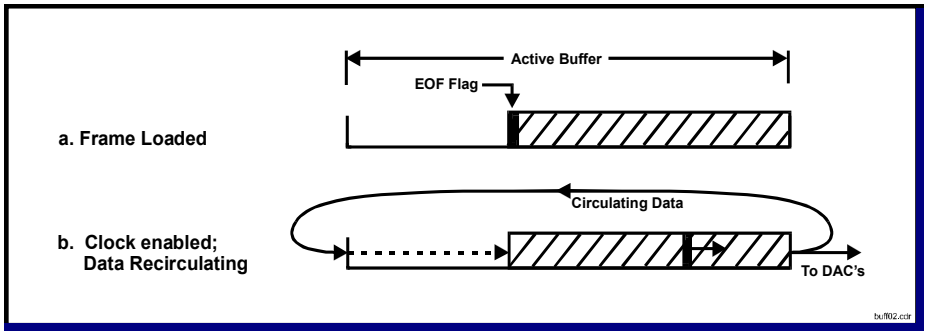

Figure 3.14-3. Circular Buffer Data Flow

3.14.3 Function Generation

3.14.3.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous sampling and circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly.

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform is retained in the buffer and can be reproduced repeatedly by subsequent triggers.

3.14.3.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions are flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions are retained in the buffer, and the series of functions is repeated indefinitely. .

3.14.3.3 Function Sequencing (Concatenation)

A new function (data frame) can be concatenated to the end of an existing function in a circular buffer, while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output.

Introduction of a new function commences by setting the LOAD REQUEST flag HIGH in the buffered output operations register, and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag attached to the final value. When the last value in the original function is clocked from the buffer, the accompanying EOF flag causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. Notice that the loading of the new function into the buffer must be completed before the existing function terminates.

In Figure 3.14-4, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

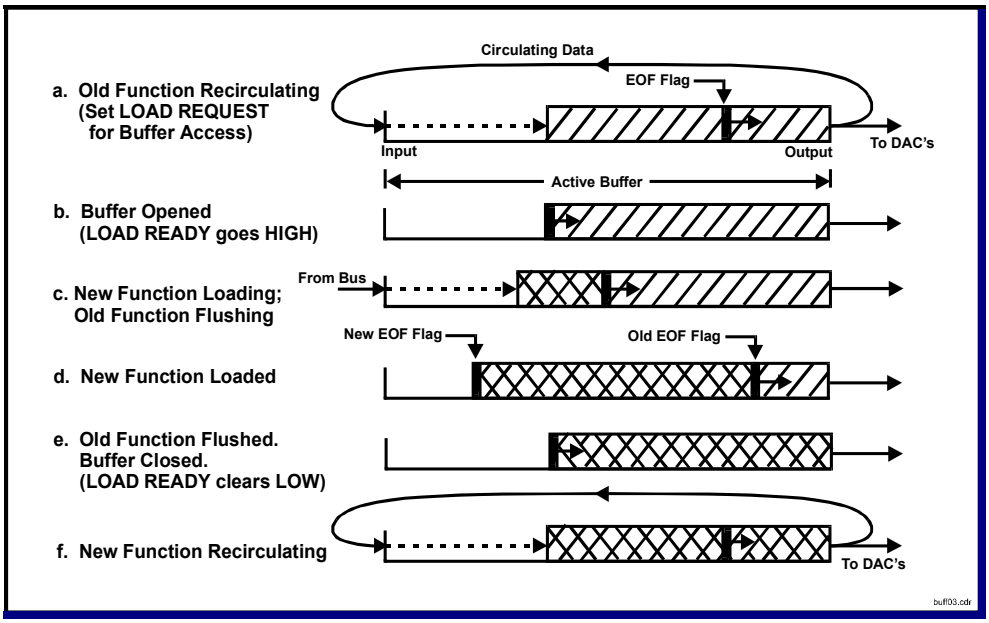

Figure 3.14-4. Function Sequencing

NOTE: If the loading of a new function extends beyond the LOAD-READY interval, the FRAME OVERFLOW flag is set HIGH in the Buffer Operations register, indicating data loss. Once set, this flag remains HIGH until written LOW directly from the bus, or by initialization

After loading the new function, allow the LOAD REQUEST control bit to be cleared automatically. This bit should not be cleared from the PCI bus.

3.14.4 Output Clocking

Each occurrence of the output clock updates either one or all of the active output channels, depending on whether sequential or simultaneous clocking (3.14.4.2, 3.14.4.3) is selected in the BCR.

Output clocking is enabled by setting the ENABLE OUTPUT CLOCKING control bit HIGH in the Buffered Output Operations register and enabling the associated clock source. The OUTPUT CLOCKING READY status bit indicates that an output clock will be accepted. This status bit is LOW during reset operations or autocalibration.

3.14.4.1 Clock Source

The source of the analog output clock is controlled by the CLOCK SOURCE control field in the Analog Output Configuration register, and the default source is the internal Rate-C generator. A software clock can be applied at any time by setting the OUTPUT S/W CLOCK control bit HIGH in either the Buffered Output Operations register or the BCR. This bit overrides the existing CLOCK SOURCE selection, and clears automatically.

If the CLOCK TRIGGER OUT control bit is set HIGH in the Analog Output Configuration register, the OUTPUT CLK OUT and OUTPUT TRIG OUT pins in the I/O connector each generates an output pulse when the corresponding internal clock or trigger occurs. If this bit is LOW (default), the OUTPUT CLK OUT and OUTPUT TRIG OUT pins produce no output.

3.14.4.1.1 External Clock

The external clock source at the OUTPUT CLK INP system I/O connector pin can have any frequency up to the maximum value specified for the output clocking rate. When the external clock source is selected, sampling occurs on a HIGH-to-LOW transition of the external analog output clock.

3.14.4.1.2 Internal Output Rate Generator

The internal Rate-C generator provides an output clocking rate that is adjustable as described in Paragraph 3.7. The Rate-C generator is enabled by setting the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.

3.14.4.2 Simultaneous Clocking

Simultaneous sampling is selected by setting the SIMULTANEOUS OUTPUTS control bit HIGH in the BCR. If simultaneous sampling is selected, the analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the sampling clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective sample rate for each channel equals the output clocking rate.

3.14.4.3 Sequential Operation

Sequential sampling is selected when the SIMULTANEOUS OUTPUTS control bit in the board control register is LOW. At each clock occurrence in sequential operation, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately. Channel values are read from the buffer beginning with the lowest-numbered active channel in a channel group, and proceeding upward through the highest-numbered active channel. When operating in this mode, the effective sample rate for each channel equals the output clocking rate *divided by the number of active channels*.

3.14.5 Sampling Mode

3.14.5.1 Continuous Sampling

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is LOW (default), the *continuous sampling* mode is selected and data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that an output clock is present. EOF flags are ignored when operating in this mode.

3.14.5.2 Data Bursts

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is HIGH, burst operation is selected. During a *triggered output burs*t, data is transferred continuously from the output buffer to the analog outputs until either the ***buffer goes empty, or an end-of-frame (EOF) flag is encountered***. In the triggered-burst sampling mode, an internal or external output trigger initiates the transfer of data from the output buffer to the output channels. The BURST READY status flag indicates that a burst trigger will be accepted, and is LOW during each burst.

The source of the output trigger is controlled by the TRIGGER SOURCE control field in the Analog Output Configuration register, and the default source is the internal Rate-D generator. A software trigger can be applied at any time by setting the OUTPUT S/W TRIGGER control bit HIGH in either the Buffer Operations register or the BCR. This bit overrides the existing CLOCK TRIGGER selection, and clears automatically. The OUTPUT SW TRIGGER bit goes HIGH during the burst, and clears automatically when the burst is completed.

If the CLOCK TRIGGER OUT control bit is set HIGH in the output configuration register, the OUTPUT CLK OUT and OUTPUT TRIG OUT pins in the I/O connector each generates an output pulse when the corresponding internal clock or trigger occurs. If this bit is LOW (default), the OUTPUT CLK OUT and OUTPUT TRIG OUT pins produce no output.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (3.14.2.1). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

3.14.5.3 Internal Output Trigger Generator

The internal Rate-D generator provides an internal trigger that is adjustable as described in Paragraph 3.7. The Rate-D generator is enabled by setting the ENABLE RATE-D GENERATOR control bit HIGH in the BCR.

3.14.6 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering (Common burst trigger)
c. Synchronous clocking (Common DAC clock)
d. Synchronous clocking and burst triggering (Common trigger and DAC clock).

As many as four boards can be synchronized together when connected in the Multidrop configuration (2.3.3), or any number can be synchronized together in the Daisy-Chain configuration. External clock and trigger I/O signaling (2.3.4) uses standard TTL levels.

NOTE: For multiboard synchronization, an analog output clock or trigger initiator must have the CLOCK TRIGGER OUT control bit asserted. Likewise, all targets that drive other targets in a daisy-chain multiboard configuration (2.3.3) must have this bit asserted.

3.15 Buffered Analog Output Application Examples

Specific operating modes and procedures vary widely according to the unique requirements of each application. The examples presented in this section illustrate basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally apply to a single output channel for simplicity of explanation. However, each active channel represents an independent set of function values, and all channels share a common output clock.

Table 3.15-1. Summary of Operation Examples

Operation Example	Description
Sequential Direct Outputs	Each value written to the output data buffer updates the associated analog output channel when clocked, independently of the other channels.
Simultaneous Direct Outputs	Data values accumulate in the output data buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously when clocked.
Continuous Function	An extension of Simultaneous Direct Outputs, in which the buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.15-2 have already been performed.

Table 3.15-2. Initial Operations

Operation	Default Value	Applicable Paragraph
The board has been reset or initialized.	---	3.3.2
The active channel group has been defined .	All channels active	3.14.1.1
The required output coding has been selected.	Offset binary	3.6

The remaining operational parameters are assumed to be in the following *default* states initially:

Parameter	Default
Buffer mode:	Open
Buffer status:	Empty
Sample rate:	105KSPS
Sampling mode:	Sequential

Parameter	Default
Clock source:	Rate-C Generator
Clock status:	Disabled
Trigger source:	Rate-D Generator
Trigger status:	Disabled

3.15.1 Sequential Direct Outputs

Table 3.15-3. Sequential Direct Outputs Example

Operation	PCI Bus Action	Board Response
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Load the output value for the first active channel.	Write the first value to the output data buffer.	Output value appears immediately (when clocked) at the analog output.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active analog outputs are updated in ascending sequence.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	Each value written to the buffer is transferred immediately to the associated analog output when clocked

Notes:
1. End-of-frame (EOF) flags are ignored when operating in the open-buffer mode. Only D17..0 are active in the output buffer.
2. Data written to the buffer at rates above 500KSPS will accumulate in the buffer.
3. Access to an individual output channel is accomplished by first selecting (enabling) only the specific channel, and by then writing the output value to the buffer.

3.15.2 Simultaneous Direct Outputs

Table 3.15-4. Simultaneous Direct (Single Group) Outputs Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the BCR.	Simultaneous clocking is selected.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the output value for the first active channel.	Write the first value to the output data buffer.	First value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining values are accumulated in the buffer. When the last value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

Notes: 1. Data written to the buffer at rates above 500KSPS will accumulate in the buffer.

3.15.3 Continuous Function

Table 3.15-5. Continuous Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Set the buffer threshold flag to 1/4 of the expected block size.	Write 1/4 block size to the threshold register (Table 3.14-5).	The threshold flag will go LOW when the buffer contents drop below the threshold.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the selected rate. The internal rate generator is enabled, if internal clocking is required.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Write a block of values to all active channels. To avoid discontinuities in the output functions, the effective loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 40MSPS during DMA transfers.	Write function values for all active channels to the output data buffer.	All active channels produce their respective output functions.
Wait for the buffer threshold flag to go LOW. (See Note 1).	Monitor the analog output buffer threshold flag until LOW.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:
1. Response to the flag must be fast enough to prevent the buffer from going empty.

3.15.4 Periodic Function

Table 3.15-6. Periodic Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. (Note 1) Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Select the circular buffer mode.	Set CIRCULAR BUFFER in the buffer operations register.	The output buffer is closed (circular).
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:
1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.15.5 Function Burst

Table 3.15-7. Function Burst Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
Select the clocking rate.	Write the required sample clocking rate to the Rate-C generator control register.	The output clocking rate is selected.
Select the triggering rate.	Write the required triggering rate to the Rate-D generator control register.	The burst triggering rate is selected.
Select triggered-burst mode.	Set ENABLE OUTPUT BURST in the buffer operations register.	The triggered-burst operating mode is selected.
Prepare the buffer operations register for burst mode:	Write to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING.	Output clocking is enabled.
Enable the internal rate generators.	Set the ENABLE RATE-C and RATE-D GENERATOR control bits in the BCR.	Required internal rate generators are enabled.
For external burst triggering, or internal rate-generator triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each trigger.

3.15.6 Function Sequencing (Concatenation)

Table 3.15-8. Function Sequencing Example

Operation	PCI Bus Action	Board Response
Establish a periodic function as described in Paragraph 3.15.4. The following operations will replace the original ('old') function in each channel with a new function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request buffer access	Set LOAD REQUEST in the buffer operations register.	The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Monitor the LOAD READY status flag. The buffer is open when this flag goes HIGH.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode after the last data value in the original function set leaves the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes.

3.16 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.16-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved bit field)
D16	Number of analog input channels: 0 => 8 Input and 8 output channels. 1 => 4 input and 4 output channels.
D17	Total Effective Buffer Capacitor: 0 => 4 MByte effective capacity. 1 => 2 MByte effective capacity.
D18-D19	Analog Input filter frequency: 0 => Filter-A = 80kHz, Filter-B = 200kHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D20-D21	Master Clock frequency: 0 => 40.320 MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D22-D31	(Reserved bit field; returns all-zero).

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of eight analog input channels contains a selftest input switching network, a selectable current-loop terminator, a differential amplifier, a scaling network and filter, and an 18-Bit ADC (Figure 4.1-1). Input ranges are software-selectable as ±10V, ±5V, ±2.5V, 0/+10V or 0/+5V, independently of the selected output range. A 512K-sample FIFO buffer accumulates analog input data for subsequent retrieval through the PCI bus.

Eight 18-bit analog output channels provide software-selected output ranges of ±10V, ±5V, ±2.5V, 0/+10V or 0/+5V and, like the analog inputs, are accessed through a dedicated 512K-sample FIFO buffer. An 8-Bit digital port is configured as two independently controlled sets of four bidirectional I/O lines.

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller, and supports universal signaling. +5 VDC power from the PCI bus is converted into regulated power voltages for the internal analog networks.

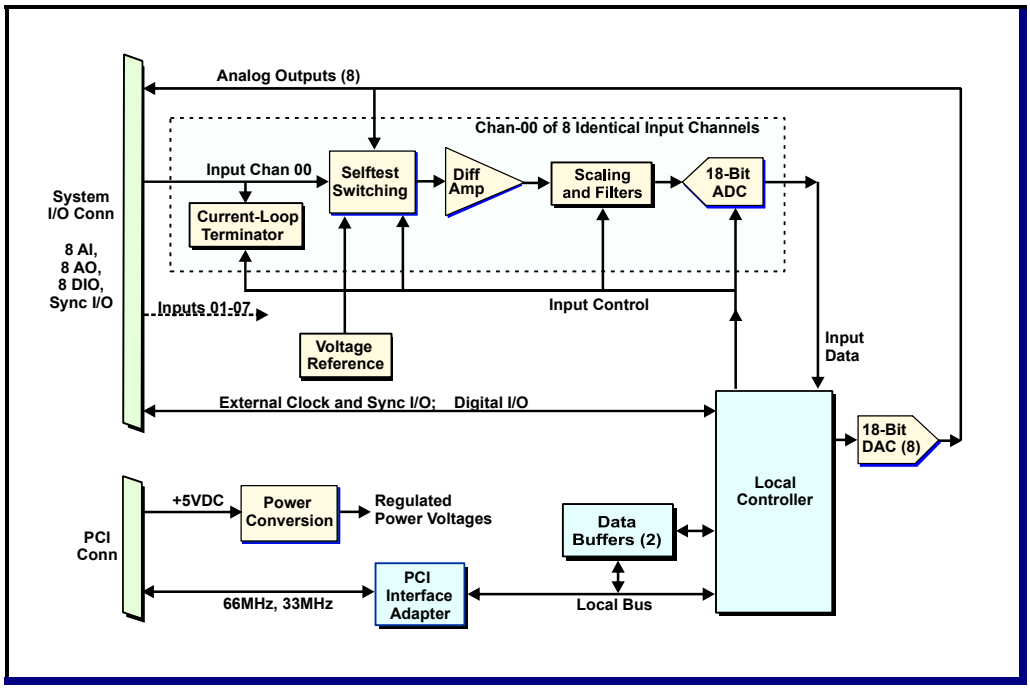

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input and output channels, and can be configured to accept either differential or single-ended system inputs.

Analog input sampling and output clocking on multiple target boards can be synchronized to a single software-designated initiator board.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, eight 18-bit ADC's receive single-ended or differential system analog input signals from the system I/O connector. For integrity testing and autocalibration operations, an internal voltage reference and the analog outputs can be routed through the selftest switches to the ADC's. An attenuator in each channel provides the necessary scaling for software-controlled input ranging.

Serial data from each ADC is deserialized and multiplexed into a continuous data stream within the local controller. The output of the multiplexer passes through a digital processor that applies gain and offset correction values obtained during autocalibration. The final processed and formatted data is loaded into the analog input data buffer.

ADC clocking can be supplied either from an internal 24-Bit rate divider operating from the master clock, or from an external source. Triggered bursts can be acquired by using a second internal rate generator or an external input as a trigger source. The burst block-size can be controlled by a 24-Bit counter, or sampling can be configured to operate continuously after a trigger.

4.3 Analog Outputs

Eight independent 18-bit DAC's are controlled through a dedicated 512 Ksample FIFO buffer. The buffer can be operated either open for data streaming, or closed (circular) for periodic function generation. Function concatenation from the PCI bus is supported. The output configuration can be selected as either single-ended or balanced differential.

Each 18-bit DAC consists of a 2-bit high-order DAC and a 16-Bit low-order DAC. The 2-bit DAC has a weighting factor equal to four times that of the 16-Bit DAC, which effectively serves as a 16-bit vernier for each of the upper four states. All four states of the 2-Bit DAC are calibrated individually during autocalibration, and then are dynamically corrected in real-time during operation. The 16-bit DAC is calibrated statically to occupy precisely one state of the 2-Bit DAC.

Output clocking and triggering can be supplied: (a) from two internal 24-Bit analog output rate generators, (b) from the analog input rate generators, or (c) from an external source. Triggered bursts, or functions, are supported. The output burst size is controlled by a tag-bit attached to the last output value in a sequence. If the tag-bit is not attached, a burst will operate continuously after a trigger, or until the buffer goes empty.

4.4 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input and output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is used to calibrate the span of each input channel, and a zero-reference is used to calibrate the offset value. These same two points in input channel-00 are then used to calibrate all eight output channels. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.5 Power Control

Regulated power voltages of ±5 VDC and ±14 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

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APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

OFFSET (Hex)	REGISTER	MODE	DEFAULT	PRIMARY FUNCTION	REF
0000	BOARD CONTROL	RW	2200 0000h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	000X 000Xh	Digital I/O port data.	3.9
0008	(Reserved)	---	---	---	---
000C	CURRENT LOOP SELECT	RW	0000 0000h	Current loop selection mask.	3.5
0010	(Reserved)	---	---	---	---
0014	ANALOG INPUT CONFIG	RW	0000 02FFh	Analog input configuration.	3.4.1
0018	ANALOG INPUT BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0000 0180h	Rate-A generator divider; 24 bits.	3.7
0020	RATE GENERATOR B	RW	0000 2760h	Rate-B generator divider; 24 bits.	3.7
0024	AI BURST BLOCK SIZE	RW	0000 0400h	Analog input burst size.	3.4.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h`	Number of data values in the input buffer.	3.4.5
002C	INPUT BUFFER THRESHOLD	RW	0007 FFFEh	Input buffer status flag threshold.	3.4.5
0030	PRIMARY STATUS	RW	0000 0000h	Principal status-flag register	3.11
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.16
0038	Autocal Values *	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1400h	Buffered Analog Outputs Control	3.14
0040	OUTPUT BUFFER THRESHOLD	RW	0007 FFFEh	Output buffer status flag threshold.	3.14.2.5
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	3.14.2.5
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.14.2
004C	RATE GENERATOR C	RW	0000 0180h	Rate-C generator divider; 24 bits.	3.7
0050	RATE GENERATOR D	RW	0000 2760h	Rate-D generator divider; 24 bits.	3.7
0054	ANALOG OUTPUT CONFIG	RW	0000 02FFh	Analog output configuration.	3.14.1
0054-007C	(Reserved)	---	---	---	---

* Maintenance register; Shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2200 0000h**

BIT	MODE [1]	DESIGNATION	DEF	DESCRIPTION	REF
D00-D07	RW	(Reserved)	0	---	---
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	3.4.4.2
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	3.4.4.2
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	3.4.5.1
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16-D17	RW	(Reserved)	0	---	---
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, each output is updated immediately when new data is received.	3.14.4.2
D19	RW	(Reserved)	0	---	---
D20	RW	OUTPUT S/W CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.14.4.1
D21	RW	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.7
D22	R/W	ENABLE RATE-D GENERATOR	0	Enables the Rate-D generator for analog outputs.	3.7
D23	R/W	OUTPUT SW TRIGGER [3]	0	Output Burst S/W Trigger. See Table 3.14-2.	3.14.5.2
D24	RW	(Reserved)	0	---	---
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.6
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog inputs.	3.7
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for triggered bursts.	3.7
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.10
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.10
D30	R/W	ANALOG INPUT WARP MODE	0	Selects the analog input warp mode **required for sample rates greater than 400KSPS.**	3.7
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Analog Input Configuration Register

Offset: 0014h **Default: 0000 02FFh**

BIT	MODE	DESIGNATION	DEF	DEF	REF
D00	RW	INPUT 00	1	Analog input Active Channel selection mask.	3.4.2
D01	RW	INPUT 01	1	HIGH to enable.	
D02	RW	INPUT 02	1		
D03	RW	INPUT 03	1		
D04	RW	INPUT 04	1		
D05	RW	INPUT 05	1		
D06	RW	INPUT 06	1		
D07	RW	INPUT 07	1		
D08-D10	RW	INPUT RANGE	2	Analog Input Range: 0 => ±2.5V. 1 => ±5V. 2 => ±10V 3 => 0 to +5V. 4 => 0 to +10V 5-7 => (Reserved).	3.4.3
D11	R/W	CLOCK TRIGGER OUT	0	Enables the Analog Input Clock and Trigger external outputs,	3.4.4.3
D12-D13	RW	CLOCK SOURCE	0	Analog Input clock source: 0 => Rate-A Generator. 1 => Rate-C Generator. 2 => Analog Input External Clock input 3 => (Reserved).	3.4.4
D14-D15	RW	TRIGGER SOURCE	0	Analog Input trigger source: 0 => Rate-B Generator. 1 => Rate-D Generator. 2 => Analog Input External Trigger input 3 => (Reserved).	3.4.4.2
D16-D20	RW	INPUT CONFIG	0	Analog Input Mode: 0 => Differential system inputs. 1 => Single-ended system inputs. 2 => ZERO Selftest. 3 => +VREF Selftest. 4-15 => (Reserved). 16 => Output Channel 00 HI (HI output pin) * 17 => Output Channel 01 HI 18 => Output Channel 02 HI 19 => Output Channel 03 HI 20 => Output Channel 04 HI 21 => Output Channel 05 HI 22 => Output Channel 06 HI 23 => Output Channel 07 HI 24 => Output Channel 00 LO (LO output pin) * 25 => Output Channel 01 LO 26 => Output Channel 02 LO 27 => Output Channel 03 LO 28 => Output Channel 04 LO 29 => Output Channel 05 LO 30 => Output Channel 06 LO 31 => Output Channel 07 LO	3.4.1.1 3.4.1.2
D21-D23	RW	(Reserved)	0	---	---
D24-D25	RW	GROUP-A FILTER	0	Group-A Input filter selection; Chan 00, 01, 04, 05: 0 => No filter. 1 => Select Filter-A. 2 => Select Filter-B. 3 => (Reserved)	3.4.6
D26-D27	RW	GROUP-B FILTER	0	Group-B Input filter selection: Same coding as Group-A; for Chan 02, 03, 06, 07.	3.4.6
D28-D31	RO	(Reserved)	0	---	---

* Differential outputs are developed between the HI(+) and LO(-) pins.

Table 3.5-1. Current Loop Selection Register

Offset: 000Ch **Default: 0000 0000h**

BIT	MODE	DESIGNATION	DEF	DEF	REF
D00	RW	TERMINATOR 00	0	Analog input current-loop termination mask.	3.5
D01	RW	TERMINATOR 01	0	Terminator xx for input Channel xx.	
D02	RW	TERMINATOR 02	0	HIGH to enable (connect).	
D03	RW	TERMINATOR 03	0		
D04	RW	TERMINATOR 04	0		
D05	RW	TERMINATOR 05	0		
D06	RW	TERMINATOR 06	0		
D07	RW	TERMINATOR 07	0		
D08-D31	RW	(Reserved)	0	---	---

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

DATA BIT	DESIGNATION	DESCRIPTION
D00	DATA00	Data value least significant bit (LSB)
D01-D16	DATA01 - DATA16	Data value intermediate bits
D17	DATA17	Data value most significant bit (MSB)
D18	END OF BURST (EOB)	Identifies the last input value in a burst.
D19	(Reserved)	Returns zero.
D20-D22	INPUT CHANNEL NUMBER	Analog input channel number.
D23-D31	(Reserved)	Always zero.

Table 3.4-3. Input Buffer Threshold Register

Offset: 002Ch **Default: 0007 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D19	RW	INPUT BUFFER THRESHOLD	7 FFFEh	Specifies the number of values in the input buffer, above which the threshold flag is asserted HIGH.
D20	RO	INPUT BUFFER THRESHOLD FLAG [1]	0	HIGH when the number of values in the input buffer exceeds the specified buffer threshold.
D21-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

Table 3.7-1. Rate Generator Registers (Rate-A,B,C,D)

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 0180 (Rate-A), 0000 2760h (Rate-B)**
Offset: 004Ch (Rate-C), 0050h (Rate-D) **Default: 0000 0180 (Rate-C), 0000 2760h (Rate-D)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

* R/W = Read/Write, RO = Read-Only.

Table 3.7-2. Typical Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (40.320 MHz Master Clock)*
(Dec)	(Hex)	(Hz)
126	007E	320,000
127	007F	317,480
128	0080	315,000
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv **

* ±0.003 percent. ** Fclk = master clock frequency; e.g.: 40.32MHz.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 000X 000Xh**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00	RW	DIO 00 DATA	X	Digital I/O Data; Bits 00-03
D01	RW	DIO 01 DATA	X	
D02	RW	DIO 02 DATA	X	
D03	RW	DIO 03 DATA	X	
D04-D06	RW	(Reserved)	0h	---
D07	R/W	DIO 00_03 OUTPUT	0	DATA 00-03 direction control; High for output.
D08	RW	DIO 04 DATA	X	Digital I/O Data; Bits 04-07
D09	RW	DIO 05 DATA	X	
D10	RW	DIO 06 DATA	X	
D11	RW	DIO 07 DATA	X	
D12-D14	RW	(Reserved)	0h	---
D15	RW	DIO 04_07 OUTPUT	0	DATA 04-07 direction control; High for output.
D16-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.11-1 Primary Status Register

Offset 0x0030 **Default 0000 0000h**

SELECTION BIT [1]	CRITICAL EVENT	RESPONSE BIT [2]	REFERENCE PARAGRAPH
D00	Autocal completed [3]	D16	3.10
D01	Input Buffer threshold flag HIGH-to-LOW transition [3]	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition [3]	D18	
D03	Input Buffer Overflow [3]	D19	3.4.5.1
D04	Analog Input Burst Initiated (BURST BUSY LO-HI) [3]	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO) [3]	D21	
D06	Analog Input Clock	D22	3.4.4
D07	Analog Output Clock	D23	3.14.4
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition [3]	D24	3.9
D09	Output Buffer threshold flag HIGH-to-LOW transition [3]	D25	3.14.2.5
D10	Output Buffer threshold flag LOW-to-HIGH transition [3]	D26	
D11	Output Load-Ready Flag HIGH-to-LOW transition [3]	D27	3.14.3.3
D12	Output Load-Ready Flag LOW-to-HIGH transition [3]	D28	
D13	Analog Output Burst Ready	D29	3.14.5.2
D14	Output Buffer Overflow or Frame Overflow [3]	D30	3.14.2.5 3.14.3.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Edge-detected response bits remain HIGH until cleared LOW.
3. Edge-detected event.

Table 3.12-1. Typical Input Buffer DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.14-1. Analog Output Configuration Register

Offset: 0054h **Default: 0000 02FFh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00	RW	OUTPUT 00	1	Analog output Active Channel selection mask. *	3.14.1.1
D01	RW	OUTPUT 01	1	HIGH to enable.	
D02	RW	OUTPUT 02	1		
D03	RW	OUTPUT 03	1		
D04	RW	OUTPUT 04	1		
D05	RW	OUTPUT 05	1		
D06	RW	OUTPUT 06	1		
D07	RW	OUTPUT 07	1		
D08-D10	RW	OUTPUT RANGE	2	Analog Output Range: 0 => ±2.5V. 1 => ±5V. 2 => ±10V 3 => 0 to +5V. 4 => 0 to +10V 5-7 => (Reserved).	3.14.1.2
D11	RW	CLOCK TRIGGER OUT	0	Enables the Analog Output Clock and Trigger external outputs,	3.14.4.1
D12-D13	RW	CLOCK SOURCE *	0	Analog Output clock source: 0 => Rate-C Generator. 1 => Rate-A Generator. 2 => Analog Output External Clock input 3 => (Reserved).	3.14.4
D14-D15	RW	TRIGGER SOURCE *	0	Analog Output trigger source: 0 => Rate-D Generator. 1 => Rate-B Generator. 2 => Analog Output External Trigger input 3 => (Reserved).	3.14.5
D16	RW	OUTPUT CONFIG	0	Analog Output Configuration: 0 => Single-ended outputs. 1 => Differential outputs.	3.14.1.4
D17	RW	(Reserved)	0	---	---
D18-D31	RO	(Reserved)	000h	---	---

Table 3.14-2. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only; Returns all-zero)**

BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	DATA 00	Least significant data bit
D01-D16	WO	DATA 01 - DATA 16	Intermediate data bits
D17	WO	DATA 17	Most significant data bit
D18	WO	EOF FLAG	End-of-frame (EOF) flag.
D19-D31	WO	**---**	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

Table 3.14-3. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_1400h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D04	R/W	(Reserved)	0h	---	---
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.14.4
D06	RO	OUTPUT CLOCK READY	0	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	3.14.4
D07	R/W	OUTPUT SW CLOCK *	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.14.4.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.14.2.7
D09	R/W	LOAD REQUEST *	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.14.3.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	3.14.3.3
D11	R/W	CLEAR OUTPUT BUFFER *	0	Resets the output buffer to empty.	3.14.2.5
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	3.14.2.5
D13	RO	OUTPUT BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	3.14.2.5
D14	RO	(Reserved)	0	Inactive; Returns zero.	---
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.14.2.5
D16	R/W	AO BUFFER OVERFLOW	0	Set HIGH when data is written to a full buffer. **	3.14.2.5
D17	R/W	FRAME OVERFLOW	0	Set HIGH when data is written to a closed buffer. **	3.14.2.5
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.14.5.2
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.14.5.2
D20	R/W	OUTPUT SW TRIGGER *	0	Produces a single output trigger event when asserted. Clears LOW automatically when the clock event is completed. Independent of triggering mode. Duplicated in the BCR.	3.14.5.2
D21-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

* Clears LOW automatically when operation is completed.
** Remains HIGH until cleared by a direct write as LOW, or by initialization.

Table 3.14-4. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D19	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D20-D31	RO	(Inactive)	0	---

Table 3.14-5. Output Buffer Threshold Register

Offset: 0040h **Default: 0007 FFFEh**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D19	RW	OUTPUT BUFFER THRESHOLD	7 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D20	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold.
D21-D31	RO	Reserved	0	---

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved bit field)
D16	Number of analog input channels: 0 => 8 Input and 8 output channels. 1 => 4 input and 4 output channels.
D17	Total Effective Buffer Capacitor: 0 => 4 MByte effective capacity. 1 => 2 MByte effective capacity.
D18-D19	Analog Input filter frequency: 0 => Filter-A = 80kHz, Filter-B = 200kHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D20-D21	Master Clock frequency: 0 => 40.320 MHz. 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D22-D31	(Reserved bit field; returns all-zero).

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APPENDIX B

COMPARISON of PCI66-18AISS8AO8 and PMC66-16AISS16AO2

Appendix B

Comparison of PCI66-18AISS8AO8 and PMC66-16AISS16AO2

Operation of the PCI66-18AISS8AO8 is similar to that of the PMC66-16AISS16AO2. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a comprehensive list of requirements.

B.1. Comparison of Features

Table B.1 compares principal PCI66-18AISS8AO8 and PMC66-16AISS16AO2 features. Modifications are shown in bold type.

Table B.1. PMC66-16AISS16AO2, PCI66-18AISS8AO8 Comparison

Feature	PMC66-16AISS16AO2	PCI66-18AISS8AO8
Input Channels	**Sixteen 16-Bit ADC's; SAR**	**Eight 18-Bit ADC's; SAR**
Input Sample Rates	**Zero to 1.0MSPS/Chan**	**Zero to 500KSPS/Chan**
Input Buffer	**256K-Sample FIFO**	**512K-Sample FIFO**
Input Ranges	**±10V, ±5V, ±2.5V**	**±10V, ±5V, ±2.5V, 0/+10V, 0/+5V**
Output Channels	**Two 16-Bit DAC's**	**Eight 18-Bit Dac's; R-2R Hybrid**
Output Clock Rates	**Zero to 1.0MSPS/Chan**	**Zero to 500KSPS/Chan**
Output Buffer	**256K-Sample FIFO**	**512K-Sample FIFO**
Output Ranges	**±10V, ±5V, ±2.5V**	**±10V, ±5V, ±2.5V, 0/+10V, 0/+5V**
Output Registers	**Two; One per channel**	**None. Direct access through buffer**
Output Configuration	**Single-Ended**	**Single-Ended or Balanced Differential; Software-selectable**
Function Generation	Yes	Yes
Rate Generators	**Three, with 24-Bit dividers**	**Four, with 24-Bit dividers**
Digital I/O Port	**6-Bit Bidirectional TTL; Byte oriented.**	**8-Bit Bidirectional TTL; Nibble oriented.**
PCI Adapter	PCI-9056 (66MHz PCI)	PCI-9056 (66MHz PCI)
Interrupt	None. (Replaced with a primary status register)	None. (Replaced with a primary status register)
PCI Interface	PCI 2.3; 33MHz/66MHz	PCI 2.3; 33MHz/66MHz
DMA (Buffers)	Block mode	Block mode
Local Clock	40-45 MHz	40-45 MHz

B.2. Migration from PMC66-16AISS16AO2:

Para 2.2.2. Input/Output Cable Connections:

- The system I/O connector has changed from 80 pins to 100 pins.

Para 2.3.1.3. Current-Loop Inputs:

- Software-selected analog input current-loop terminators have been added.

Para 2.3.2.1. Output Configurations:

- Differential outputs have been added.

Para 2.5. Reference Verification:

- Three reference adjustments are now required for calibration.

Table 3.1-1. Control and Data Registers:

- Control registers "Analog Output Chan 00" and "Analog Output Chan 01" have been deleted.
- Control register "Active Input Channels" has been replaced with new register "Analog Input Config."
- New control registers "Current Loop Select", "Rate Generator-D" and "Analog Output Config" have been added.

Table 3.2-1. Board Control Register (BCR):

- "Analog Input Mode" and "Input Range" fields have moved to the new "Analog Input Configuration" register.
- "Output Range" field has moved to the new "Analog Output Configuration" register.
- Control bits "Enable Buffered Outputs", "Trigger Initiator" and "Analog Input Clock Initiator" have been deleted.
- Control bit "Enable Rate-D Generator" has been added.

Table 3.4-1. Analog Input Configuration Register:

- New register contains the "Active Input Channels" mask, as well as "Input Range", "Clock Source", "Trigger Source", "Clock Trigger Out", "Input Config" and "Group-A/B Filter" control fields.

Table 3.4-2. Input Data Buffer:

- Control field "Input Channel Number" replaces "First-Channel Tag."

Table 3.4-3. Input Buffer Threshold Register:

- Control field "Input Buffer Threshold" has been extended to 20 bits.

Table 3.5-1. Current Loop Selection Register:

- Replaces register "Analog Output Data Register.".
- New register controls the selection of current-loop input channels.

Table 3.7-1. Rate Generator Registers (A,B,C,D):

- Renamed table. Now combines all rate control registers.

Table 3.9-1. Digital I/O Port Register:

- The original 6-Bit DIO port has been replaced with an 8-bit port.

Table 3.14-1. Analog Output Configuration Register:

- New register contains the "Active Output Channels" mask, as well as "Output Range", "Clock Source", Trigger Source", "Clock Trigger Out", "Output Config", "Address Mode", and "Output Deglitch" control fields.

Table 3.14-2. Analog Output Buffer:

- Data field has been extended to 18 bits; Address field replaces Channel-zero tag.

Table 3.14-3. Buffered Output Operations Register:

- Control bit "Analog Output Clk Initiator" and control field "AO CHAN 00/01 ACTIVE" have been deleted.

Table 3.14-4. Output Buffer Size Register:

- "Buffer Size" field has been extended to 20 bits.

Table 3.14-5. Output Buffer Threshold Register:

- Control field "Output Buffer Threshold" has been extended to 20 bits.

Table 3.16-1. Assembly Configuration Register:

- Options have been modified per new configuration requirements.

Revision History:

Revision 053007:

Para 3.7:	Added maximum input and output clocking rates.

Revision 122806:

Tables 3.1-1, 3.14-3:	Corrected BOR default value.

Revision 120506:

Para 3.4.5.1:	Added note regarding input buffer reset duration.
Para 3.10:	Revised autocal duration.
Para 3.14.1.2:	Unipolar Zero-selftest response.

Revision 110906:

Origination.

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General Standards Corp.
8302A Whitesburg Dr.
Huntsville, Alabama 35802
Telephone: (256) 880-8787
FAX: (256) 880-8788

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