General Standards Corporation

High Performance Bus Interface Solutions

Rev: 122210

CCPMC66-16AI32SSA

CONDUCTION-COOLED DIFFERENTIAL 32-CHANNEL, 16-BIT, SIMULTANEOUS SAMPLING, PMC ANALOG INPUT BOARD

With 200KSPS Sample Rate per Channel,
Rear-Panel I/O and 66MHz PCI Support

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The CCPMC66-16AI32SSA board is a single-width PCI mezzanine card (PMC) that provides high-speed simultaneous 16-bit analog input capability for PMC applications. 32 differential analog input channels can be digitized simultaneously at rates up to 200,000 conversions per second per channel, with software-controlled voltage ranges of ±2.5V, ±1.25V or ±0.625V. An optional maximum input range of ±10V also is available. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

Autocalibration determines offset and gain correction values for each input channel, and the corrections are applied subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host.

Power requirements consist of +5 VDC from the PCI bus in compliance with the PCI specification, and operation over the specified temperature range is achieved with either conventional air cooling or conduction cooling. Specific details of physical characteristics and power requirements are contained in the CCPMC66-16AI32SSA product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

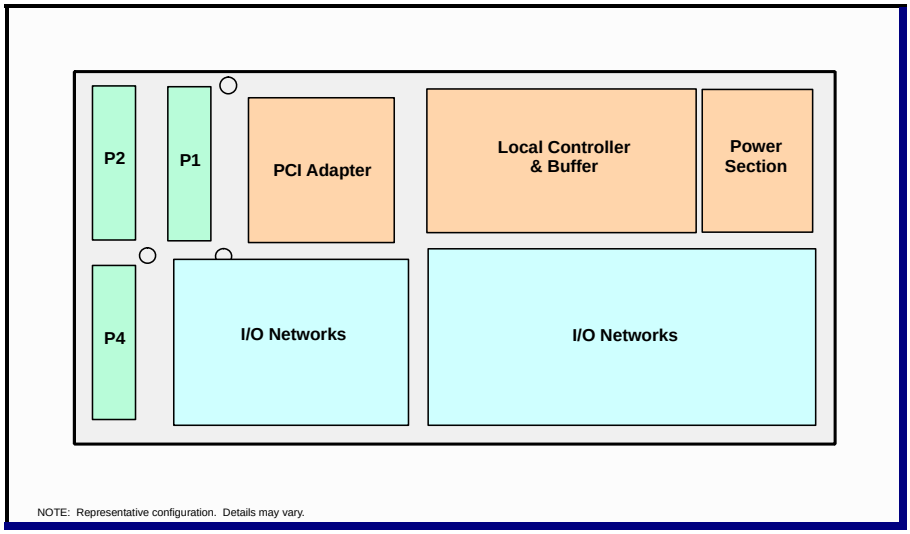

Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. System input and output connections are made through the mezzanine P4 connector. An auxiliary connector at the edge of the board provides bidirectional external sync and clock ports.

1.2 Functional Overview

The 16-Bit CCPMC66-16AI32SSA analog input board samples and digitizes 32 input channels simultaneously at rates up to 200,000 samples per second for each channel. The resulting 16-bit sampled data is available to the PCI bus through a 1M-Byte FIFO buffer. Each input channel contains a dedicated 16-Bit sampling ADC. All operational parameters are software configurable.

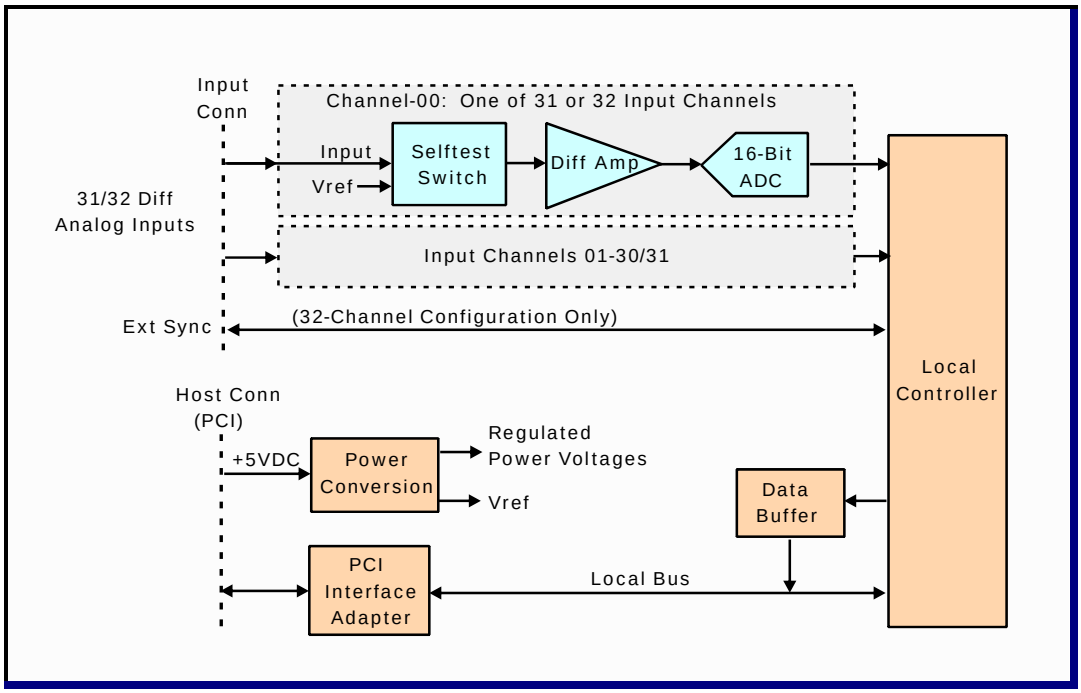

Figure 1.2-1. Functional Organization

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the three mezzanine connectors P1, P2 and P4 facing the mating connectors J1, J2 and J4 on the host board. Then carefully press the board into position on the host. Verify that the mezzanine connectors have mated completely and that the board is seated firmly against the host board.

Attach the board to the host with 2.5 x 6.5mm panhead screws. Pass the screws through the board into the corresponding mounting holes on the host rails. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System I/O connections are made through the P4 mezzanine connector with the pin assignments listed in Table 2.2-1.

Auxiliary Sync I/O connections are made through a low-profile 6-Pin, single-row located on the back of the board (Side-2), with the pin assignments shown in Table 2.2-2. The auxiliary sync I/O connector is designed to mate with a Molex cable connector Model 51146-0600.

Table 2.2-1. System Connector P4 Pin Functions

a. 31-Channel Configuration

ROW-A			ROW-B	
PIN	SIGNAL		PIN	SIGNAL
63	INP00 HI		64	INP01 HI
61	INP00 LO		62	INP01 LO
59	INP02 HI		60	INP03 HI
57	INP02 LO		58	INP03 LO
55	INP04 HI		56	INP05 HI
53	INP04 LO		54	INP05 LO
51	INP06 HI		52	INP07 HI
49	INP06 LO		50	INP07 LO
47	INP08 HI		48	INP09 HI
45	INP08 LO		46	INP09 LO
43	INP10 HI		44	INP11 HI
41	INP10 LO		42	INP11 LO
39	INP12 HI		40	INP13 HI
37	INP12 LO		38	INP13 LO
35	INP14 HI		36	INP15 HI
33	INP14 LO		34	INP15 LO
31	INP16 HI		32	INP17 HI
29	INP16 LO		30	INP17 LO
27	INP18 HI		28	INP19 HI
25	INP18 LO		26	INP19 LO
23	INP20 HI		24	INP21 HI
21	INP20 LO		22	INP21 LO
19	INP22 HI		20	INP23 HI
17	INP22 LO		18	INP23 LO
15	INP24 HI		16	INP25 HI
13	INP24 LO		14	INP25 LO
11	INP26 HI		12	INP27 HI
9	INP26 LO		10	INP27 LO
7	INP28 HI		8	INP29 HI
5	INP28 LO		6	INP29 LO
3	INP30 HI		4	INPUT RTN
1	INP30 LO		2	INPUT RTN

b. 32-Channel Configuration

ROW-A			ROW-B	
PIN	SIGNAL		PIN	SIGNAL
63	INP00 HI		64	INP01 HI
61	INP00 LO		62	INP01 LO
59	INP02 HI		60	INP03 HI
57	INP02 LO		58	INP03 LO
55	INP04 HI		56	INP05 HI
53	INP04 LO		54	INP05 LO
51	INP06 HI		52	INP07 HI
49	INP06 LO		50	INP07 LO
47	INP08 HI		48	INP09 HI
45	INP08 LO		46	INP09 LO
43	INP10 HI		44	INP11 HI
41	INP10 LO		42	INP11 LO
39	INP12 HI		40	INP13 HI
37	INP12 LO		38	INP13 LO
35	INP14 HI		36	INP15 HI
33	INP14 LO		34	INP15 LO
31	INP16 HI		32	INP17 HI
29	INP16 LO		30	INP17 LO
27	INP18 HI		28	INP19 HI
25	INP18 LO		26	INP19 LO
23	INP20 HI		24	INP21 HI
21	INP20 LO		22	INP21 LO
19	INP22 HI		20	INP23 HI
17	INP22 LO		18	INP23 LO
15	INP24 HI		16	INP25 HI
13	INP24 LO		14	INP25-31 LO *
11	INP26 HI		12	INP27 HI
9	INPUT RTN		10	INPUT RTN
7	INP28 HI		8	DIG RTN
5	INP29 HI		6	CLOCK I/O
3	INP30 HI		4	DIG RTN
1	INP31 HI		2	SYNC I/O

Table 2.2-2. Auxiliary Sync I/O Connections

SIGNAL	P1 PIN	PMC CONN PIN *
DIG RTN	1	Digital Ground
AUX-0	2	PMC P1-41
DIG RTN	3	Digital Ground
AUX-1	4	PMC P1-42
DIG RTN	5	Digital Ground
(Reserved)	6	PMC P2-10

* Contact GSC Sales for availability of PMC connector access.

2.3 System Configuration

2.3.1 Analog Inputs

The 32 analog input channels can be configured for either differential or single-ended operation.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

This operating mode also offers the highest rejection of the common mode noise, which is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode, shown in Figure 2.3-1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point which ensures that the sum of the signal level **(Vsig)** and the common mode voltage **(Vcm)** must remain within the range specified for the board. Ground current through the INPUT RTN pins must be limited in order to avoid damage to the cable or the input board.

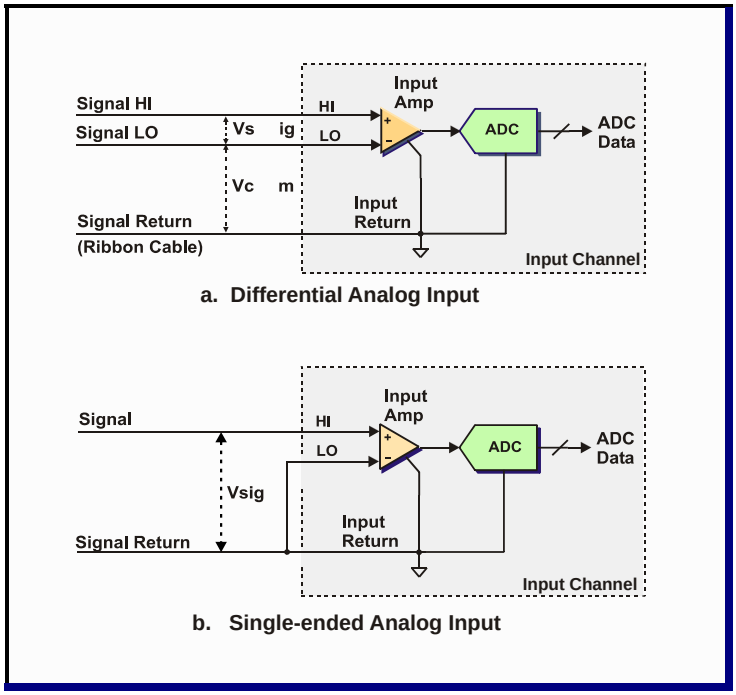

Figure 2.3-1. Analog Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1b) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. A single-ended configuration usually is more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or could generate potentially destructive ground current.

For applications in which multiple signal sources share a single ground, the differential configuration is recommended, with all "LO" inputs connected together at the common remote return.

2.3.2 External Sync I/O

The SYNC I/O pin in the I/O connector is a bidirectional TTL synchronization signal that provides external control of analog input sample triggering. The SYNC I/O signal is referenced to the SYNC I/O RTN pin, which is connected internally to digital ground.

When configured as an input, this signal initiates a triggered sample of all active input channels. The SYNC I/O input is asserted LOW, and is pulled HIGH internally through a 4.7 KOhm resistor. Minimum input pulse width is 140ns.

When configured as an output, the SYNC I/O signal is asserted for approximately 160 nanoseconds at the beginning of each scan. The SYNC I/O output signal is a TTL level that can synchronize the operation of multiple target boards to a single initiator board. Like the SYNC I/O input signal, the SYNC I/O output signal is asserted LOW. Loading of the SYNC output should be limited to 10 milliamps or less.

2.3.3 Auxiliary External Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking to external events when the ENABLE EXTERNAL SYNC control bit is HIGH in the BCR. These TTL connections are available as AUX-0 and AUX-1 (Table2.2-2), and are accessible both through a low-profile 6-Pin connector on the back of the board (Side-2).

Active AUX *outputs* produce an output pulse for each ADC sample clock, and are active in both target and initiator external sync modes. Source and sink load capacity of each output is 8 milliamps.

Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

2.3.4 Multiboard Synchronization

If multiple boards are to be synchronized together, the SYNC I/O and SYNC I/O RTN pins from one board, the ***initiator***, are connected to the SYNC I/O and SYNC I/O RTN pins of as many as four ***target*** boards (Figure 2.3-2). The controlling software determines specific synchronization functions.

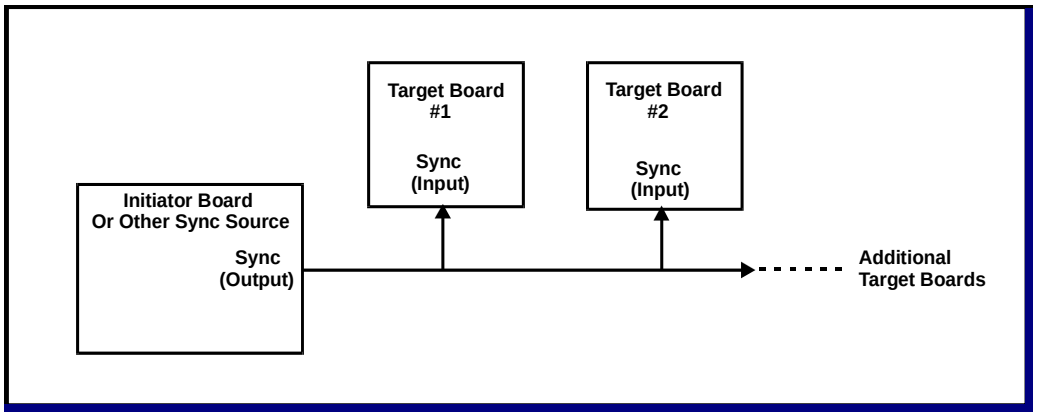

Figure 2.3-2. Multiboard Synchronization

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog input channels are software-calibrated to a single internal voltage reference by an embedded autocalibration software utility. The procedure presented here describes the verification and adjustment of the internal reference.

2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to two 0.024-inch square test posts.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the single reference voltage that ensures conformance to the product specification. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1.

This procedure assumes that the board is installed on an operational host board.

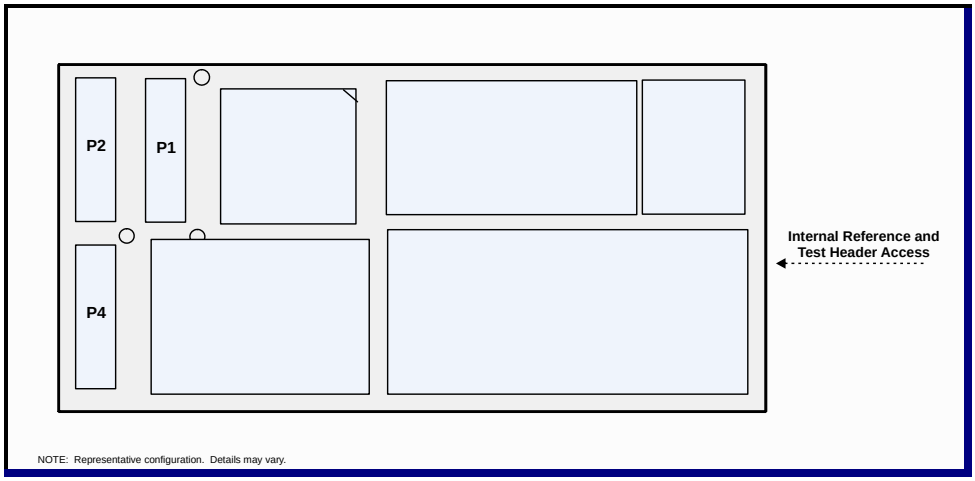

Figure 2.5-1. Reference Adjustment Access

1. Connect the digital multimeter between VCAL (+) Pin-3, and REF RTN (-) Pin-4 in the J2 test connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Select the ±2.5V input range.
4. Verify that the digital multimeter indication is +2.4975 VDC ±0.0005 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer until the digital multimeter indication is within the specified range.
5. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The CCPMC66-16AI32SSA board is compatible with the PCI Local Bus specification, and supports auto-configuration at the time of power-up. A PLX™ PCI-9056 adapter operating in J-mode controls the PCI interface, and supports both 33MHz and 66MHz PCI clock frequencies, as well as D32 PCI bus width. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space. After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All local data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	DEFA ULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	0008 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	000X XXXXh	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	0001 0C80h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer
001C	BURST SIZE	R/W	0000 0001h	Number of sample clocks in a triggered burst.
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	ACTIVE CHANNEL ASSIGNMENT	R/W	0000 0100h	Specific first and last active channels.
0028	Board Configuration	RO	000X XXXXh	Firmware revision and option straps.
002C	Autocal Values **	R/W	0000 080Xh	Autocal value readback.
0030	Auxiliary R/W Register **	R/W	0000 0000h	Auxiliary register. For internal use only.
0034	Auxiliary Sync I/O Control	R/W	0000 0000h	Controls auxiliary sync I/O port
0038	Scan Marker Upper Word	R/W	0000 0000h	Packed-data scan marker D[31..16].
003C	Scan Marker Lower Word	R/W	0000 0000h	Packed-data scan marker D[15..0]..

R/W = Read/Write, RO = Read-Only. ** Maintenance register; shown for reference only.

3.2 Board Control Register (BCR)

The Board Control Register (BCR) controls primary board functions, including analog input mode and range, and consists of 20 active control bits and status flags. Table 3.2-1 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0008 4060h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D02	R/W	AIM[2..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	(Reserved)	0	---	---
D04-D05	R/W	RANGE[1..0]	2	Analog input range. Defaults to the highest available input range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.	3.5.1.2
D07	R/W	ENABLE EXTERNAL SYNC I/O	0	Selects external sync I/O when HIGH.. (The Scan and Sync control register selects TARGET or INITIATOR mode). Not required for bursting (3.12)	3.9
D08-D10	R/W	(Reserved)	0	---	---
D11	R/W	DISABLE SCAN MARKER	0	Disables the scan marker in data packing mode.	3.11
D12	R/W	*INPUT SYNC	0	Triggers a single sample of all active channels when BCR Input Sync is selected in the Scan and Sync Control Register.	3.4.2
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.6
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	3.5.2
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.11
D19	R/W	AUTONOMOUS DEMAND MODE	1	Selects autonomous demand-mode DMA operation when HIGH, or Threshold-driven demand-mode DMA when LOW..	3.8
D20-D31	RO	(Reserved)	0	---	---

R/W = Read/Write, RO = Read-Only. *Clears automatically when operation is completed

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset, and should be required only once after the initial application of power. PCI register configuration terminates with the PCI interrupt disabled.

3.3.2 Initialization

Internal control logic can be initialized without reconfiguration of the PCI registers by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all defaults are invoked,
- The highest available input range is selected.
- All available channels are active (Table 3.4-2),
- Input sample clocking is from the Rate-A generator at 12,500 samples per second,
- Analog input data coding format is offset binary; Data packing is disabled,
- The analog input buffer is reset to empty,
- Input rate generator Rate-A is disabled (Rate Generator Register D16 = HI).

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Parameters

3.4.1 Input Voltage Range

BCR control field RANGE[], as shown in Table 3.4-1 selects the analog input voltage range.

Table 3.4-1. Analog Voltage Range Selection

	ANALOG INPUT RANGE	
RANGE[1:0]	**Low Range Set**	**High Range Set**
0	±0.625Volts	±2.5Volts
1	±1.25 Volts	±5 Volts
2	±2.5 Volts	±10 Volts
3	±2.5 Volts	±10 Volts

3.4.2 Timing Organization

Figure 3.4-1 illustrates the manner in which timing signals are organized within the board. The input sample clock selector is controlled by the Scan and Sync control register, which provides direct software control of clocking and sync operations. The external sync input and output line permits external control of timing. Two rate generators operate directly from the master clock frequency, or can be cascaded.

A sample clock can be generated by either rate generator, by the INPUT SYNC control bit in the BCR, or by an external sync source. Each Input Sample Clock triggers a sample of all active input channels. An active channel group can contain from two to 32 channels, or any single channel can be sampled individually. Each active channel group commences with Channel 00, and proceeds upward through consecutive channels to the selected number of channels.

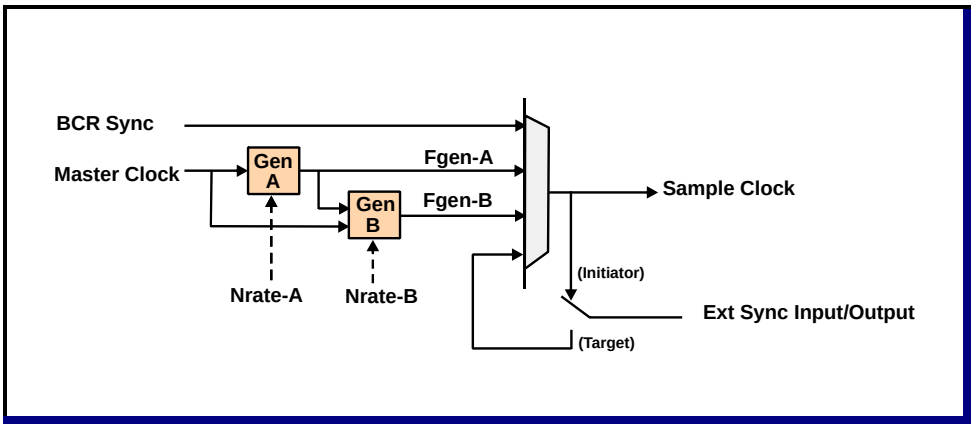

Figure 3.4-1. Clock and Sync Organization

3.4.3 Scan and Sync Control Register

The Scan and Sync control register (Table 3.4-2) controls the configuration of internal timing signals. The ACTIVE CHANNELS control field selects the number of active channels from two channels to 32 channels, or selects the single-channel mode if zero, or allows a user-defined channel group to be defined if equal to '7' (3.5.4.2).

3.4.4 Sample Rate Generators

Each of the two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate register. The two rate registers are organized as shown in Table 3.4-3. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. To prevent the input buffer from filling with extraneous data at power-up, D16 defaults to the HIGH state in the Rate-A control register.

3.4.4.1 Sample Rate Control

Each rate generator is controlled by a *divisor* **Nrate** that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of **Fclk** (MHz), the output frequency **Fgen** of each generator is determined as:

$$\textbf{Fgen (Hz)} = \textbf{Fclk (Hz) / Nrate,}$$

where **Nrate** is the decimal equivalent of D00-D15 in the rate generator register. **Fgen** is the sampling frequency, and equals the rate at which all active channels are sampled. **Fclk** has a standard value of 40.000MHz, but may have other values depending upon custom ordering options.

The maximum sampling frequency **Fgen-max** is 200 kHz.

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D02	R/W	ACTIVE CHANNELS	5	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 31 or 32 channels (00-30 or 0-31); Default value 6 => (Reserved) 7 => Channel group assignment (See Section 3.5.4.2) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	SAMPLE CLOCK SOURCE	0	Selects the analog input sample clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line (Selects TARGET mode) 3 => BCR Input Sync control bit. (See also Triggered Burst, Section 3.12).
D05-D06	R/W	(Reserved)	0	---
D07	RO	BURST BUSY	0	Indicates a burst in progress.
D08-D09	R/W	BURST ON SYNC	0	Selects the **triggered burst** acquisition mode (Section 3.12)
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	(Reserved)	0	---
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	(Reserved)	0	---
D19-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 0C80 (Rate-A), 0000 0050h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		FREQUENCY Fgen (40.000 MHz Master Clock)
(Dec)	(Hex)	(Hz)
200	00C8	200,000
201	00C9	199,005
---	---	Fgen (Hz) = 40,000,000 / Nrate

* ±0.015 percent.

3.4.4.2 Generator Cascading

To provide very low sample rates, the Rate-B generator can be configured with the RATE-B CLOCK SOURCE control field to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

Fgen-B (Hz) = Fclk / (Nrate-A * Nrate-B) ,

which can produce sample rates as low as 0.009 Hz with **Fclk** = 40 MHz.

3.4.5 Multiboard Synchronization

Multiple boards can be interconnected externally to produce synchronous analog input sampling. Figure 2.3-2 illustrates the interconnections required. External sync I/O is enabled by setting the ENABLE EXTERNAL SYNC control bit HIGH in the BCR. One of the boards is designated as the *Initiator*, and the remaining boards are designated as *targets*.

A board that is enabled for external sync I/O is designated as a ***target*** by selecting External Sync Input Line in the SAMPLE CLOCK SOURCE control field in the Scan and Sync control register. Any other value for this field designates the board as an ***initiator***. The sync signal can originate either from an initiator board, or externally as an input to a group of targets.

If the ENABLE EXTERNAL SYNC control bit is set HIGH in the BCR, an initiator generates a sync pulse at the selected sample rate, and each of the target boards responds to the sync pulse by acquiring a single sample of all of its designated active channels.

NOTES: To avoid contention on the SYNC I/O line, all initiator/target designations should be assigned before enabling external sync I/O operation. No more than one board can be designated as an initiator.

For optimum autocalibration effectiveness at rates above 20KSPS, adjust the Rate-A Generator register to the same value on all boards.

Refer to Paragraph 3.9 for alternative external sync provisions.

3.5 Analog Input Control

3.5.1 Input Data Organization

Processed conversion data from the analog-to-digital converters (ADC's) flows directly into the analog input FIFO data buffer, and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

3.5.1.1 Input Data Buffer

Nonpacked analog input data is right-justified to the LSB, and occupies bit positions D00 through D15 (Table 3.5-1). D16 is HIGH for all Channel 00 values, and LOW for data from all other channels. Bits D17-D31 are always returned as zeros. An empty buffer returns an indeterminate value. Refer to Paragraph 3-11 for the configuration of packed data.

3.5.1.2 Data Coding Format

Analog input data is arranged as 16 active right-justified data bits with the coding conventions shown in Table 3.5-2. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

Refer to Section 3.11 for the effect of data packing on buffer contents.

Table 3.5-1. Input Data Buffer; Nonpacked Data

Offset: 0008h **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16	RO	CHANNEL 00 TAG	Indicates a Channel-00 data value
D17-D31	RO	(Inactive)	---

Table 3.5-2. Input Data Coding; 16-Bit Data

ANALOG INPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	0000 FFFF
Negative Full Scale	0000 0000	0000 8000

3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-3 controls and monitors the flow of data through the analog input data buffer. Asserting the CLEAR BUFFER control bit HIGH clears, or empties, the buffer. The Threshold Flag is HIGH when the number of values in the input data buffer ***exceeds the input threshold value*** defined by bits D00-D17, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.7) can be programmed to occur on either the rising or falling edge of the threshold flag.

The Buffer Size register shown in Table 3.5-4 contains the number of locations occupied in the buffer, and is updated continuously. ***If data packing is enabled and scan marking is disabled (3.11), the number of samples present in the buffer is twice the value contained in the Buffer Size register.***

Buffer underflow and overflow flags in the BCR indicate that the buffer has been read while empty or written to when full. Each of these situations is indicative of data loss. Once set HIGH, each flag remains HIGH until cleared, either by directly clearing the bit LOW or by clearing the buffer or initializing the board.

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D17	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D20-D31	RO	(Inactive)	0	---

*Clears automatically within 200ns of being set

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	00000h	Number of locations occupied in the input buffer
D19-D31	RO	(Inactive)	0	---

3.5.3 Analog Input Function Modes

BCR control field AIM[] selects the analog input signal source, and provides selftest modes for monitoring the integrity of the analog input networks. Table 3.5-5 summarizes the input function modes.

3.5.3.1 System Analog Inputs

With the default value of 'Zero' selected for the AIM[] field in the BCR, all ADC channels are connected to the system analog inputs from the system I/O connector.

Table 3.5-5. Analog Input Function Selection

AIM[2:0]	FUNCTION OR MODE
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

3.5.3.2 Selftest Modes

In the selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and the averaged values of multiple samples should be used for critical measurements.

The ZERO selftest applies a Zero reference signal to all input channels, and should produce a nominal midscale reading of 0000 8000h. For the +VREF test, a precision reference voltage is applied to all inputs. ***The +VREF reference voltage equals 99.900% of the positive fullscale value (nominally 0000 FFDFh).***

3.5.4 Active Channel Selection

3.5.4.1 Predetermined Channel Group

The analog inputs can be sampled in groups of 2, 4, 8, 16 or 31/32 active channels, or any single channel can be selected for digitizing. The number of active channels is selected by the ACTIVE CHANNELS[] field in the scan and sync control register. Each active channel group commences with Channel-00, and proceeds upward through successive channels to the selected number of channels.

For Single-Channel sampling (ACTIVE CHANNELS[] = 0), the channel to be digitized is selected by the SINGLE-CHANNEL SELECT control field.

3.5.4.2 User-Defined Channel Group

If "Channel group assignment" is selected in the ACTIVE CHANNELS field in the Scan and Sync control register (Table 3.4-2), the first and last active channels are defined by the Active Channels Assignment control register shown in Table 3.5-6. The group of active channels is *contiguous*, beginning with the channel designated by the FIRST CHANNEL SELECT field, and proceeding upward through consecutive channels to and including the channel designated by LAST CHANNEL SELECT. The LAST CHANNEL SELECT field must be equal to or greater than the FIRST CHANNEL SELECT field.

Table 3.5-6. User-Defined Active Channel Assignment

Offset: 0000 0024h **Default: 0000 0100h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	R/W	FIRST CHANNEL SELECT	0	First (lowest-numbered) active channel
D08-D15	R/W	LAST CHANNEL SELECT	1	Last (highest-numbered) active channel
D16-D31	RO	(Reserved)	0	Inactive. Returns all-zero.

When this method is used for selecting active channels, the context of the Channel-00 tag in the data buffer (Table 3.5-1) changes to "First-Channel tag." For example, if FIRST CHANNEL SELECT = 05, then D16 in the buffer will be HIGH for Channel-05 data, and LOW otherwise. This context change applies also to the scan marker (Section 3.11).

NOTE: The Active Channel Assignment register is monitored for invalid values, and is adjusted automatically to correct assignment errors. The first channel must not be higher than the selected last channel, and the selected last channel must not exceed the highest available channel number.

3.6 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup or a PCIbus reset,
- Input range change,
- Sample rate change, if greater than 20 kHz.

A small error, on the order of 0.04-percent, can be introduced when the input range is changed, or when a large change (>20 kHz) occurs in the sample rate. Performing autocalibration with the required sample rate selected eliminates this error.

During autocalibration, no control settings are altered and external analog input signals are ignored.

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of approximately 0.5 second. Completion of the operation can be detected either by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.7) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

NOTE: For autocalibration during synchronous multiple-board operation at rates above 20KSPS, adjust the Rate-A Generator register to the same value on all boards (3.4.4).

3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.7.1)
b. The *PCI interrupt* must be enabled (Section 3.7.2).

A local interrupt request will not generate a PCI bus interrupt unless the PCI interrupt has been enabled as described in Paragraph 3.7.2.

3.7.1 Local Interrupt Request

The Interrupt Control Register shown in Table 3.7-1 controls the single local interrupt request line. Two simultaneous source conditions (IRQ 0 and1) are available for the request, with multiple conditions available for each source. IRQ 0 and 1 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for either of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *Local Interrupt Input Enable* control bits HIGH in the *Runtime Interrupt Control/Status Register* described in Section 6 of the PLX™ PCI-9056 reference manual.

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT EVENT
D00-02	R/W	IRQ0 A0,1,2	0	0	Initialization completed.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4	Triggered burst initiated (BURST BUSY => HI)
				5	Triggered burst completed (BURST BUSY => LO)
				6-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	Input buffer overflow or underflow
				4-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

3.8 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master, in either DMA Channel 00 or Channel 01. Set bit D[02] in the PCI Command register HIGH to select the bus mastering mode. Also, clear D[15] LOW in the PCI-9056 DMA Mode register to select *slow-terminate* operation. Refer to the PCI-9056 reference manual for a detailed description of DMA configuration registers.

3.8.1 Block Mode

Table 3.8-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: *Block-mode* DMA can be implemented regardless of the state of the AUTONOMOUS DEMAND MODE control bit in the BCR.

3.8.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.8-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.8.2.1 Autonomous

This mode is selected if the AUTONOMOUS DEMAND MODE control bit is HIGH in the BCR (the default condition). When operating in this mode, DMA data transfer from the input buffer is requested continuously as long as the buffer contains data. If the control bit is LOW, then Threshold-Flag Driven demand-mode DMA operation is selected (3.8.2.2).

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty* in the autonomous mode, the situation can arise in which the last one or two samples in an active channel group are retained in the buffer until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

3.8.2.2 Threshold-Flag Driven

This mode is similar to autonomous DMA, except a DMA transfer request is initiated *only* when the number of values in the buffer ***exceeds the threshold value*** selected for the buffer. The threshold-flag driven DMA request is sustained until one of the following events occurs:

- The data buffer goes empty,
- The number of values read from the buffer equals the threshold value plus one,
- The buffer is cleared,
- The board is reset,
- Autocalibration is executed.

The DMA request is terminated at the first occurrence of any of these events.

3.9 Auxiliary External Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking to external events when the ENABLE EXTERNAL SYNC control bit is HIGH in the BCR. These TTL connections are available as AUX-0 and AUX-1 (Table 2.2-2), and are accessible through a standard 6-Pin header on one edge of the board.

AUX sync signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.9-1. When an AUX signal is designated as an *input*, the signal replaces the SYNC IO input from the system connector, and the board must be configured as a sync ***target*** in the Scan and Sync control register (Table 3.4-2). If multiple AUX signals are designated as active inputs, the inputs are logically OR'd together internally. 'Inactive' and 'Active Input' AUX lines are pulled to +3.3VDC through 4.7K. Active AUX *outputs* produce an output pulse for each ADC sample clock, and are active in both target and initiator external sync modes.

To increase the reliability of external triggering in high-noise environments, selectable noise suppression increases the debounce or detection interval for active inputs, and increases the pulse width of active outputs.

Table 3.9-1. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-01	R/W	AUX-0 Control Mode	0	AUX-0 I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX-1 Control Mode	0	AUX-1 I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 1.5us, and output pulse width is 2.0us.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as AUX-0.

AUX *inputs* are edge-detected as LOW-to-HIGH transitions if the INVERT INPUTS control bit is LOW, or as HIGH-to-LOW transitions if the bit is HIGH. Minimum HIGH and LOW level durations are 135ns if the NOISE SUPPRESSION control bit is LOW, or 1.5us if the bit is HIGH. AUX *output pulses* are positive (i.e.: baseline level is LOW) if the INVERT OUTPUTS control bit is LOW, or negative (baseline HIGH) if the control bit is HIGH. Output pulse width is typically 135ns if the NOISE SUPPRESSION control bit is LOW, or 2.0us if the bit is HIGH.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10-1) contains the existing firmware revision, and a status field that indicates the configuration of optional features.

Table 3.10-1. Board Configuration Register

Offset: 0000 0028h **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D14	(Reserved status flags)
D15	Product Identification flag: High indicates CCPMC66-16AI32SSA
D16-D17	Channel Availability: 0 => 31 Channels * 1 => 8 Channels 2 => 16 Channels 3 => 32 Channels
D18	Master Clock Frequency: 0 => 40.000MHz 1 => (Reserved)
D19	Input Voltage Range Set:: 0 => ±2.5V, ±1.25V, ±0.625V 1 => ±10V, ±5V, ±2.5V.
D20-D31	(Reserved)

* External Sync-I/O is not available through the P4 connector in the 31-Channel configuration.

3.11 Data Packing

Setting the ENABLE DATA PACKING control bit high in the BCR selects the data packing mode, in which two consecutive 16-bit data values are packed into a single 32-Bit local data longword. In the data packing mode, a 32-bit scan marker code is inserted directly before each Channel-00 data value in the buffer. ***The scan marker can be disabled by setting the DISABLE SCAN MARKER control bit HIGH in the BCR.***

The scan marker code is defined by the 'Scan Marker Upper Word' and 'Scan Marker Lower Word' registers listed in Table 3.1-1, and is inserted immediately before the first (Channel-00) value in each data scan as shown in Table 3.11-1. The lower 16 bits in each register contains one word of the code. The upper 16 bits of these registers are ignored, and should be written as all-zero.

Table 3.11-1. Data Packing

	Buffer Data Field					
	ENABLE DATA PACKING = 0 DISABLE SCAN MARKER = X		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 0		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 1	
Buffer Lword Order	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**
00	0001h	Chan 00 Data	Upper Marker	Lower Marker	Chan 01 Data	Chan 00 Data
01	0000h	Chan 01 Data	Chan 01 Data	Chan 00 Data	Chan 03 Data	Chan 02 Data
02	0000h	Chan 02 Data	Chan 03 Data	Chan 02 Data	Chan 05 Data	Chan 04 Data
03	0000h	Chan 03 Data	Chan 05 Data	Chan 04 Data	Chan 07 Data	Chan 06 Data
---	---	---	---	---	---	---

Some applications may require the scan marker code to be absolutely unique and not appear randomly in the data. To support this requirement, an all-zero marker code (0000 0000h) causes every all-zero data value (0000h) to be forced to a unit code (0001h) when data packing is enabled. This arrangement supports the uniqueness requirement without affecting the differential linearity of the data itself.

NOTE: If the number of active channels is odd-numbered while data packing is enabled, an all-zero data value is inserted directly after the last active channel value. Like all other all-zero data values, the inserted value is forced to a unit code if an all-zero marker is in effect and scan marking is enabled.

3.12 Triggered Bursts

When the BURST ON SYNC control field is nonzero in the Scan and Sync control register (Table 3.4-2), the context of a sync event changes from "sample on sync" to "burst on sync." In the "*sample on sync*" context, a sync event initiates a single sample of all active channels. In the "*burst on sync*" context, a sync event initiates a **burst** of internal sample clocks, each of which produces a sample of all active channels.

3.12.1 Burst Size and Trigger Source

The number of sample clocks issued during a burst is controlled by the 20-bit **Burst Size control register** listed in Table 3.1-1, which has a range from 1 to 1,048,575 sample clocks. For Burst-Size values of one or greater, the number of sample clocks in a burst equals the value in the register. For example, if a burst size of 10 is selected while 16 channels are active, then each burst will contain 160 sample values. Selection of the burst trigger source is summarized in Table 3.12-1. A Burst-Size of zero produces a burst that extends continuously until stopped, either by disabling the internal clock or by clearing the BURST ON SYNC control field.

Table 3.12-1. Burst Trigger Source

Scan and Sync Register BURST ON SYNC	Burst Trigger Source	Sync I/O Pin
0	Bursting disabled.	(Sample-Clock I/O)
1	Rate-B generator.	Trigger Output *
2	External Sync I/O input pin (or AUX input)	Trigger Input *
3	INPUT SYNC control bit in the BCR.	Trigger Output *

* Independent of BCR control bit ENABLE EXTERNAL SYNC.

The Sync I/O pin in the system I/O connector can operate as an input or output trigger pin. The trigger output can serve as a burst trigger for target boards in which the BURST ON SYNC control field selects the external Sync I/O pin as a trigger source. The burst trigger selection supersedes the sample clock selection for control of the external Sync-I/O pin.

NOTE: During a triggered burst the BURST BUSY status flag in the Scan and Sync control register goes HIGH at the trigger event, and returns LOW at the end of the burst. Either edge of the BURST BUSY flag is selectable as an interrupt event (Table 3.7-1).

3.12.2 Sample Clock Source

When operating in the triggered-burst mode, the sample-clock source is selected by the SAMPLE CLOCK SOURCE field in the Scan and Sync control register. The single restriction on the sample clock source is that the burst trigger and the sample clock can not use the same source simultaneously.

The following sequence illustrates the setup for a typical burst operation:

1. Select the input range, sample-clock source and burst size, with clocking disabled,
2. Use Table 3.12-1 to select the burst trigger source (enables burst triggering),
3. Clear the buffer, then enable clocking.

3.13 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance is suspended. Abrupt changes include:

- A change in voltage range or sample rate,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of 32 differential analog input channels contains a dedicated 16-Bit ADC, a selftest input switching network, and a differential input amplifier (Figure 4.1-1). A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller. +5 VDC power from the PCIbus is converted into regulated power voltages for the internal analog networks.

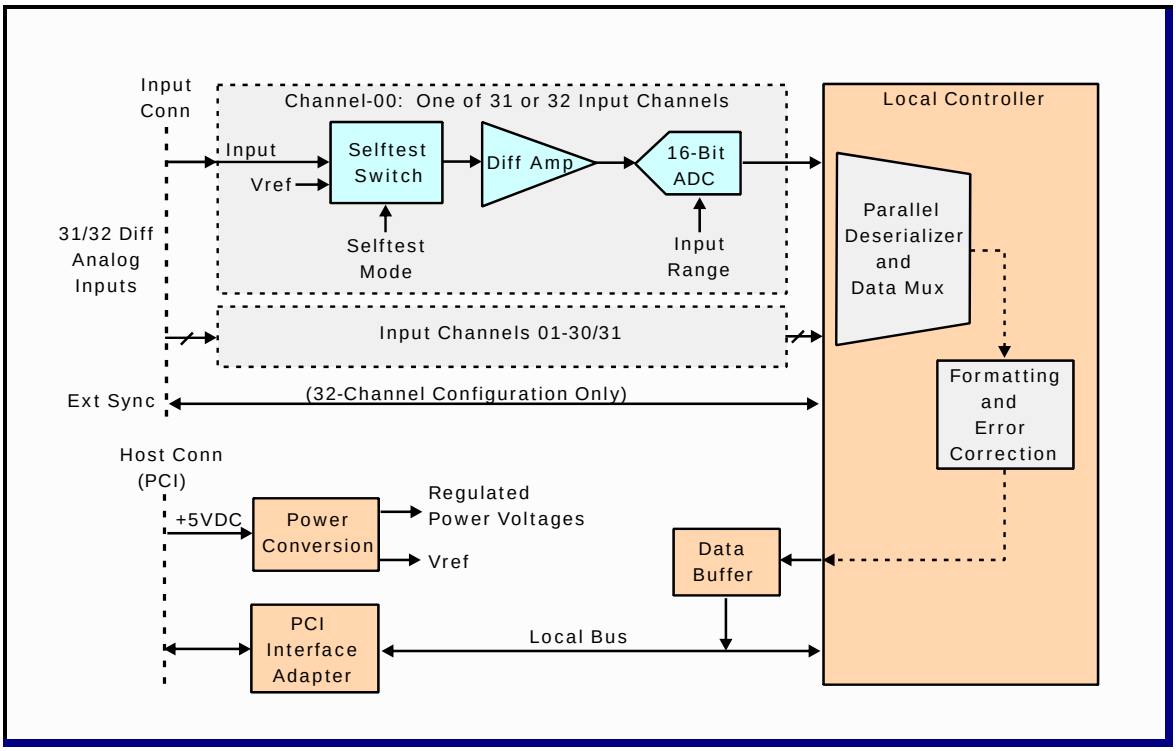

Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input channels, and the input differential amplifier is biased to accept bipolar input ranges. The input range is controlled by adjusting the ADC reference voltage. Each input sample is corrected for gain and offset errors with calibration values determined during autocalibration. A 1-Megabyte FIFO buffer accumulates analog input data for subsequent retrieval by a PMC host.

Analog input sampling on multiple target boards can be synchronized to a single software-designated initiator board. An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, the ADC's receive system analog input signals from the input connector. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC. An input attenuator in each channel provides the necessary scaling and offset parameters to support bipolar input ranges.

Serial data from each ADC is deserialized and multiplexed into a parallel data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies the gain and offset correction values that are obtained during autocalibration. The corrected data is formatted, a tag is attached to all Channel-00 data if applicable, and the data is finally loaded into the input of the analog input data buffer.

4.3 Rate Generators

The local controller contains two independent rate generators, each of which divides a master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a clocking source for the analog inputs, and the generators can be cascaded to produce very long clocking intervals.

4.4 Data Buffer

A 1M-Byte FIFO buffer accumulates analog input data for subsequent retrieval through the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by a threshold flag that can be used to generate an interrupt request when the number of values in the buffer moves above or below a selected count. Local data packing is supported.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

An internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample as it is acquired during acquisition. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated supply voltages of +5 VDC and ±15 VDC are required for internal analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

APPENDIX A

Local Control Register Quick Reference

APPENDIX A
Local Control Register Quick Reference

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	DEFA ULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	0008 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	000X XXXXh	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	0003 FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	0001 0C80h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	0000 0000h	Number of values in the input buffer
001C	BURST SIZE	R/W	0000 0001h	Number of sample clocks in a triggered burst.
0020	SCAN AND SYNC CONTROL	R/W	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	ACTIVE CHANNEL ASSIGNMENT	R/W	0000 0100h	Specific first and last active channels.
0028	Board Configuration	RO	000X XXXXh	Firmware revision and option straps.
002C	Autocal Values **	R/W	0000 080Xh	Autocal value readback.
0030	Auxiliary R/W Register **	R/W	0000 0000h	Auxiliary register. For internal use only.
0034	Auxiliary Sync I/O Control	R/W	0000 0000h	Controls auxiliary sync I/O port
0038	Scan Marker Upper Word	R/W	0000 0000h	Packed-data scan marker D[31..16].
003C	Scan Marker Lower Word	R/W	0000 0000h	Packed-data scan marker D[15..0]..

R/W = Read/Write, RO = Read-Only. ** Maintenance register; shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0008 4060h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION	REF
D00-D02	R/W	AIM[2..0]	0	Analog input mode. Selects system inputs or selftest mode. Defaults to System Inputs	3.5.3
D03	R/W	(Reserved)	0	---	---
D04-D05	R/W	RANGE[1..0]	2	Analog input range. Defaults to the highest available input range.	3.4.1
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.	3.5.1.2
D07	R/W	ENABLE EXTERNAL SYNC I/O	0	Selects external sync I/O when HIGH.. (The Scan and Sync control register selects TARGET or INITIATOR mode). Not required for bursting (3.12)	3.9
D08-D10	R/W	(Reserved)	0	---	---
D11	R/W	DISABLE SCAN MARKER	0	Disables the scan marker in data packing mode.	3.11
D12	R/W	*INPUT SYNC	0	Triggers a single sample of all active channels when BCR Input Sync is selected in the Scan and Sync Control Register.	3.4.2
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted.	3.6
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	3.6
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all register defaults.	3.3.2
D16	R/W	BUFFER UNDERFLOW	0	Set HIGH if the buffer is read while empty. Cleared by direct write or by buffer clear.	3.5.2
D17	R/W	BUFFER OVERFLOW	0	Set HIGH if the buffer is written to when full. Cleared by direct write or by buffer clear.	3.5.2
D18	R/W	ENABLE DATA PACKING	0	Enables local-bus data packing	3.11
D19	R/W	AUTONOMOUS DEMAND MODE	1	Selects autonomous demand-mode DMA operation when HIGH, or Threshold-driven demand-mode DMA when LOW..	3.8
D20-D31	RO	(Reserved)	0	---	---

R/W = Read/Write, RO = Read-Only. *Clears automatically when operation is completed

Table 3.4-1. Analog Voltage Range Selection (BCR field)

	ANALOG INPUT RANGE	
RANGE[1:0]	Low Range Set	High Range Set
0	±0.625Volts	±2.5Volts
1	±1.25 Volts	±5 Volts
2	±2.5 Volts	±10 Volts
3	±2.5 Volts	±10 Volts

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D02	R/W	ACTIVE CHANNELS	5	Number of active input channels: 0 => Single-Channel mode * 1 => 2 channels (00-01) 2 => 4 channels (00-03) 3 => 8 channels (00-07) 4 => 16 channels (00-15) 5 => 31 or 32 channels (00-30 or 0-31); Default value 6 => (Reserved) 7 => Channel group assignment (See Section 3.5.4.2) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	SAMPLE CLOCK SOURCE	0	Selects the analog input sample clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line (Selects TARGET mode) 3 => BCR Input Sync control bit. (See also Triggered Burst, Section 3.12).
D05-D06	R/W	(Reserved)	0	---
D07	RO	BURST BUSY	0	Indicates a burst in progress.
D08-D09	R/W	BURST ON SYNC	0	Selects the **triggered burst** acquisition mode (Section 3.12)
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	(Reserved)	0	---
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	(Reserved)	0	---
D19-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 0C80 (Rate-A), 0000 0050h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Rate Generator Frequency Selection

Nrate (RATE[15..0])		FREQUENCY Fgen (40.000 MHz Master Clock)
(Dec)	(Hex)	(Hz)
200	00C8	200,000
201	00C9	199,005
---	---	Fgen (Hz) = 40,000,000 / Nrate

Table 3.5-1. Input Data Buffer; Nonpacked Data

Offset: 0008h **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16	RO	CHANNEL 00 TAG	Indicates a Channel-00 data value
D17-D31	RO	(Inactive)	---

* RO indicates read-only access. Write-data is ignored.

Table 3.5-2. Input Data Coding; 16-Bit Data

ANALOG INPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	0000 FFFF
Negative Full Scale	0000 0000	0000 8000

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0003 FFFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-D17	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D18	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer and processing pipeline when asserted HIGH.
D19	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D20-D31	RO	(Inactive)	0	---

*Clears automatically within 200ns of being set

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D18	RO	BUFFER SIZE	00000h	Number of locations occupied in the input buffer
D19-D31	RO	(Inactive)	0	---

Table 3.5-5. Analog Input Function Selection (BCR field)

AIM[2:0]	FUNCTION OR MODE
0	System analog input mode (Default mode).
1	(Reserved)
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Table 3.5-6. Active Channel Assignment

Offset: 0000 0024h **Default: 0000 0100h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D07	R/W	FIRST CHANNEL SELECT	0	First (lowest-numbered) active channel
D08-D15	R/W	LAST CHANNEL SELECT	1	Last (highest-numbered) active channel
D16-D31	RO	(Reserved)	0	Inactive. Returns all-zero.

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT EVENT
D00-02	R/W	IRQ0 A0,1,2	0	0	Initialization completed.
				1	Autocalibration operation completed
				2	Input sample initiated (Sync)
				3	Input sample completed (data ready)
				4	Triggered burst initiated (BURST BUSY => HI)
				5	Triggered burst completed (BURST BUSY => LO)
				6-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3	Input buffer overflow or underflow
				4-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

Table 3.8-1. Typical DMA Registers; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.8-2. Typical DMA Registers; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0008h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.9-1. Auxiliary Sync I/O Connections

SIGNAL	PIN *	PMC CONN PIN
AUX-0	1	P1-41
AUX-1	2	P1-42
AUX-2	3	P2-10
AUX-3	4	P2-34
RETURN	5,6	(PCI GND)

* 2-Row 2mm right-angle header.

Table 3.9-2. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

DATA BIT	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-01	R/W	AUX-0 Control Mode	0	AUX-0 I/O Control Mode: 0 => Inactive 1 => Active Input (LO-to-HI edge) 2 => Active Output (Positive pulse) 3 => (Reserved)
D02-03	R/W	AUX-1 Control Mode	0	AUX-1 I/O Control Mode *
D04-05	R/W	(Reserved)	0	---
D06-07	R/W	(Reserved)	0	---
D08	R/W	INVERT INPUTS	0	Active inputs are detected on the LO-to-HI edge when this bit is LOW, or on the HI-to-LO edge when this bit is HIGH.
D09	R/W	INVERT OUTPUTS	0	Active outputs produce HIGH pulses when this bit is LOW, or LOW pulses when this bit is HIGH.
D10	R/W	NOISE SUPPRESSION	0	When LOW, input debounce time is 100ns-135ns and output pulse width is 135ns. When HIGH, input debounce time is 1.5us, and output pulse width is 2.0us.
D11-31	RO	(Reserved)	0	Read-back as all-zero.

* Same configuration as AUX-0.

Table 3.10-1. Board Configuration Register

Offset: 0000 0028h **Default: 000X XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D14	(Reserved status flags)
D15	Product Identification flag: High indicates CCPMC66-16AI32SSA
D16-D17	Channel Availability: 0 => 31 Channels * 1 => 8 Channels 2 => 16 Channels 3 => 32 Channels
D18	Master Clock Frequency: 0 => 40.000MHz 1 => (Reserved)
D19	Input Voltage Range Set:: 0 => ±2.5V, ±1.25V, ±0.625V 1 => ±10V, ±5V, ±2.5V.
D20-D31	(Reserved)

* External Sync-I/O is not available through the P4 connector in the 31-Channel configuration.

Table 3.11-1. Data Packing

	Buffer Data Field					
	ENABLE DATA PACKING = 0 DISABLE SCAN MARKER = X		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 0		ENABLE DATA PACKING = 1 DISABLE SCAN MARKER = 1	
Buffer Lword Order	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**	**D[31..16]**	**D[15..0]**
00	0001h	Chan 00 Data	Upper Marker	Lower Marker	Chan 01 Data	Chan 00 Data
01	0000h	Chan 01 Data	Chan 01 Data	Chan 00 Data	Chan 03 Data	Chan 02 Data
02	0000h	Chan 02 Data	Chan 03 Data	Chan 02 Data	Chan 05 Data	Chan 04 Data
03	0000h	Chan 03 Data	Chan 05 Data	Chan 04 Data	Chan 07 Data	Chan 06 Data
---	---	---	---	---	---	---

Table 3.12-1. Burst Trigger Source

Scan and Sync Register BURST ON SYNC	Burst Trigger Source	Sync I/O Pin
0	Bursting disabled.	(Sample-Clock I/O)
1	Rate-B generator.	Trigger Output *
2	External Sync I/O input pin (or AUX input)	Trigger Input *
3	INPUT SYNC control bit in the BCR.	Trigger Output *

* Independent of BCR control bit ENABLE EXTERNAL SYNC.

APPENDIX B

Migration From PMC66-16AI64SSA

Appendix B

Migration From PMC-16AI64SS

Operation of the CCPMC66-16AI32SSA is similar to that of the PMC66-16AI64SSA. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 provides a brief comparison of PMC66-16AI64SSA and CCPMC66-16AI32SSA features.

Table B.1. PMC66-16AI64SSA, CCPMC66-16AI32SSA Features Comparison

Feature	PMC66-16AI64SSA	CCPMC66-16AI32SSA
Number of Channels	**64**	**32**
Native Input Configuration	**Single-Ended**	**Differential**
Input Ranges	**±10V, ±5V, ±2.5V, 0/+10V, 0/+5V**	**±2.5V, ±1.25V and ±0.625V**
Form Factor	**Air-cooled PMC with front-panel I/O**	**Conduction-cooled PMC with P4 I/O**
Local Clock	**50 MHz**	**40 MHz**
Conversion Resolution	16 Bits	16 Bits
Data Buffer	1M-Byte FIFO	1M-Byte FIFO
Buffer Data Field	32 Active bits	32 Active bits
PCI Interface	PCI 2.3; D32; 33MHz/66MHz	PCI 2.3; D32; 33MHz/66MHz

B.2. Migration Issues

Section 2.0. Installation and Maintenance:

I/O pinouts and the number and type of input channels have changed, as well as the internal reference voltage.

Table 3.1-1. Control and Data Registers:

The default value of the Rate-A generator has changed.

Table 3.2-1. Board Control Register:

Differential processing controls have been eliminated.

Paragraph 3.4-1. Input Voltage Range:

Input voltage ranges have been revised to ±2.5V, ±1.25V and ±0.625V.

Table 3.4-2. Scan and Sync Control Register:

The Active-Channels 64-channel selection is now designated as reserved.

B.2. Migration Issues (Continued)

Paragraph 3.4.4. Sample Rate Generators:

The default master clock frequency has changed from 50MHz to 40MHz.

Paragraph 3.5.4. Active Channel Selection:

References to 64-channel operation have been eliminated.

Paragraph 3.5.5. Differential Processing:

This section has been eliminated entirely due to the native differential input configuration.

Paragraph 3.9. Auxiliary External Sync:

The AUX-2 control mode is now designated as reserved.

Table 3.10-1. Board Configuration Register:

Configuration option flags have changed. Also, the CCPMC66-16AI32SSA carries the same subsystem I.D. as the PMC66-16AI64SSA, and to distinguish between the two products, Bit D15 in the configuration register is always Low for the PMC66-16AI64SSA, and High for the CCPMC66-16AI32SSA.

Revision History; Preliminary Releases:

01-17-2008:	Origination.	Preliminary release.
02-18-2008:	Paragraph 2.2.2:	Revised aux-sync I/O mating connector.
02-22-2008:	Paragraph 2.3.1:	Deleted reference to application acknowledgement of input configuration.
	Paragraph 3.5.2:	Added note clarifying the buffer size register significance with packed data.
03-11-2008:	Paragraph B.2:	Table 3.10-1: Commented on configuration register Bit D15.
	Table 3.4-4:	Correct rate-generator hex values.
04-11-2008:	General:	Miscellaneous editorial corrections.
04-29-2008:	Paragraph 1.1:	Added reference to conduction cooling.
	Paragraph 3.5.2:	Deleted reference to buffer-disable control bit.
	Paragraph 3.9:	Corrected table reference.
	General:	Miscellaneous editorial corrections.
03-09-2009:	Paragraph 1.1:	Added reference to high input range set.
	Tables 3.4-1, 3.10-1:	Added High input range set.
	Table 3.11-1:	Corrected upper bit-range for unmarked packed data.
12-22-2010:	Table 3.2-1:	Added reference to high input range set.

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