General Standards Corporation

High Performance Bus Interface Solutions

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PCIe-24DSI12WRCIEPE

24-BIT, 12-CHANNEL, WIDE-RANGE, 105 KSPS DELTA-SIGMA ANALOG INPUT PCI-Express MODULE with IEPE Transducer Support

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REFERENCE MANUAL

- PRELIMINARY DRAFT-

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PCIe-24DSI12WRCIEPE module provides twelve-channel 24-bit IEPE transducer input capability in the PCI Express short-card form factor, with sample rates up to 105 KSPS per channel. To support the IEPE interface, the module provides constant-current excitation and AC coupling for each input channel. For increased flexibility the inputs can be configured for either AC or DC coupling, thereby accommodating DC-referenced inputs for precision voltage measurements. Multiboard clocking and synchronization also are supported. Input ranges are software-selectable from ±100mV to ±10V. The board is functionally and mechanically compatible with the PCI Express Specification revision 1.0a.

Power requirements consist of +12 VDC and +3.3 VDC from the PCI Express bus in accordance with the specification, and operation over the specified temperature range is achieved with conventional cooling. Specific details of physical and electrical characteristics are contained in the PCIe-24DSI12WRCIEPE product specification. System input and output connections are made through front-panel MMCX coaxial connectors. Figure 1.1 shows the physical configuration of the board, and the general arrangement of major components.

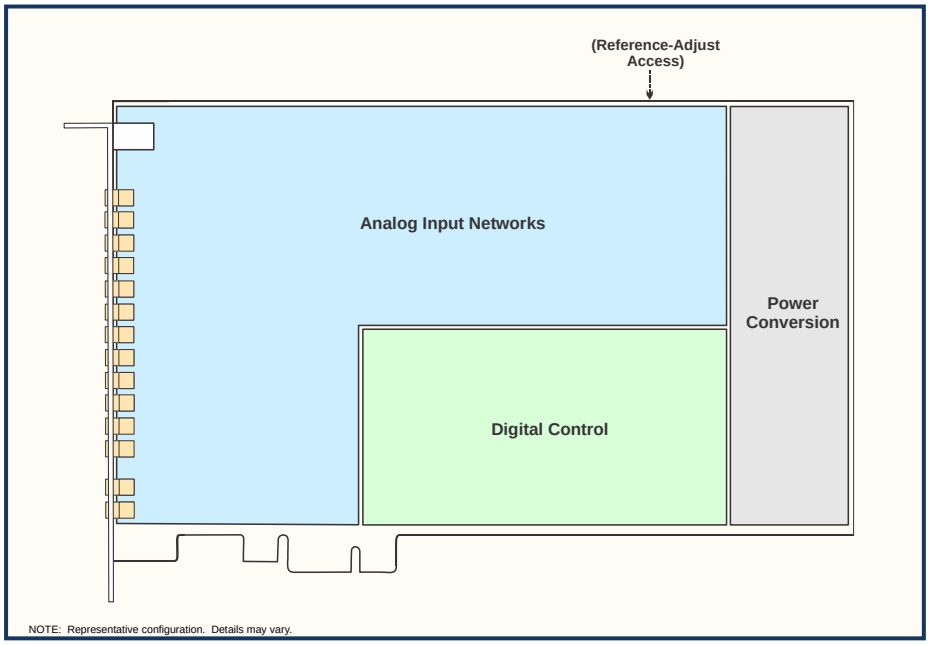

Figure 1.1. Physical Configuration

This product is designed for minimum off-line maintenance. Internal selftest switches permit the calibration and signal integrity of each channel to be verified by the host. An on-demand autocalibration function calibrates all input channels to a single precision internal voltage reference.

1.2 Functional Overview

A PCI Express bus adapter provides the interface between the PCI Express host and the internal local controller through a 32-bit local bus (Figure 1.2). Each input channel contains a dedicated scaling instrumentation amplifier and a 24-Bit delta-sigma A/D converter (ADC) that supports high-resolution data acquisition over a wide range of input levels.

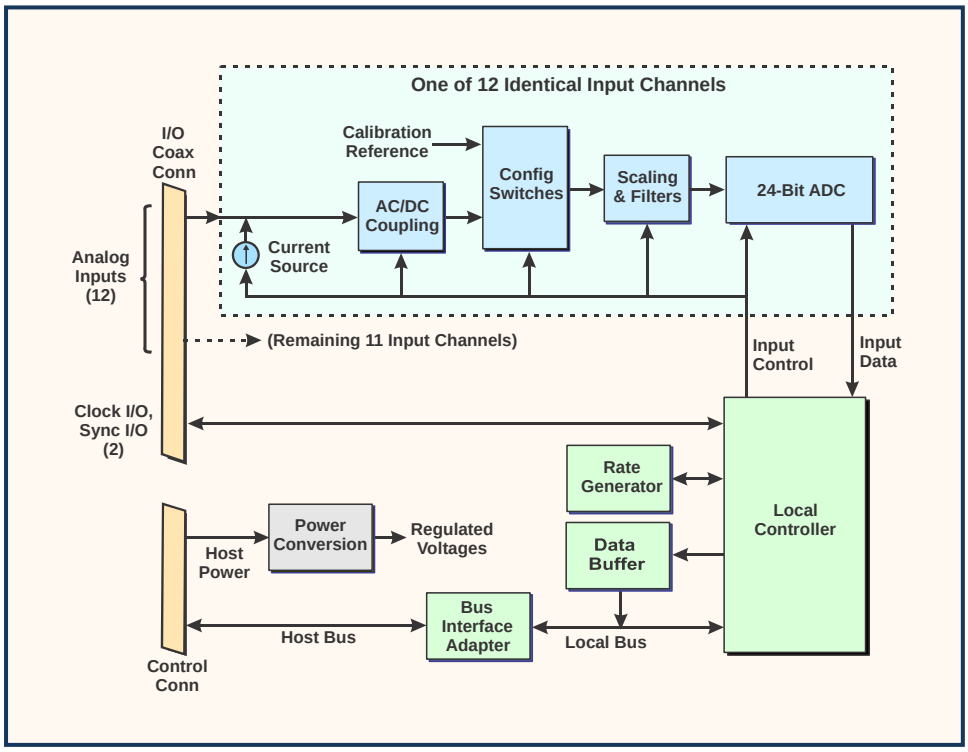

Figure 1.2. Functional Organization

An internal sample-rate clock generator uses an adjustable oscillator to provide sample rates from 0.2 KSPS to 105 KSPS, or an external clock source can control the sample rate over the same range. The input bandwidth extends down to DC. Conversion data from all active channels is transferred to the PCI Express bus through a 256K-sample FIFO data buffer.

Multiple boards can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable electrical or mechanical features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host have been properly discharged to ground.

After removing the board from the shipping package, carefully press the board into position on the host. Verify that the PCI Express connector has mated completely.

Secure the panel bracket fastener carefully to complete the installation. Do not overtighten.

2.2.2 System Cable Connections

System connections are provides through miniature MMCX coaxial receptacle connectors as shown in Figure 2.2.2. Twelve of the connectors accept input connections for the analog input channels, and two connectors support bidirectional external clocking and synchronization signaling.

The front-panel MMCX connectors are designed to mate with Emerson 135-3402-001 for RG-178 coaxial cable, or with 135-3403-001 for RG-316 cable. RG-178 cable is recommended, but RG-316 cable can be used if the associated increase in connector diameter is acceptable.

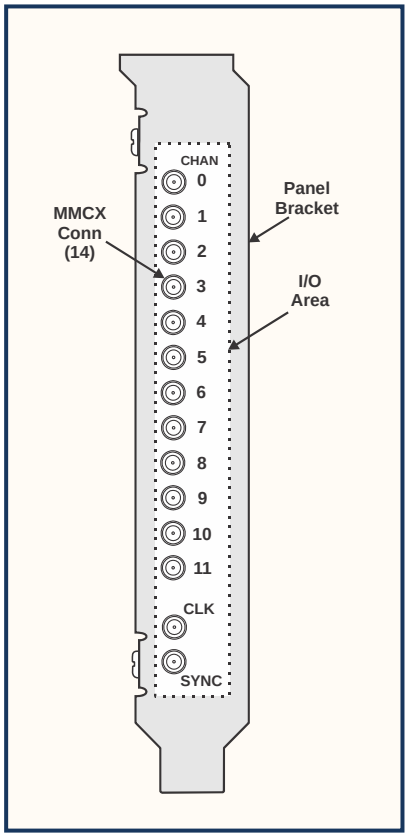

Figure 2.2.2. System I/O Connectors

System I/O Panel Mating Connectors:

Standard MMCX Coaxial cable plug:

Examples: (Straight cable plug, crimp or solder):

Emerson 135-3402-001 (RG-178).

Emerson 135-3403-001 (RG-316),
(O.D. can exceed 0.16 in; 4mm)

An internal I/O connector provides a bidirectional TTL clock and sync interface for implementation within the equipment enclosure. Table 2.2.2 identifies the pin assignments for this connector

Table 2.2.2. Auxiliary Internal Sync I/O Connector

PIN	SIGNAL
1	DIGITAL RTN
2	AUX CLOCK
3	DIGITAL RTN
4	AUX SYNC
5	DIGITAL RTN
6	Reserved. Ground or leave disconnected.

2.3 Analog Input Configuration

The analog inputs are configured as twelve unbalanced differential input pairs. Figure 2.3 illustrates the principal components in a typical input channel. A constant current source provides excitation for an IEPE transducer connected to the coaxial input connector. The current source can be disabled for applications not requiring current excitation. The Low (inverting) side of the input is connected to system ground through Rgnd, which has a typical value of 50 Ohms.

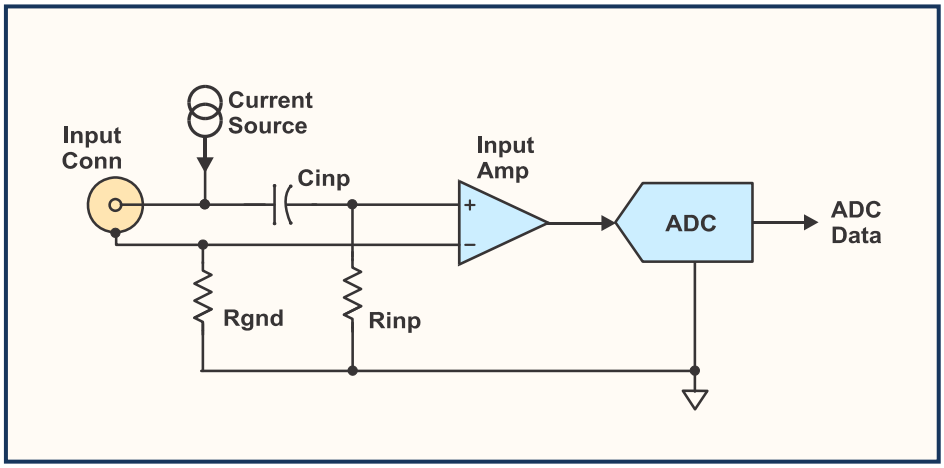

Figure 2.3. Channel Input Configuration

The transducer input signal is AC-coupled through Cinp to the noninverting side of the input amplifier, which in turn drives a 24-Bit ADC. Cinp can be bypassed for applications requiring DC-referenced inputs. Rinp functions in conjunction with Cinp to establish the AC low-frequency cutoff, as well as the input impedance.

2.4 External Clock and Sync I/O

In addition to responding to internal clock and sync functions, the inputs can be clocked and synchronized from external sources through the front-panel coaxial Clock ('CLK') and Sync connectors.

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

External bidirectional clock and trigger signals are single-ended TTL-compatible. When external clock and triggering are software-selected, the sample clock and sync are accepted through the front-panel coaxial Clock and Sync connectors.

2.4.1 Sample Clock I/O

When the board is operated as a ***Clock Initiator***, the bidirectional Clock ('CLK') connector generates a high-frequency reference frequency that can be used to synchronize the sampling of multiple *clock target* boards to a single clock initiator.

In the ***Clock Target*** mode, the Clock connector becomes an input that can accept an external input as a frequency reference for the analog inputs.

2.4.2 Sync I/O

If the board is configured as a ***Sync Target,*** an external input Sync signal can initiate the internal sequence that synchronizes all of the ADC's on the board to sample simultaneously. The Sync input is acknowledged as a Low-to-High transition, in which the Sync signal must remain High for a minimum interval of 100 nanoseconds.

When the board is operated as a ***Sync initiator***, each internal synchronization pulse is duplicated at the Sync connector as a TTL output pulse which is asserted High for 120-180 nanoseconds.

2.4.3 Multiboard Synchronization

If multiple boards are to be synchronized together, the Clock and Sync signals from one board, the ***initiator***, are connected to the corresponding coaxial connectors on one or more ***target*** boards (Figure 2.4.3). The controlling software determines specific clocking and synchronization functions. The maximum number of targets depends upon both static loading and cable characteristics, and can vary from two to as many as three or four. If a large number of targets must be synchronized, then an external clock distribution module might be required.

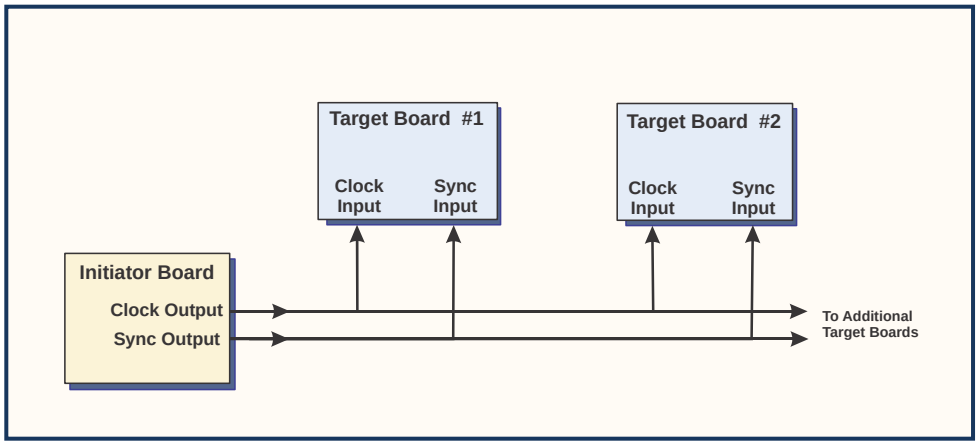

Figure 2.4.3. Multiboard Clock/Sync Connections

The Sync input can be software-configured also to initiate a triggered acquisition burst.

2.5 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended. In the event of a suspected malfunction, all associated system parameters, such as I/O cabling, power voltages, and control bus integrity should be evaluated before a board is returned to the factory for problem analysis and repair.

2.6 Reference Verification and Adjustment

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. This procedure describes the adjustment of the internal reference.

2.6.1 Equipment Required

Table 2.6.1 lists the equipment requirements for calibrating the PCIe-24DSI12WRCIEPE. Alternative equivalent equipment may be used.

Table 2.6.1. Reference Adjustment Equipment

Equipment Description	Manufacturer	Model
Digital Multimeter (DMM), 5-1/2 digit, 0.005% accuracy for DC voltage measurements at +10 Volts.	Hewlett Packard	34401A
Host system with available PCI express single-lane slot	---	---
DMM test leads suitable for connecting to 2mm header pins.	---	---

2.6.2 Adjustment Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. Adjustment of the internal reference (Vtest) is performed with an internal trimmer that is accessible on the top edge of the module, as shown in Figure 1.1. This procedure assumes that the board is installed in an operating system.

1. Connect the digital multimeter between VTEST (+) Pin-3, and REF RTN (-) Pin-4 in the J5 test connector adjacent to the reference adjustment trimmer.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is +9.9000 VDC ±0.0008 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer accordingly.
4. Verification and adjustment are completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

This product is compatible with the PCI Express local bus specification revision 1.0a, and a PLX^{tm} PEX-8311 adapter controls the one-lane interface. Configuration space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization has been completed, communication between the PCI Express bus and the local bus takes place through the control and data registers shown in Table 3.1. All local data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the input data buffer. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written LOW.

Table 3.1. Control and Data Registers

Local Addr [1]	Designation	Access Mode [2]	Default	Primary Function	Ref
00	**Board Control (BCR)**	R/W	0000 381Ch	Board Control Register (BCR)	3.2
04	**Rate Control-A**	R/W	0003 0032h	PLL reference oscillator control integer.	3.6.2
08	**Input Port Configuration**	R/W	0000 0000h	Specifies input parameters associated with the IEPE interface.	3.13
0C	**Clock-Source Assignments**	R/W	0000 0000h	ADC Clock source; Group disables.	3.6.1.2
10	**Rate Divisor**	R/W	0000 0005h	Sample rate divisor.	3.6.1.3
14	(Reserved)	R/W	0000 0000h	---	---
18	(Reserved)	RO	0000 0000h	---	---
1C	**Burst Block Size**	R/W	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.14
20	**Buffer Control**	R/W	0003 FFFEh	Input buffer control and status	3.5.3
24	**Board Configuration**	RO	00XX XXXXh	Installed firmware and hardware options	3.10
28	**Buffer Size**	RO	000X XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	Autocal Values [3]	R/W	---	---	---
30	**Input Data Buffer**	RO (DMA)	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	**Auxiliary Sync I/O Control**	R/W	0000 0000h	Auxiliary external Clock and Sync control.	3.12
38	(Reserved)	R/W	0000 0000h	---	---
3C	**Burst Trigger Timer**	R/W	0000 C000h	Internal trigger timer rate divisor	3.14
40-7C	(Reserved)	---	---	---	---

[1] Offsets from the PCI base address for local addressing.
[2] R/W = Read/Write; RO = Read-Only.
[3] Maintenance register; Shown for reference only

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and input range selections, and supports up to 32 control bits and status flags (Table 3.2). Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 381Ch**

Data Bit	Designation	Mode	Def	Function	Ref
D00	AIM0	R/W	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D01	AIM1				
D02	RANGE0	R/W	3h	Analog input range selection. Defaults to ±10V range.	3.4.2
D03	RANGE1				
D04	OFFSET BINARY	R/W	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	CLOCK INITIATOR	R/W	0	Selects INITIATOR or TARGET mode for external clock input/output signals. Defaults Low to Target mode to prevent line conflicts at initialization.	3.6.5
D06	SOFTWARE SYNC [1]	R/W	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.5.3.2, 3.6.4
D07	AUTOCAL [1]	R/W	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08	INTERRUPT A0	R/W	0h	Interrupt event selection. Default is zero.	3.8
D09	INTERRUPT A1	R/W			
D10	INTERRUPT A2	R/W			
D11	INTERRUPT REQUEST FLAG	R/W	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	AUTOCAL PASS	RO	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	CHANNELS READY	RO	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	BUFFER THRESHOLD FLAG	RO	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	INITIALIZE [1]	R/W	0	Initializes the board when asserted. Sets all defaults.	3.3.2
D16	ENABLE TRIGGER TIMER	R/W	0	Enables the internal burst trigger timer.	3.14
D17	CLEAR BUFFER ON SYNC	R/W	0	Changes the context of the SOFTWARE SYNC to CLEAR BUFFER.	3.5.3.2
D18	RATE GEN EXT CLOCK OUT (Initiator Mode only)	R/W	0	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock.	3.6.5.1
D19	HIGH SPEED ADC MODE	R/W	0	Selects the ADC High-Speed mode when HIGH, or the High-Resolution Mode when LOW.	3.6.1.3
D20	SYNC INITIATOR	R/W	0	Selects INITIATOR or TARGET mode for external Sync input/output signals. Defaults Low to Target mode to prevent line conflicts at initialization.	3.6.5
D21	ENABLE INPUT BURST	R/W	0	Selects triggered-burst acquisition when HIGH.	3.14
D22	S/W BURST TRIGGER	R/W	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	3.14
D23	EXTERNAL SYNC INPUT	R/W	0	Configures the Sync I/O connecter as the Sync source. 'Requires the SYNC INITIATOR control bit to be HIGH.	3.6.5.2
D24-31	(Reserved)	RO	0h	---	---

[1] Clears automatically.

3.3 Configuration and Initialization

3.3.1 Configuration

Board configuration is initiated by a PCI Express bus RESET, which should be required only once after the initial application of power. During configuration, initial values for both the PCI Express configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI Express configuration registers are being loaded, the response to PCI Express target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration and Initialization Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	20 ms
Settling delay for AC-coupled inputs	**5 seconds**

3.3.2 Initialization

Internal control logic can be initialized without invoking control logic configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of **5 seconds**, and produces the following conditions:

- Excitation current is disabled (3.13).
- AC coupling is selected (3.13),
- The Initiator mode is selected, (3.6.5.1),
- The width of the buffer data field is adjusted to 16 bits (3.5.2),
- The input buffer is disabled; Acquisition is suspended (3.5.3.2),
- The internal Rate-A generator is the ADC clock source (3.6.1),
- Internal rate generator frequency is 51.200 MHz (3.6.2),
- Rate divisor is preset to 5, and High-Resolution sampling is selected (3.2, 3.6.1.3),
- Sample rate is 10.0 KSPS (3.6.1),
- The internal burst-trigger timer is adjusted to 1.00 kHz (3.14.2),
- The analog input buffer is reset to empty; buffer threshold equals 0003 FFFEh (3.5.3),
- Analog inputs are configured for ±10 Volt operation (3.4.2),
- All control registers are initialized; all defaults are invoked (3.3.2),
- The local interrupt request is asserted as an initialization-completed event (3.8).

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[1..0], the effects of which are summarized in Table 3.4. The analog input selection arranges all input channels in differential configuration during normal operation, or invokes one of two selftest modes.

To prevent the input amplifiers from being overdriven inadvertently, the +VREF test signal is disabled for all ranges except the highest range.

Table 3.4. Analog Input Function Selection

AIM[1..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

NOTE: The input configuration is also controlled by the IEPE control register (3.13).

3.4.1 Selftest Modes

Two selftest modes verify the accuracy of any or all input channels by replacing the system input connections with either a precision internal reference voltage (+VREF) or a zero reference (ZERO). ***The +VREF test applies a precision test voltage of +9.900V to all input channels only on the ±10V input range, and Zero (0.0000V) on all other ranges.*** The ZERO test applies a value of 0.0000 Volts on all ranges. The accuracy of selftest measurements should correspond to the product accuracy specification.

NOTE: For maximum test accuracy, the internal reference voltage must be allowed to settle completely when the test mode is changed. After selecting either of these test modes, insert a minimum settling delay of 100 milliseconds before acquiring test values:

The selftest modes require DC coupling (3.13). If AC coupling is selected when entering selftest, the DC coupling mode will be selected automatically, and AC coupling will be restored when selftest is completed. Consequently, the AC coupling delay will be invoked after selftestl, during which the CHANNELS READY flag will be deasserted. No delay is invoked if DC coupling is selected when entering selftest.

3.4.2 Input Range Selection

Any one of four input voltage ranges can be selected for all input channels. RANGE[1..0] control bits in the BCR select the input range, as shown in Table 3.4.2.

Table 3.4.2. Analog Input Range Selection

RANGE[1..0]	Standard Input Range
0	±10mV
1	±100mV
2	±1.0V
3	±10V

NOTE: Overdriving the inputs by more than 20-percent beyond the selected input range can cause increased input leakage current. Overdriving beyond 50-percent will increase internal power supply loading and possibly cause corrupted data.

3.4.3 Settling Delays and the Channels-Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate intervals indicated:

5 Seconds:	**Board initialization (3.3),**
10 us-20 ms:	Buffer reset; Sample-rate dependent (3.5.3.2).
20 ms:	Modified sample rate parameter ; i.e.: Nrate, Ndiv, Clock source.
2-700 ms:	ADC synchronization (3.6.5.2), or Speed-mode change (3.6.1.3).

NOTE: The Channels Ready flag is deasserted for 5 seconds after AC coupling is selected or after Excitation Current is enabled (3.13), in order to allow the AC coupled inputs to settle.

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO buffer, which has a capacity of 256K (262,144) data values. Data accumulates in the buffer until extracted by the host bus from a single register location, indicated as 'Input Data Buffer' in Table 3.1. Reading an empty buffer returns an indeterminate value. For each input sample set, data is arranged with Channel-00 appearing first, and the highest-numbered active channel appearing last.

3.5.2 Data Organization

Each value in the data buffer consists of a 4-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the DATA WIDTH control field in the buffer control register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Selected Data Width	Reserved (Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..28]	D[27..24]	D[23..16]	D[15..0]
18 Bits	D[31..28]	D[27..24]	D[23..18]	D[17..0]
20 Bits	D[31..28]	D[27..24]	D[23..20]	D[19..0]
24 Bits	D[31..28]	D[27..24]	---	D[23..0]

3.5.2.1 Channel Tags

A channel tag that identifies each input channel is attached to each data value in the buffer. This tag value equals the associated input channel number. The channel tag can be eliminated by setting the DISABLE CHANNEL TAG control bit in the Buffer Control Register.

3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +10.000 Volts for the ±10V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR*)* is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 305.175 microvolts for the ±10V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3) contains the threshold value for the buffer threshold flag in the BCR, and also provides control bits for clearing the buffer and for disabling the buffer input.

NOTE: Since delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Enable' controls.

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer can be used to control the BCR status bit BUFFER THRESHOLD FLAG, which can be selected as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh**

Bit Field	Mode	Designation	Def	Function
D[18..00]	R/W	BUFFER THRESHOLD	0003 FFFEh	Buffer Flag Threshold
D[19]	R/W	ENABLE BUFFER INPUT	0	Enables ADC inputs to the buffer.
D[20]	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer. Asserted HIGH while the buffer is cleared, either locally or externally.
D[22..21]	R/W	DATA WIDTH	0	Controls the width of the buffer data field: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23]	R/W	DISABLE CHANNEL TAG	0	Replaces the channel tag with a zero-field.
D[24]	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW [2]	0	Reports buffer underflow (Read on empty)
D[31..26]	RO	(Reserved)	0h	---

[1] Clears automatically. [2] Cleared by writing LOW, or by Initialization.

3.5.3.2 Buffer Clearing and Enabling/Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer, and holds the buffer in reset until the ADC data pipeline clears. The buffer-clear delay is less than 10 **milliseconds; typically 5 milliseconds**. This bit clears automatically, but is held HIGH while the buffer is being cleared.

Asserting the ENABLE BUFFER INPUT control bit enables inputs to the buffer from the ADC input channels, and initiates the accumulation of input data. Clearing this control bit disables the buffer and suspends sample acquisition. Input data already present in the buffer when this bit is deasserted remains in the buffer.

Buffer enabling and disabling operations both are synchronous with the input data stream. That is, regardless of when the enabling control bit is set or cleared, actual enabling of the buffer always occurs immediately prior to a complete sample set arriving, and disabling always occurs immediately after the last active channel in a sample set is loaded into the buffer.

NOTE: Global Buffer Clear:

The buffer also can be cleared by writing a "one" to the SOFTWARE SYNC control bit in the BCR when the CLEAR BUFFER ON SYNC control bit is HIGH. For multiple synchronized boards:

1. On all boards: Set the CLEAR BUFFER ON SYNC bit,
2. On the Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on the initiator.
   (All ADC's and buffers are now scan-synchronized).
3. On all boards: Clear the CLEAR BUFFER ON SYNC bit.

3.5.4 Buffer Size Register

This read-only register listed in Table 3.1 contains the number of analog input values currently stored in the input data buffer, from zero to 262144 (40000h).

3.5.5 Buffer Underflow and Overflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared either by writing LOW directly, or by Initialization.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Sample rate,
b. Phase, or skew,
c. Channel synchronization.

The effective input bandwidth is determined by the sample rate, while phase and synchronization control the relative timing of sampling between multiple channels. Phase and synchronization are considerations in applications that require consistent relative timing of sampling among multiple channels or multiple boards.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

NOTE: It is critically important that the inputs always be synchronized (3.6.4) after changing any parameter that affects the sample rate. Failure to do so can cause the general corruption of input data. Any change to the Rate-A control, Clock Source Assignments, Rate Divisor or the High Speed/Resolution mode will initiate an automatic synchronization sequence. However any sample-rate change, especially from an external source, should still be followed by synchronization through the BCR.

3.6.1 Sample Rate Control

3.6.1.1 Sample Clock Organization

Sample rates are derived either from an adjustable internal rate generator, or from a single external hardware clock, as shown in Figure 3.6.1.1. The input channels are divided into two equal groups (Table 3.6.1.1), and all active input channels operate from the same clocking source. Group-1 can be independently designated as either active (enabled) or inactive (disabled). The sample rate for both channel groups is controlled by the following operations:

a. Assignment of both groups to the internal rate generator or to an external clock,
b. Rate generator frequency selection, if the internal rate source is selected,
c. Rate divisor selection, unless the Direct External Sample Clock is selected.

The number of channels per group is reduced to four channels for 8-channel boards, or to two channels for 4-Channel boards. This scheme ensures that the board is partitioned into two equal channel groups, regardless of the number of channels present on a board.

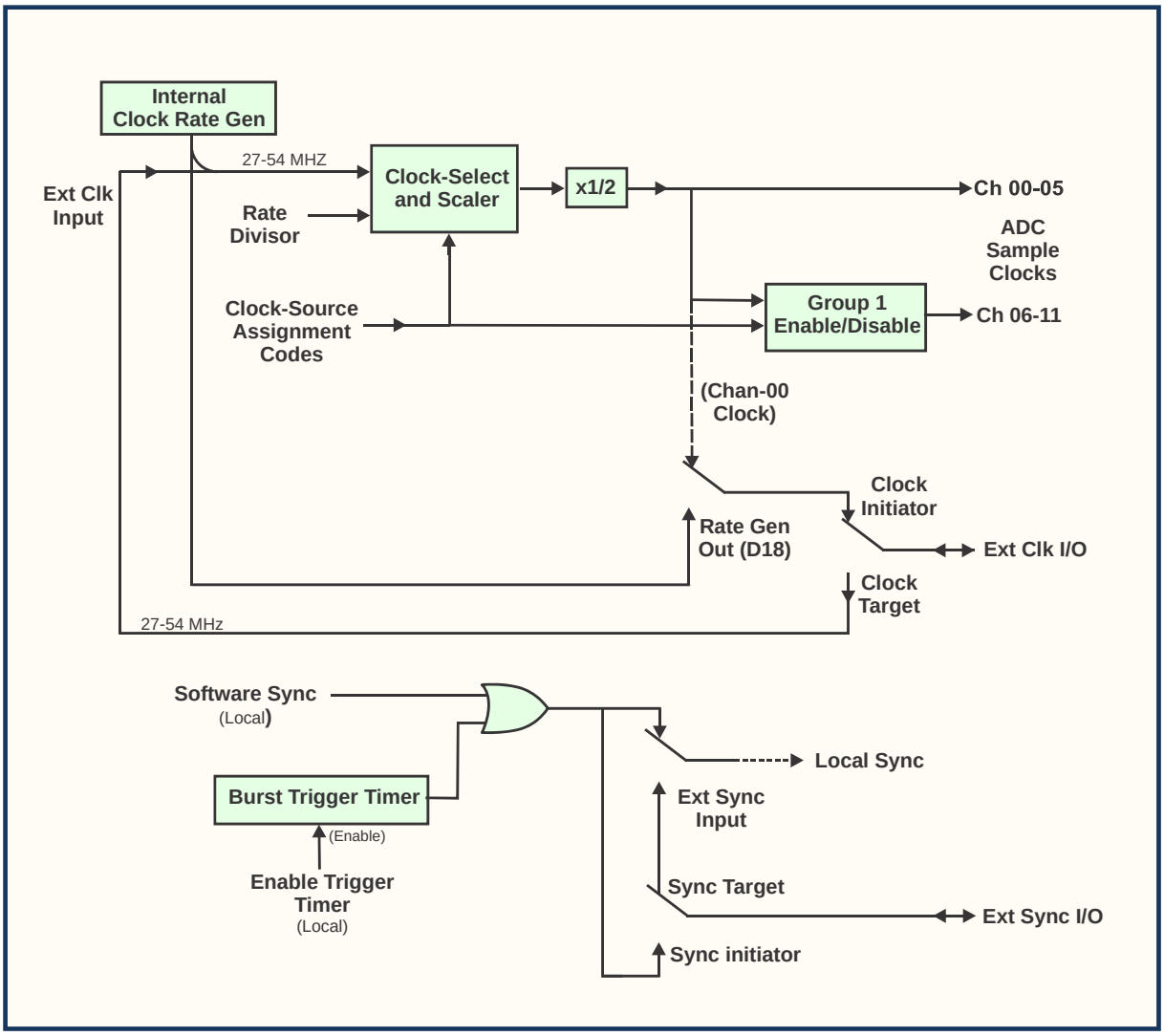

Figure 3.6.1.1. ADC Clock and Sync Organization, 12 Channels

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	12-CHAN BOARD	8-CHAN BOARD	4-CHAN BOARD
0	Channels 00-05	00-03	00, 01
1	Channels 06-11	04-07	02, 03

3.6.1.2 Clock Source Assignment

A 4-bit code CLOCK SOURCE in the Clock Source Assignments register (Table 3.6.1.2-1) selects either the internal rate generator or the external sample rate clock as sample rate source. Group selection codes are arranged in the register as shown in the table, and use the assignment codes listed in Table 3.6.1.2-2. ***The Group-0 assignment selects the sample rate source for both groups***, while the Group-1 assignment simply enables or disables the group. A disabled group does not provide data to the input data buffer.

Table 3.6.1.2-1. Clock-Source Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 CLOCK SOURCE	0
D[07..04]	GROUP 1 CLOCK SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Clock-Source Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT	GROUP 1 ASSIGNMENT
0	Internal Rate Generator *	No effect. (Same as Group-0)
1-3	(Reserved)	
4	External Sample Clock (as rate generator input)	
5	Direct External Sample Clock (routed directly to ADC)	
6	**Invalid**	**Disabled**
7-15	(Reserved)	(Reserved)

* Applies to both channel groups. Disabling Group-0 disables both groups.

NOTE: Disabled channels will fail autocalibration (3.7). Ensure that both clocking groups are enabled during autocalibration.

3.6.1.3 Sample Clock Generation

The ADC's operate in one of two sampling modes, the High-Resolution mode or the High-Speed mode, selected by the HIGH SPEED ADC MODE control bit in the BCR. The sample rate range is 0.4-105KSPS in the High-speed mode, or 0.2-52.5KSPS in the High-Resolution mode. The signal-to-noise ratio (SNR) is approximately 3dB higher in the High-Resolution mode, when compared with High-Speed mode performance.

A rate divisor integer **Ndiv** (Table 3.6.1.3-1) controls a *rate divisor* for the rate generator or external clock input.

Table 3.6.1.3-1. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0005h**

BIT FIELD:	DESIGNATION	FUNCTION
D[08..00]	RATE DIVISOR (**Ndiv)**	Prescales the rate generator input frequency.
D[31..9]	(Reserved)	---

NOTE: Changing the state of the HIGH SPEED ADC MODE control bit forces a buffer reset and deasserts the CHANNELS READY status flag (3.4.3) for approximately 140 ADC sample periods.

The ADC sample rate **Fsamp** is determined by a rate generator frequency **Fgen** and rate divisor **Ndiv** as: (all values shown in decimal)

$$\textbf{Fsamp (High-Speed)} = \frac{\textbf{Fgen}}{\textbf{Ndiv * 512}}, \qquad \textbf{(3-1a)}$$

$$\textbf{Fsamp (High-Resolution)} = \frac{\textbf{Fgen}}{\textbf{Ndiv * 1024}}, \qquad \textbf{(3-1b)}$$

where **Fsamp** and **Fgen** are in kilohertz, and **Ndiv** is an integer. **Fgen** has a nominal range of 27-54 MHz, and **Ndiv** can have any integer value from 1-300.

NOTE: These relationships take into account the 2:1 division of the ADC sample clock frequency shown in Figure 3.6.1.1. This 2:1 division ensures a 50-percent duty cycle at the ADCs.

Table 3.6.1.3-2. Sample-Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz nominal range
Rate Divisor	**Ndiv**	1-300
Sample Rate Range	**High-Speed Mode**	0.4 - 105 KSPS
	High-Resolution Mode	0.2 - 52.5 KSPS

3.6.2 Rate Generator Control

The internal rate generator is a PLL-controlled oscillator that is phase-locked to a stable reference frequency. The frequency of the generator is controlled by the Rate Control-A register listed in Table 3.1, and shown in Table 3.6.2-1.

Fgen can be obtained either externally through the system I/O connector (3.6.5) or from the internal phase-locked loop (PLL) oscillator, and has a nominal frequency range of 27-54 MHz. The frequency **Fgen** of the internal oscillator is related to a reference frequency **Fref** by integers **Nref** and **Nvco** as:

$$\mathbf{Fgen} = \mathbf{Fref} * \frac{\mathbf{Nvco}}{\mathbf{Nref}} \quad , \qquad \textbf{(3-2)}$$

where **Nvco** and **Nref** each has a maximum range from 25 to 300, with the optimum range being 30-200 (Very low values can create stability issues, and very high values will spread the oscillator spectrum). **Fref** is the frequency of the reference oscillator, which has a standard frequency of **49.152MHz**. Table 3.6.2-2 summarizes the rate generator control parameters.

NOTE: The nominal range of Fgen (27-54 MHz) and an Fref value of 49.152MHz imply a valid range of 0.55-1.10 for the ratio Nvco/Nref.

Table 3.6.2-1. Rate Generator Control Register

Offset: 0004h **Default: 0003 0032h**

BIT FIELD	MODE	DESIGNATION	FUNCTION *
D[11..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 25-300.
D[23..12]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 25-300.
D[31..24]	R/W	(Reserved)	---

* For maximum phase stability, select the lowest possible values for Nvco and Nref.

NOTE: Nvco and Nref each has a maximum range from 25 to 300. For optimum performance (lowest noise), select the *lowest* possible values for Nvco and Nref.

By combining Equation 3-2 with 3-1a and 3.1b:

$$\mathbf{Fsamp\ (High\text{-}Speed)} = \frac{\mathbf{Fref}}{\mathbf{Ndiv} * \mathbf{512}} * \frac{\mathbf{Nvco}}{\mathbf{Nref}} \quad , \qquad \textbf{(3-3a)}$$

$$\mathbf{Fsamp\ (High\text{-}Resolution)} = \frac{\mathbf{Fref}}{\mathbf{Ndiv} * \mathbf{1024}} * \frac{\mathbf{Nvco}}{\mathbf{Nref}} \quad , \qquad \textbf{(3-3b)}$$

where **Fsamp** and **Fref** are in kilohertz, and **Ndiv, Nvco** and **Nref** are integers. Table 3.6.2-2 summarizes the acceptable ranges for these control parameters.

Table 3.6.2-2. Rate-Generator Control Parameters

PARAMETER	NOTATION	NOMINAL RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz
Reference Frequency	**Fref**	Standard value = 49.152 MHz
VCO Factor	**Nvco**	25-300; Optimum at 30-200.
Reference Factor	**Nref**	25-300; Optimum at 30-200.
Nvco/Nref Factor Ratio	**Nvco/Nref**	0.55-1.10

To establish a specific sample rate Fsamp, determine the in-range values of **Ndiv**, **Nvco** and **Nref** that produce the closest available rate. For the best SNR performance, use the High-Resolution sampling mode if possible.

Table 3.6.2-3. Sample Rate Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)	Ndiv	MODE (BCR)
0.200	30	30	49.1520	240	High-Resolution
1.000	30	30	49.1520	48	(Fsamp = Fgen/1024Ndiv)
10.000	50	48	51.2000	5	
20.000	30	36	40.9600	2	
50.000	50	48	51.2000	2	High-Speed
100.000	50	48	51.2000	1	(Fsamp = Fgen/512Ndiv)
102.400	32	30	52.4288	1	
105.000	35	32	53.7600	1	

Fref = 49.152MHz. All values shown in decimal format.

3.6.3 Direct External Clocking

If the rate assignment selection (Table 3.6.1.2-2) is "Direct External Sample Clock", and if Clock Target is selected, the signal at the external clock input is routed directly to the ADC's without modification. This configuration eliminates the effect of the **Ndiv**, **Nvco** and **Nref** control variables, and gives the external clock source direct control of the ADC's.

Although the variables **Ndiv**, **Nvco** and **Nref** have no effect in this configuration, the sampling mode of the ADC's still must be controlled by the HIGH SPEED ADC MODE control bit in the BCR. In general, all boards operating in a multiboard synchronization configuration will use the same value for this control bit.

3.6.4 Channel Synchronization

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously if operating from a common clock.

Synchronization is invoked by setting the SOFTWARE SYNC control bit HIGH in the BCR. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition (Paragraph 3.4.3). The CHANNELS READY transition can be selected as a condition for an interrupt request event.

NOTE: It is critically important that the inputs always be synchronized after changing any parameter that affects the sample rate. Failure to do so can cause the general corruption of input data. Any change to the Rate-A control, Clock Source Assignments, Rate Divisor or the High Speed/Resolution mode will initiate an automatic synchronization sequence. However any sample-rate change, especially from an external source, should still be followed by synchronization through the BCR.

3.6.5 Multiboard Operation

Multiple PCIe-24DSI12WRCIEPE boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*. A board is designated as a clock and sync initiator by setting the CLOCK INITIATOR and SYNC INITIATOR control bits HIGH in the BCR, or as a target when the control bits are LOW.

NOTE: The Clock and Sync Initiator and Target modes are independent of each other, and a board can be a Clock Target and a Sync Initiator, or a Clock Initiator and a Sync Target.

External clock and sync inputs can be provided from TTL sources other than an initiator board.

NOTE: The Clock and Sync Initiator control bits establish the signal direction in the associated I/O connectors. Both bits default LOW to the target mode, in order to avoid possible line conflicts from occurring at initialization.

3.6.5.1 External Sample Clock

Clock Target boards receive an external clock from the bidirectional external clock I/O connector (Figure 3.6.1.1). The external clock input is designated as the clocking source by writing either the "External Sample Clock" or "Direct External Sample Clock" assignment code to each target board's Clock-Source Assignments register (Table 3.6.1.2-2), and by clearing the CLOCK INITIATOR control bit in the BCR. For calculation of target board sample rates, the external sample clock corresponds to the rate generator frequency **Fgen** described in Section 3.6.1 if "External Sample Clock" is selected, or provides the ADC sample clock directly if "Direct External Sample Clock" is selected.

A ***Clock initiator*** configures the Clock I/O connector as an output, and provides an external clock output from either of two sources. If the RATE GEN EXT CLOCK OUT control bit in the BCR is LOW (default), the external clock output frequency equals twice the Group 00 ADC sample clock frequency, and is the internal rate generator output divided by the rate divisor. If the control bit is HIGH, the internal rate generator's unmodified output provides the external clock.

Multiple boards can all be configured as targets and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the source driver, an external clock distribution module might be required.

3.6.5.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board. During synchronization, all ADC's are reset and initialized in a sequence that requires approximately 140 sample intervals for completion. The data buffers also are reset during the sequence, at the end of which, all channels on all boards are synchronized to within one sample clock interval, and all data buffers commence acquiring data simultaneously.

A S*ync Target* is established by clearing the SYNC INITIATOR control bit LOW in the BCR, and setting the EXTERNAL SYNC INPUT control bit HIGH.

A *Sync Initiator* is established by setting the SYNC INITIATOR control bit HIGH, and clearing the EXTERNAL SYNC INPUT control bit LOW.

The "CHANNELS READY flag is deasserted on all boards during the synchronization sequence, and returns HIGH when all boards are synchronized and commence acquiring data.

NOTE: A "sample clock interval" is the period of the ADC sample clock (1/Fgen) while the "sample interval" is the interval between data samples (1/Fsamp) and is 256-512 times the sample clock interval.

The SOFTWARE SYNC control bit in the BCR can be used also to clear the buffers on the ***Sync Initiator*** and ***Sync Target*** boards simultaneously without executing a full synchronization sequence, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR. This process requires 4-5 sample intervals for completion. ***If implemented, the CLEAR BUFFER ON SYNC control bit must be asserted on the initiator and all targets.***

For very low-frequency sample clocks, the synchronization interval can approach one second. Notice that in the absence of an ADC clock, the synchronization or buffer-clear interval will be indefinitely long.

Refer to Paragraph 3.14 if burst-triggering is to be implemented.

3.7 Autocalibration

Autocalibration is an embedded utility that calibrates all input channels to a single internal voltage reference. Offset and gain error corrections for each channel are determined and stored during autocalibration, and then are applied to each channel in real-time during data acquisition. The correction values are retained until either: (a) power is removed, (b) a PCI reset occurs, or (c) autocalibration is invoked again. Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. Completion of autocalibration is indicated by the AUTOCAL flag clearing automatically to the LOW state. The end of autocalibration is selectable as an interrupt request event (3.8.1). Autocalibration calibrates all channels on all ranges in a single sequence.

An autocalibration sequence can have a duration from 1 to 45 seconds, depending upon the selected sample rate and the number of active channels. For 12 active channels, the ***approximate*** autocal duration is

$$\mathbf{T_{autocal}\ (seconds) = 1 + (9{,}000/Fsamp),}$$

where Fsamp is the selected sample rate in samples-per-second. For example:

$T_{autocal}$ @ 10ksps = 1 + (9,000/10,000) ~= 1.9 Seconds.
$T_{autocal}$ @ 400sps = 1 + (9,000/400) ~= 24 Seconds.

The input coupling mode (3.13) also affects the effective autocal duration, since autocalibration requires DC coupling. If AC coupling is selected when entering autocal, the DC coupling mode will be forced during the calibration sequence, and AC coupling will be restored when autocal is completed. Consequently, the AC coupling delay will be invoked after autocal, during which the CHANNELS READY flag will be deasserted. No delay is invoked if DC coupling is selected when entering autocal.

Read or write access from the PCI Express bus during autocalibration could disrupt the calibration process, and should be avoided. Either a suitable delay or the "Autocal Completed" interrupt should be used to detect the end of autocalibration.

If a board is defective, the autocalibration process may be unable to successfully calibrate all input channels. If this situation occurs, the AUTOCAL PASS status flag in the BCR will be LOW when the autocal sequence is completed. A HIGH state for AUTOCAL PASS indicates that autocalibration was successful for all channels.

To ensure full conformance to the product specification, autocalibration should always be invoked after:

(a). Power has been applied to the board,

(b). A PCI reset event has occurred,

(c). The clock source or sampling rate has been altered.

Autocalibration can be invoked at any time, but should not occur while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied. For optimum performance, a warmup delay of 15 minutes is recommended.

NOTE: Disabled channels will fail autocalibration. Ensure that both clocking groups are enabled during autocalibration (3.6.1.2).

3.8 Interrupt Control

In order for the board to generate a PCI Express interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI Express interrupt emulation* must be enabled.

If the internal controller generates a local interrupt request, a PCI Express interrupt will not occur unless the PCI Express interrupt has been enabled.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI Express bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	(Reserved)
7	(Reserved)

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI Express bus unless interrupt emulation is enabled. Refer to the PEX-8311 reference manual for details pertaining to this function.

3.9 DMA Operation

DMA transfers from the analog input FIFO buffer are supported in either **block-mode** or **demand mode**, with the board operating as bus master. Demand mode operation requires the ***slow terminate*** mode. Refer to the PEX-8311 reference manual for a detailed description of the associated DMA configuration registers.

NOTE: The PEX-8311 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PEX-8311 adapter to the PCI Express bus, and no samples are lost.

3.10 Board Configuration Register

The read-only board configuration register (Table 3.10.1) contains the existing firmware revision, and a status field that indicates the availability of optional features.

Table 3.10.1. Board Configuration Register

Offset: 0000 0024h **Default: 0000 XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D17	Number of input channels: 0 => 12 Channels 1 => 8 Channels 2 => 4 Channels 3 => (Reserved)
D18-D19	Image Filter Frequency: 0 => 150kHz 1 => No filter. 2-3 => (Reserved)
D20-D21	AC Cutoff Frequency: 0 => 0.5 Hz 1 => 2 Hz 2-3 => (Reserved)
D22-D23	Excitation Current:: 0 => 4mA 1-3 => (Reserved)
D24-D31	(Reserved; all-zero)

3.11 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance might be suspended. Abrupt changes include:

- A change in voltage range, or selection of AC input coupling,
- A major input step-change,
- Transitioning into or out of a selftest mode, or out of autocalibration,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes, specified performance should resume after a settling interval of 20-100 milliseconds.

NOTE: The Channels Ready flag is deasserted for 5 seconds after AC coupling is selected or after Excitation Current is enabled, in order to allow the AC coupled inputs to settle.

3.12 Auxiliary External Clock and Sync I/O

Two auxiliary external connections provide an alternate method of synchronizing sample clocking to external events. These bidirectional TTL connections are available as AUX CLOCK and AUX SYNC (Table 2.2.2), and when active *as inputs*, replace the corresponding external EXT CLK I/O and EXT SYNC I/O inputs in the system I/O connector. The AUX I/O signals are accessible through a 6-Pin header on the board.

AUX clock and sync signals are designated independently through the Auxiliary Sync I/O Control register as inputs, outputs, or inactive, as indicated in Table 3.12. When an AUX signal is designated as an ***input***, the signal replaces the corresponding CLK INP or SYNC INP input from the system connectors. The AUX I/O pins are pulled up internally to +3.3VDC through 33K.

Table 3.12. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input 2, 3 => Active Output
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode 0 => Inactive 1 => Active Input 2, 3 => Active Output
D04-31	RO	(Reserved)	0	Read-back as all-zero.

In order for Aux inputs to be acknowledged, in addition to making the appropriate 'active' selections in Table 3.12, "External Sample Clock" must be selected with the Clock-Source Assignment code (Table 3.6.1.2-2), and EXTERNAL SYNC INPUT must be HIGH in the BCR.

The AUX *CLOCK* and AUX SYNC ***as active outputs,*** duplicate the CLOCK and SYNC I/O signals respectively in the associated front-panel coaxial connectors, ***but are not affected by the CLOCK INITIATOR and SYNC INTIATOR control bits in the BCR***.

3.13 Controlling the IEPE Interface

IEPE (Integrated Electronics Piezoelectric) transducers usually require a constant excitation current for power, as well as an AC-coupled input to reject the transducers DC output bias. These parameters are controlled through the Input Port Configuration register shown in Table 3.13.

Although AC coupling usually is required in IEPE applications, the DC coupling capability also is provided for related situations requiring precision voltage acquisition. The DC COUPLING control bit selects either AC or DC coupling, and defaults LOW to AC coupling.

NOTE: The normal input mode for this product is AC coupling. When DC coupling is selected, the inputs are protected only to ±15V with power applied, or to ±2V with power removed. Excitation current should be disabled if DC coupling is selected unless the resistance of the input device is low enough to ensure that the input voltage does not exceed ±15V

Table 3.13. Input Port Configuration Register

Offset: 0000 0008h **Default: 0000 0000h**

Control Bit:	Designation	Def	Function	Normal IEPE State
D[00]	DC COUPLING	0	Configures the inputs for AC coupling when LOW, or for DC coupling when High.	Low
D[01]	EXCITATION CURRENT	0	Provides excitation current to all inputs when HIGH. Disables the current sources when LOW.	High
D[02]	INPUT COMPENSATION	0	Inserts line compensation to stabilize very long transducer cables. Limits input bandwidth to approximately 50kHz.	Low
D[03]	Aux Current *	0	Diagnostic; Injects a coarse constant current to all inputs when High, or has no effect when Low.	Low
D[31..04]	(Reserved)	---	---	---

* Diagnostic control bit for factory testing. Leave in the LOW state.

Excitation current is enabled or disabled by the EXCITATION CURRENT control bit. This bit defaults LOW to prevent excitation current from being applied during the initialization sequence.

NOTE: The Channels Ready flag is deasserted for 5 seconds after AC coupling is selected or after Excitation Current is enabled, in order to allow the AC coupled inputs to settle.

For very long transducer cables with significant inductance, setting the INPUT COMPENSATION control bit will provide line compensation and improve stability. With line compensation enabled, the input bandwidth is limited typically to 50kHz.

3.14 Triggered Burst Sampling

3.14.1 Burst Control

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, a Burst Trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired. Sampling then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit Input Burst Block Size control register (Table 3.1). The number of samples acquired in a burst *for each active channe*l equals the value contained in this register. The total number of samples acquired equals this value *times* the number of active channels. If a BURST BLOCK SIZE of zero is selected, a trigger initiates a nonterminating burst that continues as long as bursting is enabled, the buffer is enabled, and a sample clock is present.

A trigger can be generated by (a) asserting the S/W BURST TRIGGER control bit in the BCR, or (b) by implementing the internal burst trigger timer (3.14.2), or (c) by injecting a positive pulse of 120 nanoseconds or greater width as the EXT SYNC INP input signal at the system I/O connector. Regardless of the source of the trigger, the S/W BURST TRIGGER bit in the BCR will always be HIGH during a triggered burst, and the trigger will appear also as a 120 nanosecond positive pulse at the EXT SYNC OUT output in the I/O connecter for synchronously triggering other boards. *Input triggers are ignored when S/W BURST TRIGGER is HIGH, of if the buffer is disabled (3.5.3.2).*

A software trigger can be applied at any time by setting the INPUT S/W TRIGGER control bit HIGH in the BCR. This bit clears automatically.

Note: If the ENABLE INPUT BURST control bit is HIGH in the BCR, an external SYNC input will be regarded as a burst trigger, and synchronization as described in Paragraph 3.6.5.2 will not occur. To burst-trigger multiple boards, synchronize the boards before asserting ENABLE INPUT BURST.

Note: Although External Sync I/O is active as a Burst Trigger I/O port when bursting is enabled, the SOFTWARE SYNC control bit in the BCR is ignored in this mode.

3.14.2 Internal Burst Timer

When the ENABLE TRIGGER TIMER control bit is HIGH in the BCR, the internal trigger timer generates a continuous series of burst triggers. The trigger rate is determined as:

TRIGGER RATE (Hz) = Fref / TRIGGER RATE DIVISOR,

where Fref is the master clock frequency in Hertz, and TRIGGER RATE DIVISOR is defined in the 24-Bit Trigger Rate Divisor register shown in Table 3.14.1. Fref has a standard value of 49.152MHz.

Table 3.14.2. Burst Trigger Timer Register

Offset: 0000 003Ch **Default: 0000 C000h**

BIT FIELD:	DESIGNATION	FUNCTION
D[23..00]	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D[31..24]	(Reserved)	---

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PCIe-24DSI12WRCIEPE contains twelve delta-sigma 24-Bit A/D converters and the supporting functions necessary for implementing IEPE transducers, as well as precision voltage acquisition. A PCI Express bus adapter (Figure 4.1) provides the interface between the controlling PCI Express bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

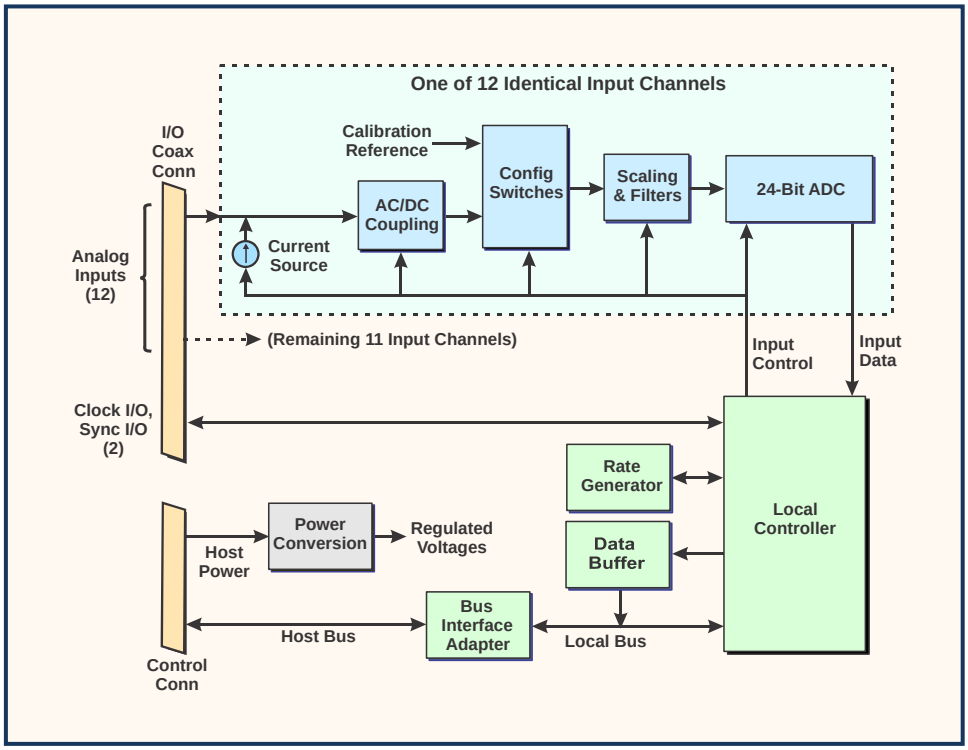

Figure 4.1. Functional Block Diagram

Input configuration switches allow the controller to select any of several signal sources as inputs to the ADC's. This feature is used to establish the internal connections necessary during autocalibration, and also permits verification from the PCI Express bus of the integrity of all analog input channels. All channels are calibrated against a single precision voltage reference. The offset and gain calibration of each input channel are adjusted with correction values that are determined during autocalibration.

4.2 Analog Inputs

Each input channel provides the excitation current and AC coupling required by IEPE transducers, and can also be software-configured with the current source disabled and with DC coupling enabled for precision voltage acquisition. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. During normal operation, the analog input signal passes through a scaling differential amplifier which controls the input range, and which suppresses any common mode voltage that might be present. During selftest and autocalibration operations, the input configuration switches can be used to replace the system input signal with either a precision zero (ground) or a positive full-scale reference voltage.

Each ADC implements a sharp-cutoff lowpass digital image filter that has a bandwidth slightly less than one-half the sampling frequency. A characteristic of this filter (and of most digital filters) is a loss of attenuation at multiples of the ADC clocking frequency. Consequently, 'images' of any out-of-band signal components present in the input signal can occur at these frequencies and can be aliased into the passband as interference. For this reason, each input signal passes through a lowpass 2nd-order Butterworth analog filter that is designed to suppress image components that might be present in the input signals.

The final conditioned and scaled input signal is digitized by each ADC into a 24-BIt serial data value that is deserialized into parallel format by the local controller. The controller then attaches a 4-bit channel tag to the data word, applies offset and gain correction factors, and finally transfers the corrected data to the input data buffer.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all input channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The offset error of each channel is determined first by selecting a zero input reference level and storing the values reported from all channels. A precision internal voltage reference then is used to determine the necessary gain correction which, like offset correction, is stored for use during normal acquisition

The internal voltage reference is adjusted to equal 99.000 percent of the selected input voltage range. This in-range value ensures that the ADC's will provide the nonsaturated, or in-range, responses that are necessary during the calibration adjustment process.

4.4 Sampling Clocks

An internal sample rate generator provides a frequency range of approximately 27-54 MHz, which is divided down by a software-specified integer to provide sample rates from 0.2-105 KSPS.

An external clock output can be assigned to replace the output of the internal rate generator, or can serve directly as the ADC clock. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive the external clock are *clock targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Control

Regulated supply voltages of +5 Volts, +6 Volts and ±14 Volts are required by the analog networks. Multiple DC/DC converters in the power section use +3.3V and +12V input power from the PCI Express bus to produce preregulated DC voltages. These preregulated voltages subsequently are postregulated with linear regulators to the required supply voltages. Linear regulators ensure that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

Local Addr [1]	Designation	Access Mode [2]	Default	Primary Function	Ref
00	**Board Control (BCR)**	R/W	0000 381Ch	Board Control Register (BCR)	3.2
04	**Rate Control-A**	R/W	0003 0032h	PLL reference oscillator control integer.	3.6.2
08	**Input Port Configuration**	R/W	0000 0000h	Specifies input parameters associated with the IEPE interface.	3.13
0C	**Clock-Source Assignments**	R/W	0000 0000h	ADC Clock source; Group disables.	3.6.1.2
10	**Rate Divisor**	R/W	0000 0005h	Sample rate divisor.	3.6.1.3
14	(Reserved)	R/W	0000 0000h	---	---
18	(Reserved)	RO	0000 0000h	---	---
1C	**Burst Block Size**	R/W	0000 0001h	Specifies the number of sample sets to be acquired in a triggered burst	3.14
20	**Buffer Control**	R/W	0003 FFFEh	Input buffer control and status	3.5.3
24	**Board Configuration**	RO	00XX XXXXh	Installed firmware and hardware options	3.10
28	**Buffer Size**	RO	000X XXXXh	Number of ADC values in the input buffer.	3.5.4
2C	Autocal Values [3]	R/W	---	---	---
30	**Input Data Buffer**	RO (DMA)	XXXX XXXXh	Input Data Buffer; Data and channel tag	3.5
34	**Auxiliary Sync I/O Control**	R/W	0000 0000h	Auxiliary external Clock and Sync control.	3.12
38	(Reserved)	R/W	0000 0000h	---	---
3C	**Burst Trigger Timer**	R/W	0000 C000h	Internal trigger timer rate divisor	3.14
40-7C	(Reserved)	---	---	---	---

[1] Offsets from the PCI base address for local addressing.

[2] R/W = Read/Write; RO = Read-Only.

[3] Maintenance register; Shown for reference only

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 381Ch**

Data Bit	Designation	Mode	Def	Function	Ref
D00	AIM0	R/W	0h	Analog input mode. Selects system inputs or selftest mode. Defaults to system inputs.	3.4
D01	AIM1				
D02	RANGE0	R/W	3h	Analog input range selection. Defaults to ±10V range.	3.4.2
D03	RANGE1				
D04	OFFSET BINARY	R/W	1	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	CLOCK INITIATOR	R/W	0	Selects INITIATOR or TARGET mode for external clock input/output signals. Defaults Low to Target mode to prevent line conflicts at initialization.	3.6.5
D06	SOFTWARE SYNC [1]	R/W	0	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.5.3.2, 3.6.4
D07	AUTOCAL [1]	R/W	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion.	3.7
D08	INTERRUPT A0	R/W	0h	Interrupt event selection. Default is zero.	3.8
D09	INTERRUPT A1	R/W			
D10	INTERRUPT A2	R/W			
D11	INTERRUPT REQUEST FLAG	R/W	1	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	AUTOCAL PASS	RO	1	Set HIGH at reset or autocal initialization. Cleared LOW if autocalibration terminates unsuccessfully.	3.7
D13	CHANNELS READY	RO	1	LOW during any change in channel parameters. Asserted HIGH when inputs are ready to acquire data.	3.4.3
D14	BUFFER THRESHOLD FLAG	RO	0	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	INITIALIZE [1]	R/W	0	Initializes the board when asserted. Sets all defaults.	3.3.2
D16	ENABLE TRIGGER TIMER	R/W	0	Enables the internal burst trigger timer.	3.14
D17	CLEAR BUFFER ON SYNC	R/W	0	Changes the context of the SOFTWARE SYNC to CLEAR BUFFER.	3.5.3.2
D18	RATE GEN EXT CLOCK OUT (Initiator Mode only)	R/W	0	When HIGH: Selects the internal rate generator as the external clock output source. When LOW: Selects the Group-00 sample clock.	3.6.5.1
D19	HIGH SPEED ADC MODE	R/W	0	Selects the ADC High-Speed mode when HIGH, or the High-Resolution Mode when LOW.	3.6.1.3
D20	SYNC INITIATOR	R/W	0	Selects INITIATOR or TARGET mode for external Sync input/output signals. Defaults Low to Target mode to prevent line conflicts at initialization.	3.6.5
D21	ENABLE INPUT BURST	R/W	0	Selects triggered-burst acquisition when HIGH.	3.14
D22	S/W BURST TRIGGER	R/W	0	Initiates a triggered burst when asserted. Forced HIGH during any triggered burst.	3.14
D23	EXTERNAL SYNC INPUT	R/W	0	Configures the Sync I/O connecter as the Sync source. 'Requires the SYNC INITIATOR control bit to be HIGH.	3.6.5.2
D24-31	(Reserved)	RO	0h	---	---

[1] Clears automatically.

Table 3.3.1. Configuration and Initialization Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	20 ms
Settling delay for AC-coupled inputs	**5 seconds**

Table 3.4. Analog Input Function Selection

AIM[1..0]	Function or Mode
0	Differential analog input mode.
1	(Reserved).
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.

Table 3.4.2. Analog Input Range Selection

RANGE[1..0]	Standard Input Range
0	±10mV
1	±100mV
2	±1.0V
3	±10V

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

Selected Data Width	Reserved (Zero)	Channel Tag	Zero-Pad	Channel Data Value
16 Bits	D[31..28]	D[27..24]	D[23..16]	D[15..0]
18 Bits	D[31..28]	D[27..24]	D[23..18]	D[17..0]
20 Bits	D[31..28]	D[27..24]	D[23..20]	D[19..0]
24 Bits	D[31..28]	D[27..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh**

Bit Field	Mode	Designation	Def	Function
D[18..00]	R/W	BUFFER THRESHOLD	0003 FFFEh	Buffer Flag Threshold
D[19]	R/W	ENABLE BUFFER INPUT	0	Enables ADC inputs to the buffer.
D[20]	R/W	CLEAR BUFFER [1]	0	Clears (empties) the buffer. Asserted HIGH while the buffer is cleared, either locally or externally.
D[22..21]	R/W	DATA WIDTH	0	Controls the width of the buffer data field: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23]	R/W	DISABLE CHANNEL TAG	0	Replaces the channel tag with a zero-field.
D[24]	R/W	BUFFER OVERFLOW [2]	0	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW [2]	0	Reports buffer underflow (Read on empty)
D[31..26]	RO	(Reserved)	0h	---

[1] Clears automatically. [2] Cleared by writing LOW, or by Initialization.

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	12-CHAN BOARD	8-CHAN BOARD	4-CHAN BOARD
0	Channels 00-05	00-03	00, 01
1	Channels 06-11	04-07	02, 03

Table 3.6.1.2-1. Clock-Source Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 CLOCK SOURCE	0
D[07..04]	GROUP 1 CLOCK SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Clock-Source Assignment Codes

ASSIGNMENT CODE	GROUP 0 ASSIGNMENT	GROUP 1 ASSIGNMENT
0	Internal Rate Generator *	No effect. (Same as Group-0)
1-3	(Reserved)	
4	External Sample Clock (as rate generator input)	
5	Direct External Sample Clock (routed directly to ADC)	
6	**Invalid**	**Disabled**
7-15	(Reserved)	(Reserved)

* Applies to both channel groups. Disabling Group-0 disables both groups.

Table 3.6.1.3-1. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0005h**

BIT FIELD:	DESIGNATION	FUNCTION
D[08..00]	RATE DIVISOR (**Ndiv)**	Prescales the rate generator input frequency.
D[31..9]	(Reserved)	---

Table 3.6.1.3-2. Sample-Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz nominal range
Rate Divisor	**Ndiv**	1-300
Sample Rate Range	**High-Speed Mode**	0.4 - 105 KSPS
	High-Resolution Mode	0.2 - 52.5 KSPS

Table 3.6.2-1. Rate Generator Control Register

Offset: 0004h **Default: 0003 0032h**

BIT FIELD	MODE	DESIGNATION	FUNCTION *
D[11..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 25-300.
D[23..12]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 25-300.
D[31..24]	R/W	(Reserved)	---

* For maximum phase stability, select the lowest possible values for Nvco and Nref.

Table 3.6.2-2. Rate-Generator Control Parameters

PARAMETER	NOTATION	NOMINAL RANGE
VCO Frequency Range	**Fgen**	27 - 54 MHz
Reference Frequency	**Fref**	Standard value = 49.152 MHz
VCO Factor	**Nvco**	25-300; Optimum at 30-200.
Reference Factor	**Nref**	25-300; Optimum at 30-200.
Nvco/Nref Factor Ratio	**Nvco/Nref**	0.55-1.10

Table 3.6.2-3. Sample Rate Examples

Sample Rate (KSPS)	Nvco	Nref	Fgen (Mhz)	Ndiv	MODE (BCR)
0.200	30	30	49.1520	240	High-Resolution (Fsamp = Fgen/1024Ndiv)
1.000	30	30	49.1520	48	
10.000	50	48	51.2000	5	
20.000	30	36	40.9600	2	
50.000	50	48	51.2000	2	High-Speed (Fsamp = Fgen/512Ndiv)
100.000	50	48	51.2000	1	
102.400	32	30	52.4288	1	
105.000	35	32	53.7600	1	

Fref = 49.152MHz. All values shown in decimal format.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	Autocal completed
2	Channels Ready; LOW-to-HIGH transition
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	Triggered Burst Completed
6	(Reserved)
7	(Reserved)

Table 3.10.1. Board Configuration Register

Offset: 0000 0024h **Default: 0000 XXXXh**

BIT FIELD	DESCRIPTION
D00-D11	Firmware Revision
D12-D15	(Reserved status flags).
D16-D17	Number of input channels: 0 => 12 Channels 1 => 8 Channels 2 => 4 Channels 3 => (Reserved)
D18-D19	Image Filter Frequency: 0 => 150kHz 1 => No filter. 2-3 => (Reserved)
D20-D21	AC Cutoff Frequency: 0 => 0.5 Hz 1 => 2 Hz 2-3 => (Reserved)
D22-D23	Excitation Current:: 0 => 4mA 1-3 => (Reserved)
D24-D31	(Reserved; all-zero)

Table 3.12.1. Auxiliary Sync I/O Control

Offset: 0000 0034h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-01	R/W	AUX CLOCK Control Mode	0	AUX CLOCK I/O Control Mode: 0 => Inactive 1 => Active Input 2, 3 => Active Output
D02-03	R/W	AUX SYNC Control Mode	0	AUX SYNC I/O Control Mode 0 => Inactive 1 => Active Input 2, 3 => Active Output
D04-31	RO	(Reserved)	0	Read-back as all-zero.

Table 3.13. Input Port Configuration Register

Offset: 0000 0008h **Default: 0000 0000h**

Control Bit:	Designation	Def	Function	Normal IEPE State
D[00]	DC COUPLING	0	Configures the inputs for AC coupling when LOW, or for DC coupling when High.	Low
D[01]	EXCITATION CURRENT	0	Provides excitation current to all inputs when HIGH. Disables the current sources when LOW.	High
D[02]	INPUT COMPENSATION	0	Inserts line compensation to stabilize very long transducer cables. Limits input bandwidth to approximately 50kHz.	Low
D[03]	Aux Current *	0	Diagnostic; Injects a coarse constant current to all inputs when High, or has no effect when Low.	Low
D[31..04]	(Reserved)	---	---	---

* Diagnostic control bit for factory testing. Leave in the LOW state.

Table 3.14.2. Burst Trigger Timer Register

Offset: 0000 003Ch **Default: 0000 C000h**

BIT FIELD:	DESIGNATION	FUNCTION
D[23..00]	TRIGGER RATE DIVISOR	Rate divisor for internally timed triggered bursts.
D[31..24]	(Reserved)	---

APPENDIX B

Migration From PMC66-24DSI16WRC

Appendix B

Migration From PMC66-24DSI12WRC

Operation of the PCIe-24DSI12WRCIEPE is similar to that of the PMC66-24DSI16WRC. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements or changes.

B.1. Comparison of Features

Table B.1 summarizes principal PMC66-24DSI16WRC and PCIe-24DSI12WRCIEPE features.

Table B.1. PCI-24DSI32, PCIe-24DSI12WRCIEPE Features Comparison

Feature	PMC66-24DSI16WRC	PCIe-24DSI12WRCIEPE
Number of Input Channels	**16**	**12**
Control Interface	**PCI 2.3; D32; 33MHz/66MHz**	**PCI Express, Single lane**
Transducer Excitation	**None**	**Constant Current**
Input Coupling	**DC**	**DC or AC, software-selected**
Form Factor	**Single-width PMC**	**PCI Express Short card**
Local Clock	**40 MHz**	**49.152 MHz**
External clock and sync I/O	**LVDS, TTL Front-panel & internal**	**TTL, Front-panel & Internal**
Native Resolution	24 Bits	
Sample Rate Range	0.2 KSPS to 105 KSPS	
Triggered-Burst Sampling	Yes	
Autocalibration	On-demand	

B.2. Migration Issues

Section 2.0. Installation and Maintenance:

Front-panel system I/O connections are now MMCX coaxial connectors.
Constant current excitation has been added.

Table 3.1. Control and Data Registers

The Digital I/O Port register has been replaced with the Input Port Configuration register.
The Master Clock Adjust register has been deleted.
Rate Control-A and Burst Trigger Timer register defaults have been modified.

Table 3.2. Board Control Register

D05 is redefined as Clock Initiator, D20 as Sync Initiator, and D23 as External Sync Input. See also Paragraph 3.6.5 below.

Section 3.3.2: Initialization:

Initialization duration has been increased to **5 seconds**, to allow the AC coupled inputs to settle.

NOTE: A minimum settling delay of 5 seconds should be provided after selecting AC coupling or enabling the excitation current, in order to allow the AC coupled inputs to settle.

Section 3.6.1: Sample Rate Control

The reference frequency Fref has changed from 40.000MHz to 49.152 MHz.

Section 3.6.5: Multiboard Operation

The Clock and Sync I/O ports have been modified to permit independent assignment as inputs or outputs.

Section 3.13: Controlling the IEPE Interface

The IEPE interface replaces the adjustable master clock frequency function.

Section 3.15: Digital I/O Port

This function has been deleted.

APPENDIX C

TYPICAL SYNC AND TRIGGER CONFIGURATIONS

APPENDIX C
Typical SYNC AND TRIGGER CONFIGURATIONS

This section provides tabulations pertaining to typical applications involving the Synchronization, Burst Triggering and Sample Clocking functions of this product, and is not a definitive list of all possible control combinations.

Table C.1: PCIe-24DSI12WRCIEPE: Typical Sync Configurations

(Paragraphs 3.6.4, 3.6.5, 3.12)

Control Bits							I/O Pins		
S/W SYNC (Pulse)	SYNC INITIATOR	EXTERNAL SYNC INPUT	AUX SYNC Control Mode	ENABLE INPUT BURST	S/W TRIGGER (Pulse)R	ENABLE TRIGGER TIMER	SYNC (Fr Pnl)	AUX SYNC	Local ADC Sync Source
1	0	0	0	0	0	0	0	0	Single (BCR)
1	1	0	0		0	0	Sync Out	0	Single (BCR)
1	0	0	2 (Out)		0	0	0	Sync Out	Single (BCR)
1	1	0	2 (Out)		0	0	Sync Out	Sync Out	Single (BCR)
0	0	1	0		0	0	Sync In	0	SYNC Port Input Rate
0	0	1	1 (In)		0	0	0	Sync In	AUX Port Input Rate

Table C.2: PCIe-24DSI12WRCIEPE: Typical Burst Triggering Configurations

(Paragraphs 3.6.4, 3.6.5, 3.12, 3.14)

Control Bits							I/O Pins		
S/W SYNC (Pulse)	SYNC INITIATOR	EXTERNAL SYNC INPUT	AUX SYNC Control Mode	ENABLE INPUT BURST	S/W TRIGGER (Pulse)	ENABLE TRIGGER TIMER	SYNC (Fr Pnl)	AUX SYNC	Local Triggering Source
0	0	0	0	1	1	0	0	0	Single (BCR)
	1	0	0		1	0	Trig Out	0	Single (BCR)
	0	0	2 (Out)		1	0	0	Trig Out	Single (BCR)
	1	0	2 (Out)		1	0	Trig Out	Trig Out	Single (BCR)
	0	1	2 (Out)		0	0	Trig In	Trig Out at Trig In Rate	SYNC Port Input Rate
	0	1	0		0	0	Trig In	0	SYNC Port Input Rate
	0	1	1 (In)		0	0	0	Trig In	AUX Port Input Rate
	0	0	0		0	1	0	0	Internal Trigger Timer
	1	0	0		0	1	Trig Out at Internal rate	0	Internal Trigger Timer
	0	0	2 (Out)		0	1	0	Trig Out at Internal rate	Internal Trigger Timer
	1	0	2 (Out)		0	1	Trig Out at Internal rate	Trig Out at Internal rate	Internal Trigger Timer

Table C.3: PCIe-24DSI12WRCIEPE Sample Clock Configurations

(Paragraphs 3.6.1, 3.6.5)

Control Bits			I/O Pins		
CLOCK INITIATOR	**Group-0 Clock Source**	**AUX CLOCK Control Mode**	CLOCK (Fr Pnl)	AUX CLOCK	**Local Response**
0	**0**	**0**	**0**	**0**	**ADC Clock Divided from Internal Rate-A**
1	**0**	**0**	**Rate-A Out**	**0**	
0	**0**	**2 (Out)**	**0**	**Rate-A Out**	
1	**0**	**2 (Out)**	**Rate-A Out**	**Rate-A Out**	
0	**4**	**0**	**Ext Rate In**	**0**	**ADC Clock Divided from Ext Rate In**
0	**4**	**1 (In)**	**0**	**Ext Rate In**	
0	**5**	**0**	**Ext Rate In**	**0**	**ADC's Clock Directly from Ext Rate In**
0	**5**	**1 (In)**	**0**	**Ext Rate In**	

Revision History:

06-21-2014: Origination as preliminary draft.

07-07-2014: 3.6.1.2, 3.7: Added note pertaining to autocalibration.
Table 3.6.1.2-2: Revised Group-0 Code=6 response.

09-25-2014: Figure 3.6.1.1: Updated illustration.
Paragraph 3.6.1.3: Added note pertaining to Figure 3.6.1.1.
Paragraphs 3.4.1, 3.7: Added description of the effect of AC coupling on selftest and autocal.
Paragraph 3.13: Added note pertaining to DC coupling and excitation current.

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