General Standards Corporation

High Performance Bus Interface Solutions

Rev: 010509

PC104P-24DSI6LN

24-BIT, SIX-CHANNEL, LOW-NOISE, 200 KSPS DELTA-SIGMA ANALOG INPUT PC104-*Plus* MODULE

REFERENCE MANUAL

--- PRELIMINARY ---

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1.0

INTRODUCTION

1.1 General Description

The PC104P-24DSI6LN module provides 24-bit low-noise analog input capability for the PC104-*Plus* bus at sample rates up to 200 KSPS per channel. In addition to providing six analog input channels, this product supports multiboard clocking and synchronization. The module is functionally and mechanically compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with minimal air cooling. Specific details pertaining to performance are contained in the PMC-24DSI6LN product specification.

This product is designed for minimum off-line maintenance. All system input and output connections are made through a 68-Pin dual-ribbon cable connector. Figure 1.1 represents the physical configuration of the module.

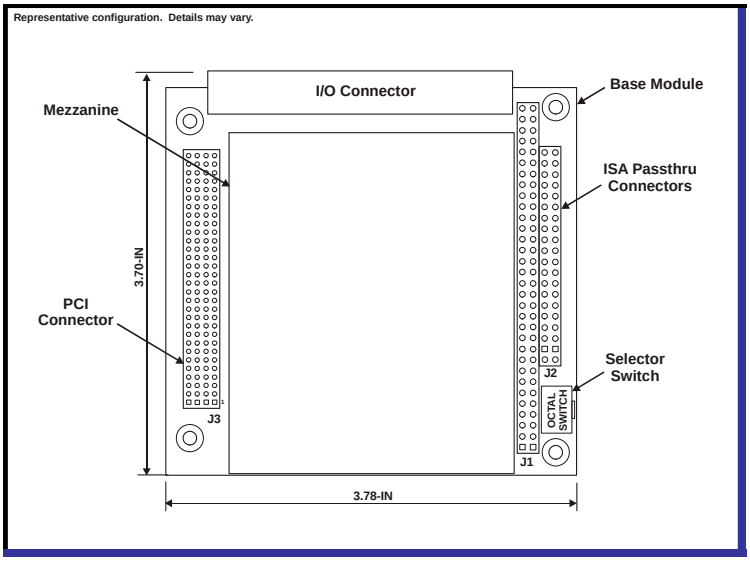

Figure 1.1. Physical Configuration

Although the PC104P-24DSI6LN is functionally equivalent to the PMC-24DSI6LN, overall dimensions for the PC104-Plus form factor differ from PMC dimensions as:

Height: 23.3 mm (0.92 in)
Width: 94.0 mm (3.78 in)
Depth: 95.9 mm (3.70 in).

1.2 Functional Overview

A PCI interface adapter provides the interface between the controlling PCI bus and the internal local controller through a 32-bit local bus (Figure 1.2). Inputs are organized into two channel groups, either of which can be designated as either active or inactive. Each even-odd channel pair also contains a dual delta-sigma A/D converter (ADC) that provides two separate but synchronized conversion channels.

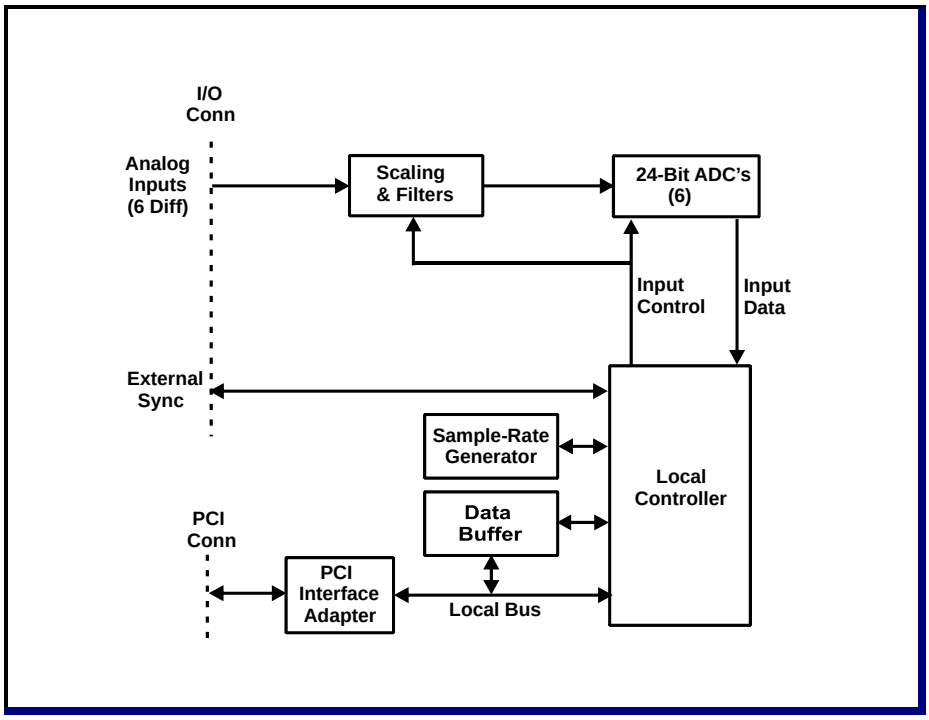

Figure 1.2. Functional Organization

An internal sample-rate clock generator is adjustable from 25.6 MHz to 51.2 MHz, and is divided down within the local controller to provide sample rates from 2.0 KSPS to 200 KSPS. Input bandwidth extends down to DC. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample FIFO data buffer.

Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals. Hardware sync and clock input/output signals permit multiple boards to be connected together for phase-locked operation from a common clock.

SECTION 2.0
INSTALLATION AND MAINTENANCE

2.1 Board Configuration

With the single exception of a rotary selection switch, this product has no field-alterable configuration features, and is completely configured at the factory.

The selection switch (Figure 1.1-1) allows the board to be configured as one of four unique devices in a PC104-*Plus* stack. Positions 0 through 3 provide four unique bus-access configurations, while positions 4 through 7 are unused. The exact relationship or mapping of switch positions and slot-specific signals may vary among manufacturers of PC104-*Plus* motherboards.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the module should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the module from the conductive shipping envelope, ensure that the work surface, the installer and the host equipment have been properly discharged to ground.

After removing the module from the antistatic shipping container, align the PCI and ISA connector pins with the corresponding receptacles on either the host board if the module is the first module in the stack, or on the preceding module in the stack. Press the module carefully but firmly downward into position, and verify that the PCI and ISA connectors have mated completely and that the spacers are seated against the host or preceding module.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board.

The system I/O connector is designed to mate with a 68-pin dual-ribbon connector, equivalent to AMP #749621-7. This insulation displacement (IDC) cable connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2.2 and in Figure 2.2.2.

Table 2.2.2. System Connector Pin Assignments

ROW-A		ROW-B	
PIN	FUNCTION	PIN	FUNCTION
1	INPUT RETURN	1	INPUT RETURN
2	INPUT RETURN	2	INPUT RETURN
3	**INP CHAN 00 LO**	3	INPUT RETURN
4	**INP CHAN 00 HI**	4	INPUT RETURN
5	INPUT RETURN	5	INPUT RETURN
6	INPUT RETURN	6	INPUT RETURN
7	**INP CHAN 01 LO**	7	INPUT RETURN
8	**INP CHAN 01 HI**	8	INPUT RETURN
9	INPUT RETURN	9	INPUT RETURN
10	INPUT RETURN	10	INPUT RETURN
11	**INP CHAN 02 LO**	11	INPUT RETURN
12	**INP CHAN 02 HI**	12	INPUT RETURN
13	INPUT RETURN	13	INPUT RETURN
14	INPUT RETURN	14	INPUT RETURN
15	**INP CHAN 03 LO**	15	INPUT RETURN
16	**INP CHAN 03 HI**	16	INPUT RETURN
17	INPUT RETURN	17	INPUT RETURN
18	INPUT RETURN	18	INPUT RETURN
19	**INP CHAN 04 LO**	19	INPUT RETURN
20	**INP CHAN 04 HI**	20	INPUT RETURN
21	INPUT RETURN	21	INPUT RETURN
22	INPUT RETURN	22	INPUT RETURN
23	**INP CHAN 05 LO**	23	INPUT RETURN
24	**INP CHAN 05 HI**	24	INPUT RETURN
25	INPUT RETURN	25	INPUT RETURN
26	INPUT RETURN	26	INPUT RETURN
27	DIGITAL RETURN	27	DIGITAL RETURN
28	DIGITAL RETURN	28	DIGITAL RETURN
29	**EXT CLK INP LO ****	29	**EXT CLK OUT LO**
30	**EXT CLK INP HI ***	30	**EXT CLK OUT HI ***
31	DIGITAL RETURN	31	DIGITAL RETURN
32	DIGITAL RETURN	32	DIGITAL RETURN
33	**EXT SYNC INP LO ****	33	**EXT SYNC OUT LO**
34	**EXT SYNC INP HI ***	34	**EXT SYNC OUT HI ***

* TTL signal levels when TTL sync I/O is selected.
** 'LO' digital inputs must be open (unconnected) in TTL mode.

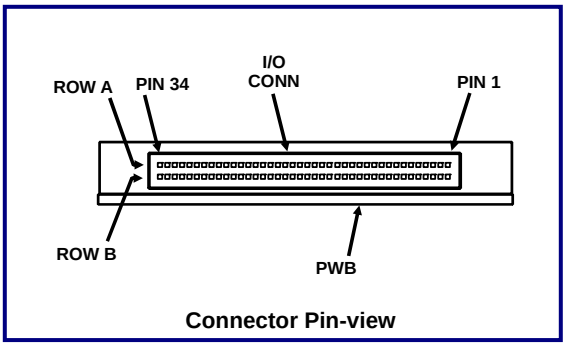

Figure 2.2.2. System I/O Connector

System Cable Mating Connector:
68-pin 0.050" Subminiature connector: with metal shield: AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**
Amp # 787170-7

2.3 Analog Input Configuration

The analog inputs are configured as six differential input pairs. Differential operation provides the highest noise immunity, and is recommended for the majority of applications. Pull-down resistors are provided on all analog inputs. Although the input configuration is differential, single-ended signal sources can be accommodated as described in Paragraph 2.3.2.

2.3.1 Differential Inputs

Differential operation is essential when the input source returns are at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2.3.1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return should be connected to system ground (remote common) as closely as possible to the input sources. The average HI/LO signal level relative to the input return is the common mode voltage **Vcm** which, for optimum performance, must not exceed the maximum value indicated in the product specification.

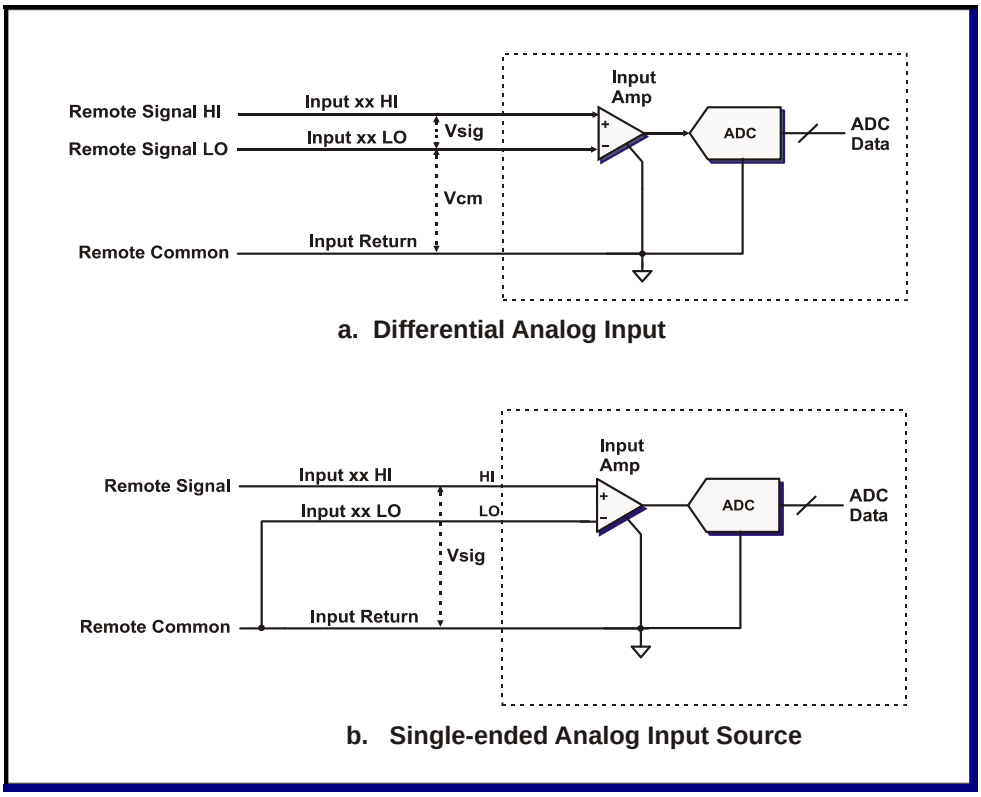

Figure 2.3.1. Input Configurations

2.3.2 Single-Ended Input Sources

Single-ended signal sources can be accommodated as shown in Figure 2.3.1b, with the signal line connected to INP CHAN XX HI, and the associated INP CHAN XX LO input connected to INPUT RETURN at the source. The single-ended operating connection provides suitable performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

CAUTION: If a significant potential difference exists between the remote signal return and INPUT RETURN, a low impedance between the two returns can cause excessive current to flow, which in turn can cause erroneous measurements or possible damage to the board. Return-current should be controlled to less than a few milliamps for best performance, and to less than 100 milliamps to avoid damage.

2.4 Multiboard Clocking and Synchronization

Analog input converters on multiple boards can be:

a. Clocked from a single clock source (Multiboard clocking), and/or:

b. Synchronized to a common time reference (Multiboard synchronization).

Clocking multiple converters from a single source prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronizing* the converters on multiple boards causes the converters to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

2.4.1 Interboard Connections

Figure 2.4.1 illustrates how multiple PC104P-24DSI6LN boards can be daisy-chained together in an initiator-target sequence to provide common clocking between boards. The CLOCK OUTPUT HI/LO lines from an initiator are connected to the CLOCK INPUT HI/LO lines on a target board, and the SYNC output and input pairs are connected similarly. Each target board can serve as an initiator for another target board, and multiple boards can be daisy-chained together for synchronous operation.

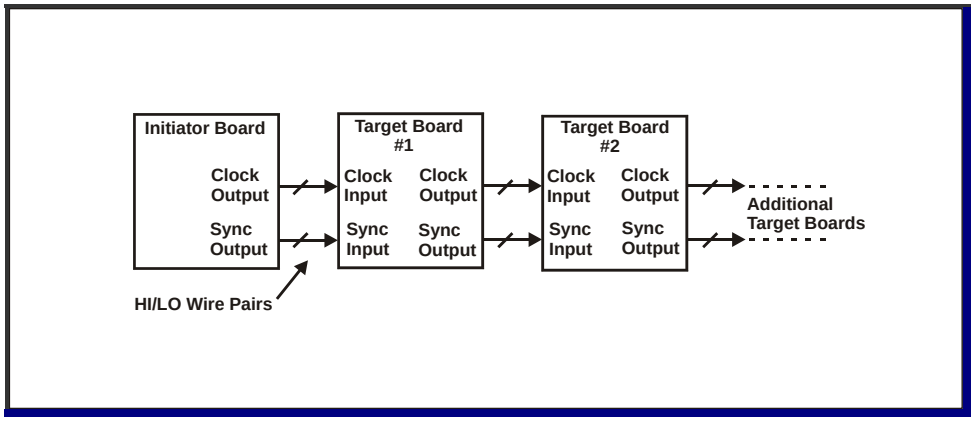

Figure 2.4.1. Multiboard Clock/Sync Connections

By using an external clock and sync distribution module, multiple boards can be interconnected in a 'star' configuration to eliminate the clock and sync propagation delay introduced by each board in a daisy chain configuration.

The clock output signal is generated internally on an initiator board, or is a duplicate of the clock input signal on a target board. Similarly, the sync output is the software-generated sync signal on an initiator board, or a duplicate of the sync input signal on a target board.

Note: External clock and sync inputs can be provided from external sources other than an initiator board, and can software-configured for either single-ended TTL or differential LVDS logic levels. As a general rule, LVDS levels should be used in applications requiring I/O cable lengths that exceed 20-30 centimeters (10 inches).

In the TTL configuration, clock and sync inputs and outputs are connected through the "HI" I/O pins. LO inputs must be left open or disconnected, and the LO outputs are inactive. TTL signals are referenced to DIGITAL RETURN.

Because each board provides active clock and sync outputs for the next board in the chain, the number of boards in the chain is limited only if the propagation delay of approximately 10 nanoseconds introduced by each board becomes significant through multiple boards. For LVDS clock and sync I/O configurations, cable-length between boards should not exceed one meter for general-purpose ribbon cable, while high-quality 100-Ohm cable can extend the length to 10 meters or more.

Application software controls the designation of each board as an initiator or a target, and also selects the channels on each board that will respond to the external clock. Although only software-designated channels respond to the external clock, all channels on all target boards respond to the external sync input.

For additional synchronization options, refer to Section 3.12.

2.4.2 Multiboard Synchronization

Boards that are interconnected for multiboard synchronization initiate internal *synchronization sequences* each time a sync pulse is generated by the initiator board. The sync I/O can also be used to reset (clear) the data buffers on target boards.

2.5 Maintenance

This product requires no scheduled hardware maintenance.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PC104P-24DSI6LN board is compatible with the PCI Local Bus specification Revision 2.3, and the PCI interface is controlled by a PLX™ PCI-9080 PCI adapter. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space.

After initialization, communication between the PCI bus and the board takes place through the control and data registers shown in Table 3.1. All data transfers are long-word D32. Reserved bits in each register are ignored during write operations, and are forced LOW during read operations. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written as LOW.

Table 3.1. Control and Data Registers

LOCAL ADDR [1]	ACCESS MODE [2]	REGISTER	DEFAULT	DESCRIPTION
00	R/W	**Board Control (BCR)**	0000 2830h [3]	Board Control Register (BCR)
04	R/W	**Rate Control A**	0040 0032h	Rate Generator-A control
08	R/W	**Rate Control B**	0040 0032h	Rate Generator-B control.
0C	R/W	**Rate Assignments**	0000 0000h	Channel-group rate generator assignment
10	R/W	**Rate Divisors**	0000 0505h	Channel-group sample rate divisors.
14	R/W	(Reserved)	0000 0000h	---
18	RO	**PLL Reference Freq**	XXXX XXXXh	PLL reference frequency indicator.
1C	R/W	**GPS Synchronization**	0000 2000h	Controls sample rate GPS synchronization.
20	R/W	**Buffer Control**	0003 FFFEh [4]	Input buffer control and status
24	RO	**Board Configuration**	00XX XXXXh	Installed firmware and hardware options
28	RO	**Buffer Size**	0XXX XXXXh	Number of ADC values in the input buffer.
2C	RO	(Reserved)	---	---
30	RO (DMA)	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag
34-7C	--	(Reserved)	---	---

[1] Offsets from the "PCI base address for local addressing".
[2] R/W = Read/Write; RO = Read-Only.
[3] Changes to 0000 6830h when the input buffer fills.
[4] Changes to 0103 FFFEh when the buffer fills.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including analog input mode and analog input range, and consists of 32 control bits and status flags. Table 3.2 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 2830h ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION	SECTION
D00-03	R/W	(Reserved)	---	---
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults to Initiator mode.	3.6.3
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.3.2
D07	R/W	(Reserved)	---	---
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.	3.8.1
D09	R/W	INTERRUPT A1		
D10	R/W	INTERRUPT A2		
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	RO	(Reserved)	---	---
D13	RO	CHANNELS READY	LOW during any change in channel parameters. Asserted HIGH when ADC clocks are stabilized.	3.4.3
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	R/W	*INITIALIZE	Initializes the board when asserted HIGH.	3.3.2
D16	R/W	ASYNCHRONOUS SCAN	***Disables*** synchronous sampling mode when ***HIGH***.	3.10
D17	R/W	CLEAR BUFFER ON SYNC	Changes the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.	3.5.3.2
D18	R/W	RATE-A EXT CLOCK OUT (Initiator Mode only)	When HIGH: Selects the Rate-A generator as the external clock output source. When LOW: Selects the Group-00 sample clock as the output. (If Group-00 external clocking is selected, the output is driven by the Rate-A generator and the Group-00 divisor).	3.6.3.1
D19	R/W	(Reserved)	---	---
D20	R/W	TTL EXTERNAL SYNC I/O	Selects TTL external sync I/O configuration.	2.4.1, 3.6.3
D21	R/W	(Reserved)	---	---
D22	R/W	AC INPUT RESPONSE	Selects AC input coupling for all ADC's when HIGH; DC coupling when LOW.	3.6.4
D23	R/W	ADC RATE OUT	When this bit is HIGH, a positive pulse is generated at the EXT CLK OUT pin(s) in the I/O connector each time an ADC sample is acquired.	3.6.3.3
D24-31	RO	(Reserved)	---	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.
** Changes to 0000 7830h when the input buffer fills.

3.3 Configuration and Initialization

3.3.1 Configuration

Configuration is initiated by a PCI bus RESET, and should be required only once after the initial application of power. During board configuration, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	5 seconds

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted.

3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization has a maximum duration of 5 seconds, and produces the following conditions:

- The Initiator mode is selected, External clock output is Channel-00 sample clock,
- Synchronous Scanning is selected,
- The width of the buffer data field is adjusted to 16 bits,
- Rate generator(s) are adjusted to 25.6 MHz,
- Rate divisor(s) are preset to 5,
- Sample rate is 10 KSPS for all channels; i.e.: 25.6MHz / (512 *5).
- Both channel groups are controlled by rate generator A.
- The analog input buffer is reset to empty; buffer threshold equals 0003 FFFEh
- All control registers are initialized; all defaults are invoked
- The local interrupt request is asserted as an initialization-completed event.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Configuration

The analog inputs are configured as six differential HI/LO signal pairs. The fullscale input voltage range is determined by an ordering option as either ±10V, ±5V or ±2.5V.

3.4.1 Settling Delays and the Channels Ready Flag

When a critical parameter such as input mode or sample rate is changed, a settling transition occurs during which input measurements are unpredictable. A settling delay is inserted automatically when any or all of these parameters are changed, and the CHANNELS READY status flag in the BCR goes LOW during the delay. A LOW-to-HIGH transition of this flag is selectable as an interrupt request "channels ready" event (Section 3.8.1). The CHANNELS READY flag goes low during the following operations for the approximate intervals indicated:

5 Seconds:	Board initialization (3.3),
1 us:	Buffer reset, if not in synchronous-scanning mode (3.5.3.2),
10 us-5 ms:	Buffer reset, if in synchronous-scanning mode (3.5.3.2),
500 ms:	Sample rate change ; i.e.: Nrate, Ndiv, Rate assignments (3.6).
1-500 ms:	ADC synchronization (3.6.2 and 3.10),
1-500 ms:	Synchronous-scan initiation (3.10),

3.5 Input Data Buffer

3.5.1 General Characteristics

Analog input samples accumulate in the analog input data FIFO data buffer, which has a capacity of 256K data values. Data accumulates in the buffer until extracted by the PCI bus from a single register location, indicated as INPUT DATA BUFFER in Table 3.1. Reading an empty buffer returns an indeterminate value.

3.5.2 Data Organization

Each value in the data buffer consists of a 5-bit channel tag field, a zero-pad field, and a data field, as shown in Table 3.5.2. The width of the right-justified data field is adjustable from 16 bits to 24 bits by the buffer control register (Table 3.5.3), and the width of the zero-pad field is adjusted accordingly. The zero-pad field becomes a sign-extension field if two's complement data coding is selected.

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

SELECTED DATA WIDTH	RESERVED (Zero)	CHANNEL TAG	ZERO-PAD	CHANNEL DATA VALUE
16 Bits	D[31..29]	D[28..24]	D[23..16]	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

3.5.2.1 Channel Tags

If the input channels are not scan-synchronized (Paragraph 3.10), the order in which channel data accumulates in the buffer is not generally predictable. Therefore, a channel tag that identifies each input channel is attached to associated data values in the buffer.

3.5.2.2 Input Data Format

Input data values can be represented either in offset binary format by asserting the OFFSET BINARY control bit HIGH (default state) in the BCR, or in two's complement format by clearing the control bit LOW. Both coding conventions are illustrated for 16-Bit data in Table 3.5.2.2.

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	**OFFSET BINARY**	**TWO'S COMPLEMENT**
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Positive Full Scale is a positive level that equals the selected input voltage range for the board (e.g.: +5.000 Volts for the ±5V range). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total input voltage range. For 16-Bit data, one LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V range).

3.5.3 Buffer Control Register

The buffer control register (Table 3.5.3) contains the threshold value for the buffer status flag, and also provides control bits for clearing the buffer and for disabling the buffer input.

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold
D[18]	R/W	DISABLE BUFFER INPUT	Disables inputs to the data buffer.
D[19]	R/W	CLEAR BUFFER **	Clears (empties) the buffer
D[21..20]	R/W	DATA WIDTH	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23..22]	RO	(Reserved)	---
D[24]	R/W	BUFFER OVERFLOW ***	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW ***	Reports buffer underflow (Read on empty)
D[31..26]	RO	(Reserved)	

* Changes to 0103 FFFEh when the buffer fills. ** Clears automatically. *** Clear by writing LOW, or by reset.

NOTE: Since delta-sigma ADC's perform conversions continuously, the initiation and termination of acquisition sequences is controlled by the buffer's 'Clear' and 'Disable' controls.

3.5.3.1 Status Flag and Threshold

The amount of data contained in the input buffer can be used to control the BUFFER THRESHOLD FLAG status bit in the BCR, which can be selected also as an interrupt request event. The interrupt request event can be selected to occur on either the rising or falling edge of the flag (Table 3.8.1).

The threshold flag is asserted HIGH when the number of samples in the buffer ***exceeds*** the BUFFER THRESHOLD value in the buffer control register. A buffer-empty event is produced when the threshold value is adjusted to equal 0000 0000h and the threshold flag undergoes a HIGH-to-LOW transition.

3.5.3.2 Buffer Clearing and Disabling

Asserting the CLEAR BUFFER control bit in the buffer control register resets (empties) the buffer, and holds the buffer in reset for approximately 10 microseconds to allow the internal data pipeline to empty. This bit clears automatically.

Asserting the DISABLE BUFFER INPUT control bit disables inputs to the buffer from the ADC input channels, and halts the accumulation of further input data. Input data already present in the buffer when this bit is asserted remains in the buffer.

Note: The buffer also can be cleared by writing a "one" to the SOFTWARE SYNC control bit in the BCR when the CLEAR BUFFER ON SYNC control bit is HIGH. See "Global Buffer Clear" in Section 3.10.

3.5.4 Buffer Size Register

This read-only register contains the number of analog input values currently stored in the input data buffer.

3.5.5 Buffer Underflow and Overflow Flags

BUFFER OVERFLOW and BUFFER UNDERFLOW status bits in the buffer control register report overflow (write on full) or underflow (read on empty) events. Once set, these status bits remain HIGH until cleared by writing LOW directly, or by a board reset.

3.6 Input Sampling Control

The local controller establishes the following input sampling parameters:

a. Sample rate,
b. Interchannel phase, or skew,
c. Channel synchronization.

The effective input bandwidth is determined by the sample rate, while phase and synchronization control the relative timing of sampling between multiple channels. Phase and synchronization are considerations in applications that require consistent relative timing of sampling among multiple channels or multiple boards.

Clocking multiple converters from a single sample rate clock prevents the *sampling drift* that occurs when converters are clocked from different sources. *Synchronization* causes the converters in all channels to initiate conversions simultaneously, and can be used to eliminate *sampling skew* between channels.

3.6.1 Sample Rate Control

3.6.1.1 Rate Clock Organization

Sample rates are derived from two internal, independent rate generators, or from a single external hardware clock, as shown in Figure 3.6.1.1. All available input channels are divided equally into two sample groups, and the sample rates for all channels are controlled by the following operations:

a. Assignment of each group to an internal rate generator or to the external clock,
b. Rate generator frequency selection,
c. Rate divisor selection.

3.6.1.2 Rate Generator Assignment

A 4-bit code RATE SOURCE in the Rate Assignments register selects either an internal rate generator or the external sample rate clock as sample rate source. Group selection codes are arranged in the register as shown in Table 3.6.1.2-1, and use the assignment codes listed in Table 3.6.1.2-2. Channels in a group with a rate assignment of "none" are disabled and do not provide data to the input data buffer.

Note: If scan-synchronization is selected (Section 3.10), the ADC's in all channels are automatically clocked by the Channel-00 ADC clock.

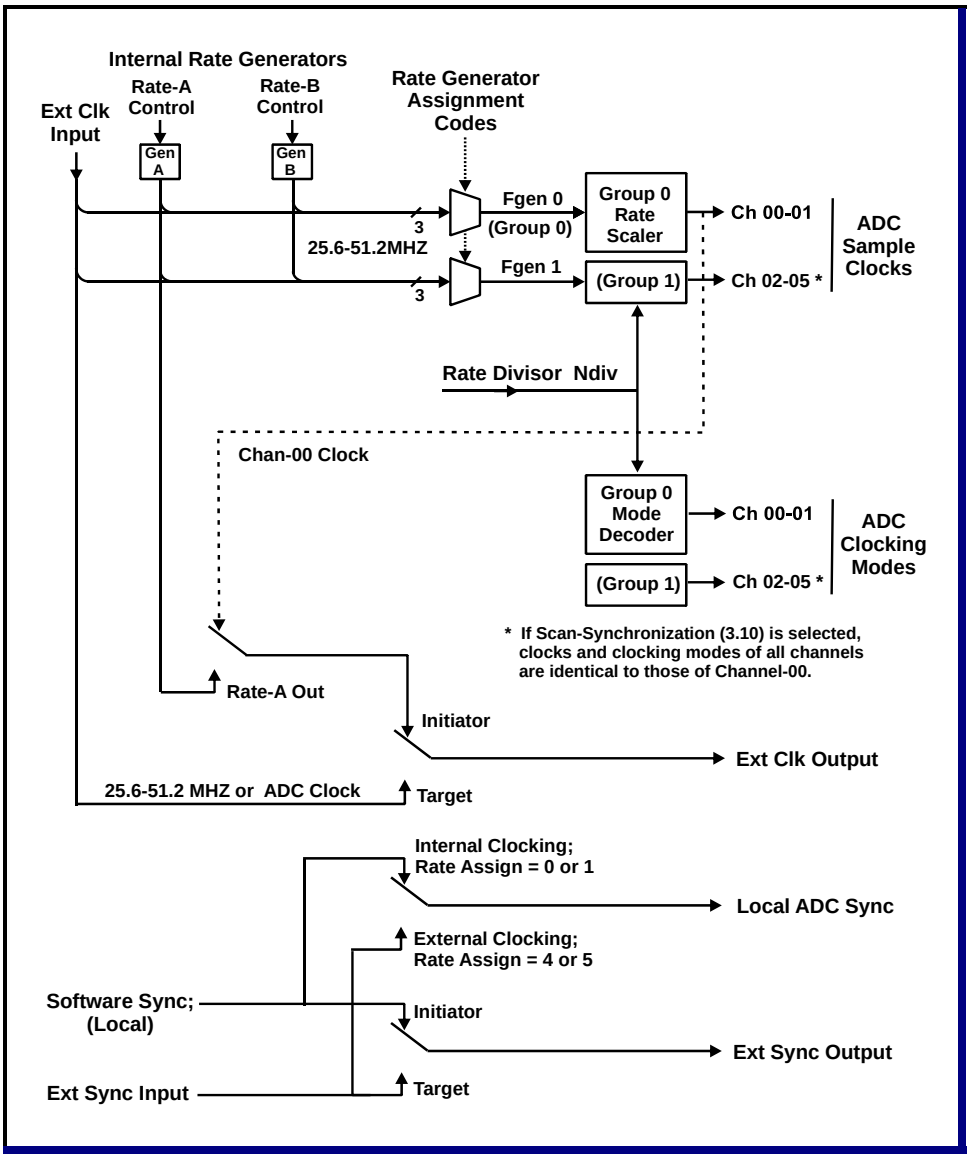

Figure 3.6.1.1. ADC Clock and Sync Organization, 6 Channels

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	6-CHAN BOARD	4-CHAN BOARD
0	Channels 00-01	00, 01
1	Channels 02-05	02, 03

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 RATE SOURCE	0
D[07..04]	GROUP 1 RATE SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	RATE CLOCK SOURCE
0	Rate Generator-A
1	Rate Generator-B
2	(Reserved)
3	(Reserved)
4	External Sample Clock (as Rate-A generator input)
5	Direct External Sample Clock (routed directly to ADC)
6-7	None (Disabled)
8-15	(Reserved)

3.6.1.3 Sample Clock Generation

A rate divisor integer **Ndiv** controls a *rate divisor* for the rate generator or external clock input. Rate divisors are arranged in the Rate Divisor register as shown in Table 3.6.1.3.

Table 3.6.1.3. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0505h**

BIT FIELD:	GROUP DIVISOR
D[07..00]	RATE DIVISOR 0 (**Ndiv**): 0 - 25
D[15..08]	RATE DIVISOR 1 (**Ndiv**): 0 - 25
D[31..16]	(Reserved)

The ADC sample rate **Fsamp** is determined by the rate generator frequency **Fgen** and a rate **DIVISOR** as: (all values in decimal)

$$\textbf{Fsamp = Fgen / (512 * DIVISOR),} \qquad \textbf{(3-1)}$$

where **Fsamp** and **Fgen** are in kilohertz, and **DIVISOR** is defined as:

If Ndiv > 0, then DIVISOR = Ndiv,
If Ndiv = 0, then DIVISOR = 0.5,

where **Ndiv** can have any integer value from zero through 25, and **Fgen** has a range of 25.6 MHz through 51.2 MHz.

If the clock source is an internal rate generator, **Fgen** is determined by **Nrate** as described in Paragraph 3.6.1.4. If the source is the external clock input, then **Fgen** equals the frequency of the external clock.

Note: The ADC's operate in one of three different clocking modes, with each mode determined by the assigned sample rate. In addition to establishing the sample rate division factor **DIVISOR**, the integer **Ndiv** also controls the ADC clocking mode.

3.6.1.4 Rate Generator Control

Fgen is generated by an internal phase-locked loop (PLL) oscillator. The frequency **Fgen** of the oscillator is related to a reference frequency **Fref** by integers **Nvco** and **Nref** (Table 3.6.1.4-1) as:

$$\textbf{Fgen} = \textbf{Fref} * \frac{\textbf{Nvco}}{\textbf{Nref}} \quad , \qquad \textbf{(3-2)}$$

where **Nvco** and **Nref** each has a maximum range from 30 to 1000, and **Fref** is the frequency of the reference oscillator, which has a standard frequency of **32.768MHz**. Table 3.6.1.4-3 is a summary of sample rate control parameters.

*Because specific applications might require custom values for **Fref**, an approximate measurement of the installed PLL reference oscillator frequency is available in the PLL Reference Freq register listed in Table 3.1. This value is determined at initialization, and equals **Fref** in Hertz with an accuracy of approximately 0.02-percent. It is intended as an indicator only, and is not recommended as a source for the actual **Fref** frequency.*

NOTE: Nvco and Nref each has a maximum range from 30 to 1000. For optimum performance, select the *lowest* possible values for Nvco and Nref.

By combining Equation 3-2 with Equation 3-1 in Section 3.6.1.3:

$$\frac{\textbf{Nvco}}{\textbf{Nref}} = \frac{\textbf{Fsamp} * 512 * \textbf{DIVISOR}}{\textbf{Fref} \text{ (32.768MHz)}} \quad . \qquad \textbf{(3-3)}$$

Table 3.6.1.4-1. PLL Rate Control Registers

Offset: Rate-A: 0004h, Rate-B: 0008h **Default: 0040 0032h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[09..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 30-1000.
D[15..10]	R/W	(Reserved)	---
D[25..16]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 30-1000.
D[31..26]	R/W	(Reserved)	---

* Both rate generators default to 25.6MHz.

Table 3.6.1.4-2. Summary of PLL Sample Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Factor	**Nvco**	30-1000
Reference Factor	**Nref**	30-1000
Rate Divisor	**Ndiv**	0 - 25
Reference Frequency	**Fref**	Standard value = 32.768MHz

The following examples illustrates one of several methods for determining **Nvco** and **Nref**: (Calculating the optimum values for integers **Nvco** and **Nref** can often be simplified by converting all variables, including **Fref**, into products of their prime factors):

EXAMPLE: Required sample rate **Fsamp** is **15.360 kHz**. **Fref = 32.768 MHz**:

1. Insert the **Fref** and required **Fsamp** values into Equation 3-3, expressing both in Hertz.

$$\frac{\mathbf{Nvco}}{\mathbf{Nref}} = \frac{\mathbf{15360 * 512 * DIVISOR}}{\mathbf{32768000}} .$$

2. Convert **Fref** and **Fsamp** into their prime factors, and simplify the fraction by canceling all factors that are duplicated in the numerator and denominator

$$\frac{\mathbf{Nvco}}{\mathbf{Nref}} = \frac{\mathbf{(2^{10} * 3 * 5) * (2^{9}) * DIVISOR}}{\mathbf{2^{18} * 5^{3}}} = \frac{\mathbf{6 * DIVISOR}}{\mathbf{25}} .$$

3. Select a value for **DIVISOR** that adjusts the value of the fraction to between 0.78 and 1.56 (25.6MHz to 51.2MHz /32.768MHz), with unity being ideal. In this case, use **DIVISOR = 4:**

$$\frac{\mathbf{Nvco}}{\mathbf{Nref}} = \frac{\mathbf{24}}{\mathbf{25}}$$

4. Multiply both numerator and denominator by an integer that produces the lowest possible in-range values for **Nvco** and **Nref**, which must be 30 or greater. In this case, multiply by 2:

$$\frac{\mathbf{Nvco}}{\mathbf{Nref}} = \frac{\mathbf{48}}{\mathbf{50}} .$$

5. Final Results: **Nvco = 48; Nref = 50; DIVISOR = 4**.

To confirm the results, first use Equation 3-2 to verify that the rate generator frequency **Fgen** is within the specified range of 25.6 - 51.2 MHz. If **Fgen** is out of range, select another **DIVISOR** value in Step-3:

$$\text{Fgen} = \text{Fref} * \frac{\text{Nvco}}{\text{Nref}}$$

$$= 32{,}768{,}000 \text{ Hz} * \frac{48}{50} = \underline{31{,}457{,}280 \text{ Hz}}.$$

Finally, use Equation 3-1 to verify the sample rate **Fsamp**:

$$\text{Fsamp} = \frac{\text{Fgen}}{512 * \text{DIVISOR}}$$

$$= \frac{31{,}457{,}280 \text{ Hz}}{512 * 4} = \underline{15{,}360 \text{ Hz}} \ .$$

3.6.1.5 Direct External Clocking

If the rate assignment selection (Table 3.6.1.2-2) is "Direct External Sample Clock," the signal at the external clock input is routed directly to the ADC's without modification. This configuration eliminates the effects of the Rate Control registers, and gives the external clock source direct control of the ADC's.

Although the Rate Control A/B registers and the Rate Divisor register **(Ndiv**) have no effect on the clocking frequency in this configuration, the ***clocking mode*** of the ADC's must be controlled by **Ndiv** as shown in Figure 3.6.1.1. Table 3.6.1.6 shows the relationships between the sample rate **Fsamp**, the external clock frequency, and the required values for **Ndiv**.

Table 3.6.1.5. Direct External Clocking

Sample Rate Fsamp (KSPS)	External Clock Frequency	Divisor Integer Ndiv
2-50	256 * Fsamp	**2 thru 25**
50-100	128 * Fsamp	**1**
100-200	64 * Fsamp	**0**

3.6.1.6 Harmonically Locked Channels

Channel groups operating at different frequencies that are exact submultiples of a common frequency perform conversions repetitively, relative to a sampling frame, and are *harmonically locked*. An example of this might be two groups operating from the same Fgen source at 25.6 MHz, with Ndiv values of 2 and 8. Using Equation 3-1 in Paragraph 3.6.1.3, the corresponding sample rates for the two groups would be 25 KSPS and 6.25 KSPS, respectively.

3.6.2 Channel Synchronization

Due to the oversampling nature of delta-sigma conversion, each conversion represents a sampling interval consisting of multiple clock cycles, and simply operating all converters from a common clock does not ensure simultaneous, or skew-free, sampling. To ensure simultaneous sampling, the converters must be synchronized to perform conversions simultaneously relative to a common point in time. Thereafter, the converters will continue to sample simultaneously while operating from a common clock.

Synchronization is invoked by **clearing** the ASYNCHRONOUS SYNC control bit ***LOW*** in the BCR. This is the default state after initialization. Completion of the synchronization sequence is indicated by the CHANNELS READY flag in the BCR undergoing a Low-to-High transition (Paragraph 3.4.3). The CHANNELS READY transition can be selected as a condition for an interrupt request event.

3.6.3 Multiboard Operation

Multiple PC104P-24DSI6LN boards can be connected together to share a common sampling clock and synchronization command. One of the boards is designated as the *initiator*, and the remaining boards are designated as *targets*. A board is designated as an initiator by setting the INITIATOR control bit HIGH in the BCR, or as a target when the control bit is LOW. *The INITIATOR control bit controls only the sources of the external clock and sync outputs, and has no other effect.*

The TTL EXTERNAL SYNC I/O control bit in the BCR selects single-ended TTL logic levels for the external clock and sync I/O signal when HIGH, or differential LVDS logic when LOW.

3.6.3.1 External Sample Clock

Target boards receive an external clock from the external clock input connection, and duplicate the input clock at the external clock output connection (Figure 3.6.1.1). The external clock input is designated as the clocking source by writing either the "External Sample Clock" or "Direct External Sample Clock" assignment code to the target boards' Rate Assignments register described in Paragraph 3.6.1.2. For calculation of target board sample rates, the external sample clock corresponds to the rate generator frequency **Fgen** described in Section 3.6.1 if "External Sample Clock" is selected, or provides the ADC sample clock directly if "Direct External Sample Clock" is selected.

An ***initiator*** provides an external clock output from either of two sources. If the RATE GEN EXT CLOCK OUT control bit in the BCR is LOW (default), the external clock output is identical to the Group 00 ADC sample clock, which equals the internal rate generator output divided by the rate divisor. If the control bit is HIGH, the rate generator unmodified output provides the external clock.

NOTE: The INITIATOR control bit controls only the sources of the external clock and sync output signals, and has no other effect.

Multiple boards can all be configured as initiators and operated in a "star" configuration to operate from a single rate generator. To avoid overloading the LVDS source driver, an LVDS distribution module usually is required in this configuration.

3.6.3.2 External Sync

Boards that are hardware-configured for multiboard synchronization initiate a *synchronization sequence* each time a sync pulse is generated by the initiator board.

The SOFTWARE SYNC control bit in the BCR can be used also to clear the buffers on the initiator and target boards simultaneously, by first setting the CLEAR BUFFER ON SYNC control bit HIGH in the BCR.

3.6.3.3 ADC Acquisition Rate Output

The ADC clocking frequency is a multiple of the actual acquisition rate, also referred to as the word rate. The frequency multiple equals the oversampling factor listed in Table 3.6.1.5 as x64, x128 or x256, and it is this frequency that appears at the EXT CLK OUT pin(s) in the system I/O connector when operating in the initiator mode.

However, if the ADC RATE OUT control bit is set HIGH in the BCR, a positive 30-100ns pulse is generated at the EXT CLK OUT pin(s) in the system I/O connector simultaneously with the acquisition of each data sample from the ADC's. Consequently, this pulse occurs at the true data sampling rate, or *word rate*, and is independent of the oversampling factor.

The ADC RATE OUT control function is implemented in firmware Revision 0900 and higher.

3.6.4 ADC Input Coupling

ADC input coupling defaults to DC-coupled, and can be selected as AC-coupled by setting the AC INPUT RESPONSE control bit HIGH in the BCR. The dynamic range is significantly higher if AC coupling is selected, and the low-end of the AC-coupled passband is -3dB at:

-3dB Low-end Frequency = Fsamp / 48,000,

where Low-end Frequency is expressed in Hz and Fsamp is in samples per second.

3.7 Autocalibration

Autocalibration is not implemented in this configuration.

3.8 Interrupt Control

In order for the board to generate a PCI interrupt on INTA#, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described below in Paragraph 3.8.2.

3.8.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The condition for the interrupt request is selected as shown in Table 3.8.1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the PCI bus clears the BCR request flag. A local interrupt request is generated automatically at the end of initialization.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	(Reserved)
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	(Reserved)
6	(Reserved)
7	(Reserved)

3.8.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX™ PCI-9080 reference manual..

3.9 DMA Operation

DMA transfers from the analog input buffer are supported in either of two DMA channels with the board operating as bus master. Table 3.9.1 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** Channel-0 DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***exceeds the selected buffer threshold*** *(Table 3.5.3).*

The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The number of values read from the buffer equals the threshold value *plus one*,
(c) The buffer is cleared,
(d) The board is reset,

The first occurrence of any of these events terminates the DMA request.

3.10 Scan Synchronization

Although the data sequence for any specific channel in the data buffer represents the actual sampling sequence for that channel, the ordering of multiple channels in the buffer can vary due to the asynchronous nature of the sample clock relative to the board's master clock. These variations in channel order can occur even though all channels are synchronized to a common sample clock.

Variations in the ordering of multiple channels can be eliminated by synchronizing the acquisition of each scan to the board's master clock. This ***scan-synchronization*** can be effective only if all active channels are operating from a common clock source.

Note: References to *channel synchronization* in this manual pertain to the situation in which the sampling of all input channels occurs simultaneously. *Scan-synchronization* refers to the synchronization of discrete data scans to the master clock, to ensure a consistent ordering of data channels in the data buffer.

For synchronized scans, the channel sequence for each scan in the buffer is ordered from lowest to highest. All samples in each scan represent the same sample event, and are arranged beginning with the lowest active channel and proceeding upward through the highest active channel. Table 3.10.1 illustrates examples of channel sequences in both synchronized and nonsynchronized scans in which eight channels are active. Scan synchronization is invoked by clearing the ASYNCHRONOUS SCAN control bit LOW in the BCR.

Table 3.10.1. Channel Order (Active channels 00-05)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	345012	012345
Tn+1	501234	012345
Tn+2	012345	012345
Tn+3	450123	012345
Tn+4	123450	012345

Synchronous scanning is the default condition after a board reset. To disable synchronous scanning, set the ASYNCHRONOUS SCAN control bit HIGH in the BCR.

To enable synchronous scanning, set then clear the ASYNCHRONOUS SCAN control bit in the BCR, and wait for the CHANNELS READY flag (3.4.3) in the BCR to undergo a LOW-to-HIGH transition. While the CHANNELS READY flag is LOW, the following sequence is executed by the local controller:

1. The Group-0 sample clock (Section 3.6.1) is distributed to all input channels,
2. All ADC's are channel-synchronized (Section 3.6.2),
3. All channels are scan-synchronized.

The buffer clears to empty, and the first two scans are discarded to ensure full synchronization. Subsequent samples are scan-synchronized as described above. The Channels-Ready flag can be used to generate an interrupt at the end of the process.

Notice that all enabled input channels receive the sample clock selected for Group-0 *while operating in the scan-synchronized mode*, and the sample clock settings for Group-1 are ignored. Disabled groups remain disabled.

Use the following sequence to enable synchronous scanning of multiple boards (Paragraph 3.6.3)

Synchronize ADC's:

1. On all boards: Set, then clear ASYNCHRONOUS SCAN;
   Wait for Channels Ready LOW-to-HIGH on all boards (LOW 1-100ms).
   (Sampling is synchronized on each board, but sample-skewed between boards)
2. On Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on all boards (LOW 1-100ms).
   (All ADC's are scan synchronized; but data in the buffers is still skewed)

Global Buffer Clear:

3. On all boards: Set the CLEAR BUFFER ON SYNC bit,
4. On Initiator: Set SOFTWARE SYNC;
   Wait for Channels Ready LOW-to-HIGH on the initiator. (LOW 10us to 5ms),
   (All ADC's and buffers are scan-synchronized)
5. On all boards: Clear the CLEAR BUFFER ON SYNC bit.

3.11 Board Configuration Register

The read-only board configuration register (Table 3.11.1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.11.1. Board Configuration Register

Offset: 0000 0024h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D15	Firmware Revision
D16	High if 6 channels are available; Low for 4 channels.
D17-18	Indicates Input Voltage Range: 0 => ±10V 1 => ±5V 2 => ±2.5V 3 => (Reserved)
D19-20	Indicates Image Filter frequency: 0 => 270kHz (Standard) 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D21	High for extended temperature operation, Low for commercial.
D22	Model identification flag. High only for xxx_24DSI6LN
D23-D31	(Reserved)

3.12 GPS Synchronization *(Firmware revisions 8103 and higher)*

To synchronize input sampling to an external timing reference, the external sync input pins in the I/O connector can be configured to accept a 1PPS GPS clock. The GPS input defaults to differential LVDS signaling, but TTL levels can be accommodated by setting the TTL EXTERNAL SYNC I/O control bit HIGH in the BCR.

While GPS synchronization is enabled, the functions normally associated with the external sync input are disabled (3.6.3).

NOTE: GPS synchronization requires that all active channels operate from a common rate generator, and that scan-synchronization is in effect (3.10). That is, the ASYNCHRONOUS SCAN control bit must be in the default LOW state in the BCR.

3.12.1 Locking Sequence

GPS synchronization is enabled by setting the ENABLE GPS SYNC control bit high in the GPS Synchronization control register (Table 3.12.1). Setting this bit clears the input buffer and initiates a locking sequence in which the GPS signal and sampling frequency are verified to be correct. Input acquisition is disabled during the locking sequence, which has a normal duration of 2-4 seconds. Erratic or marginal timing characteristics may extend this interval.

At the end of the locking sequence, assertion of the GPS LOCK status bit indicates that the GPS input has been detected and acknowledged to be approximately 1PPS. The SAMPLE RATE LOCK status bit is set HIGH if the internal sample rate equals the number in the TARGET SAMPLE RATE bit field. If either of these tests fails, the associated status bit is deasserted and the locking sequence is repeated.

Table 3.12.1. GPS Synchronization Control Register

Offset: 001Ch **Default: 0000 2000h**

BIT FIELD	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D19	R/W	TARGET SAMPLE RATE	0 2000h	Required (target) number of ADC samples per second.
D20	R/W	ENABLE GPS SYNC	0	When HIGH, enables synchronization to a 1PPS GPS input on the EXT SYNC INP HI connector pin. The GPS input is treated as a standard external sync input (3.6.3) when this bit is LOW.
D21	R/W	SELECT WIDE TOLERANCE	0	When HIGH, increases the correction tolerance for a lock condition from one sample per GPS cycle to five.
D22	R/W	NEGATIVE GPS SYNC	0	The GPS input is synchronized to the positive (low-to-high) edge of the signal when this bit is low, or to the negative (high-to-low) edge when this bit is HIGH.
D23	R/W	(Reserved)	0h	---
D24	RO	GPS LOCK	0	Indicates that the 1PPS GPS input has been detected and verified.
D25	RO	SAMPLE RATE LOCK	0	Indicates that the ADC sample rate is locked to the GPS input signal.
D26-31	RO	(Reserved)	0h	---

Normally, the GPS input is detected on the high-going (positive) edge of the signal. To accommodate low-going (negative) GPS input pulse signals, the NEGATIVE GPS SYNC control bit reverses the polarity of the GPS input.

3.12.2 Sample Rate Adjustment

When full lock has been obtained, i.e.: both GPS and Sample Rate locked, the number of ADC samples (Nsamp) acquired during each ensuing second is compared with the TARGET SAMPLE RATE bit field (Ntarget) in the GPS Synchronization control register. Subsequent action depends upon the value of Nsamp as:

Nsamp = Ntarget: No adjustment required,
Nsamp = Ntarget+1: Discard the next set of samples from all active channels,
Nsamp = Ntarget-1: Repeat the last acquired sample set for active channels,

Ntarget +1 < Nsamp < Ntarget -1: Disable acquisition and repeat the locking sequence.

If the SELECT WIDE TOLERANCE control bit is HIGH, the maximum correction increases from ±1 to ±5, and the last condition changes to:

Ntarget +5 < Nsamp < Ntarget -5: Disable acquisition and repeat the locking sequence,

NOTE: Due to the 25PPM tolerance of the internal clock oscillator, the Wide-Tolerance mode is recommended for sample rates greater than 35 KSPS.

3.12.3 Synchronization Example

The following procedure would establish GPS synchronization with a sample rate of 8192 samples per second and a TTL GPS input signal.

1. Set the TTL EXTERNAL SYNC I/O control bit HIGH in the BCR. (The TTL GPS input signal must be connected between Pins A34 (Signal input) and A32 (signal return, or ground) in the system I/O connector.) Refer to Sections 2.2.2 and 2.4.1.

3. Establish the nominal sample rate as 8192 SPS:
   Select the following control values for the VCO (Section 3.6.1.4.1):
   Nvco = 64 (40h), Nref = 125 (7Dh), Ndiv = 4.

   From equation 3.3 in Section 3.6.1.4.1:
   Fsamp(SPS) = (Nvco/Nref) * 64000/DIVISOR.
   = (64/125) * 64000/4,
   Fsamp(SPS) = 8192.

3. Wait for the CHANNELS READY status bit in the BCR to go HIGH.

4. In the GPS Synchronization control register:
   Write the value 8192 (02000h) to the TARGET SAMPLE RATE bit field,
   Set the ENABLE GPS SYNC control bit HIGH.

If the GPS input signal is present, the GPS LOCK and SAMPLE RATE LOCK status bits go HIGH within four seconds, typically, and synchronous acquisition commences.

3.13 Settling Time Considerations

An abrupt change in the analog configuration generally is followed by a 'settling' interval during which the analog networks are transitioning to a new state, and during which specified performance is suspended. Abrupt changes include:

- A change in voltage range or sample rate,
- A major input step-change,
- A system or local reset,
- Power application.

The settling time required to reestablish specified performance depends upon the type of disruption, and can vary from tens of milliseconds for a change in voltage-range, to as long as 10-15 minutes after the initial application of power. For *most* configuration changes other than the application of power, specified performance should resume after a settling interval of 20-100 milliseconds. Low-frequency filters will extend the settling interval by an amount that depends upon the filter characteristics. In general, the longest settling delay consistent with application requirements should be implemented.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PC104P-24DSI6LN board contains three dual delta-sigma 24-Bit A/D converters and all supporting functions necessary for adding analog I/O capability to a PC104-*Plus* stack. A PCI interface adapter (Figure 4.1) provides the interface between the controlling PCI bus and an internal local controller through a 32-bit local bus. The local controller performs all internal configuration and data manipulation functions.

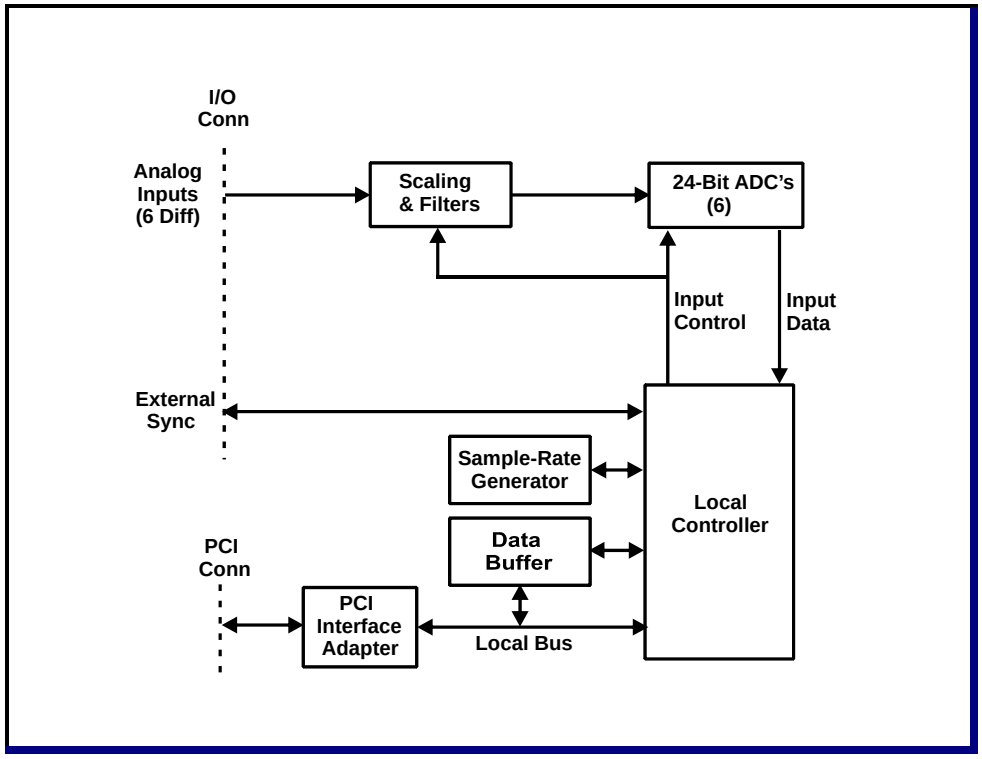

Figure 4.1. Functional Block Diagram

4.2 Analog Inputs

The six analog input channels are arranged in two channel groups, with each group containing one-half of the channels present on the board. Either group can be designated as either active or inactive, with only active groups sending input data to the data buffer. Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4.1. The analog input signal passes through a differential amplifier which removes any common mode voltage that might be present.

A range control attenuator adjusts the maximum level of the signal to the full-scale input range of 2.0 VRMS required by the ADC. High frequency noise and digital filter images are attenuated by a simple lowpass analog filter, the standard cutoff frequency for which is 270kHz.

The final conditioned, scaled and filtered input signal is digitized by each ADC into a 24-BIt serial data word that is deserialized into parallel format by the local controller. The local controller then attaches a 3-bit channel tag to the data word, applies offset and gain corrections, and finally transfers the corrected data to the input data buffer.

Antialias filtering is provided by each ADC in the form of a lowpass digital filter with a sharp cutoff frequency at approximately 40-50 percent of the sampling frequency. The digital filter has no filtering effect at multiples of the sampling clock. To prevent extraneous signal frequency components within these "filter images" from appearing in the passband, the hardware image filters shown in Figure 4.1 provides filtering within the digital filter images.

4.3 Autocalibration

Autocalibration is not implemented in this configuration.

4.4 Sampling Clocks

Each of two internal sample rate generators provides a frequency range of 25.6 - 51.2 MHz, which is divided down by a software-specified integers to provide sample rates from 2.0 KSPS to 200 KSPS. Either generator can be assigned to either channel group.

An external clock output can be assigned as the output of the rate generator, or as the ADC sample clock. A board from which a rate generator or ADC sample clock originates is a *clock initiator*. Boards that receive and retransmit the external clock are *clock targets*. Multiple targets can be controlled from a single initiator.

4.5 Power Control

Regulated precision supply voltages of +5 and ±14 Volts are required by the internal analog networks. Multiple DC/DC converters in the power conditioner use the coarsely regulated +5V input power from the PCI bus to produce preregulated DC voltages that subsequently are postregulated with linear regulators to the required supply voltages. Linear regulation ensures that the final power voltages delivered to the analog networks are well-regulated and free of noise.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers in the order in which they appear in Section 3.

Table 3.1. Control and Data Registers

LOCAL ADDR [1]	ACCESS MODE [2]	REGISTER	DEFAULT	DESCRIPTION
00	R/W	**Board Control (BCR)**	0000 2830h [3]	Board Control Register (BCR)
04	R/W	**Rate Control A**	0040 0032h	Rate Generator-A control
08	R/W	**Rate Control B**	0040 0032h	Rate Generator-B control.
0C	R/W	**Rate Assignments**	0000 0000h	Channel-group rate generator assignment
10	R/W	**Rate Divisors**	0000 0505h	Channel-group sample rate divisors.
14	R/W	(Reserved)	0000 0000h	---
18	RO	**PLL Reference Freq**	XXXX XXXXh	PLL reference frequency indicator.
1C	R/W	**GPS Synchronization**	0000 2000h	Controls sample rate GPS synchronization.
20	R/W	**Buffer Control**	0003 FFFEh [4]	Input buffer control and status
24	RO	**Board Configuration**	00XX XXXXh	Installed firmware and hardware options
28	RO	**Buffer Size**	0XXX XXXXh	Number of ADC values in the input buffer.
2C	RO	(Reserved)	---	---
30	RO (DMA)	**Input Data Buffer**	XXXX XXXXh	Input Data Buffer; Data and channel tag
34-7C	--	(Reserved)	---	---

[1] Offsets from the "PCI base address for local addressing".
[2] R/W = Read/Write; RO = Read-Only.
[3] Changes to 0000 6830h when the input buffer fills.
[4] Changes to 0103 FFFEh when the buffer fills.

Table 3.2. Board Control Register

Offset: 0000h **Default: 0000 2830h ****

DATA BIT	MODE	DESIGNATION	DESCRIPTION	SECTION
D00-03	R/W	(Reserved)	---	---
D04	R/W	OFFSET BINARY	Selects offset binary or two's complement input data format. Defaults HIGH to offset binary.	3.5.2.2
D05	R/W	INITIATOR	Selects INITIATOR or TARGET mode for external clock and sync signals. Defaults to Initiator mode.	3.6.3
D06	R/W	*SOFTWARE SYNC	Initiates a local ADC sync operation when asserted. Also generates an external sync output if INITIATOR mode is selected. Clears automatically.	3.6.3.2
D07	R/W	(Reserved)	---	---
D08	R/W	INTERRUPT A0	Interrupt event selection. Default is zero.	3.8.1
D09	R/W	INTERRUPT A1		
D10	R/W	INTERRUPT A2		
D11	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.	
D12	RO	(Reserved)	---	---
D13	RO	CHANNELS READY	LOW during any change in channel parameters. Asserted HIGH when ADC clocks are stabilized.	3.4.3
D14	RO	BUFFER THRESHOLD FLAG	Asserted HIGH when buffer contents exceed the assigned threshold.	3.5.3.1
D15	R/W	*INITIALIZE	Initializes the board when asserted HIGH.	3.3.2
D16	R/W	ASYNCHRONOUS SCAN	***Disables*** synchronous sampling mode when ***HIGH***.	3.10
D17	R/W	CLEAR BUFFER ON SYNC	Changes the context of the SOFTWARE SYNC control bit changes to CLEAR BUFFER.	3.5.3.2
D18	R/W	RATE-A EXT CLOCK OUT (Initiator Mode only)	When HIGH: Selects the Rate-A generator as the external clock output source. When LOW: Selects the Group-00 sample clock as the output. (If Group-00 external clocking is selected, the output is driven by the Rate-A generator and the Group-00 divisor).	3.6.3.1
D19	R/W	(Reserved)	---	---
D20	R/W	TTL EXTERNAL SYNC I/O	Selects TTL external sync I/O configuration.	2.4.1, 3.6.3
D21	R/W	(Reserved)	---	---
D22	R/W	AC INPUT RESPONSE	Selects AC input coupling for all ADC's when HIGH; DC coupling when LOW.	3.6.4
D23	R/W	ADC RATE OUT	When this bit is HIGH, a positive pulse is generated at the EXT CLK OUT pin(s) in the I/O connector each time an ADC sample is acquired.	3.6.3.3
D24-31	RO	(Reserved)	---	---

* Cleared automatically. R/W = Read/Write; RO = Read-Only.

** Changes to 0000 7830h when the input buffer fills.

Table 3.3.1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal EEPROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms
A/D converters and clocks are initialized	5 seconds

Table 3.5.2. Input Data Buffer Organization

Offset: 0000 0030h **Default: XXXX XXXXh**

SELECTED DATA WIDTH	RESERVED (Zero)	CHANNEL TAG	ZERO-PAD	CHANNEL DATA VALUE
16 Bits	D[31..29]	D[28..24]	D[23..16]	D[15..0]
18 Bits	D[31..29]	D[28..24]	D[23..18]	D[17..0]
20 Bits	D[31..29]	D[28..24]	D[23..20]	D[19..0]
24 Bits	D[31..29]	D[28..24]	---	D[23..0]

Table 3.5.2.2. Analog Input Data Coding; 16-Bit Data Field

	DIGITAL VALUE (Hex)	
ANALOG INPUT LEVEL	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	FFFFh	7FFFh
Zero plus 1 LSB	8001h	0001h
Zero	8000h	0000h
Zero minus 1 LSB	7FFFh	FFFFh
Negative Full Scale plus 1 LSB	0001h	8001h
Negative Full Scale	0000h	8000h

Table 3.5.3. Buffer Control Register

Offset: 0000 0020h **Default: 0003 FFFEh ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[17..00]	R/W	BUFFER THRESHOLD	Buffer Flag Threshold
D[18]	R/W	DISABLE BUFFER INPUT	Disables inputs to the data buffer.
D[19]	R/W	CLEAR BUFFER **	Clears (empties) the buffer
D[21..20]	R/W	DATA WIDTH	Controls the width of the buffer data field as: 0 => 16 bits 1 => 18 bits 2 => 20 bits 3 => 24 bits.
D[23..22]	RO	(Reserved)	---
D[24]	R/W	BUFFER OVERFLOW ***	Reports buffer overflow (Write on full)
D[25]	R/W	BUFFER UNDERFLOW ***	Reports buffer underflow (Read on empty)
D[31..26]	RO	(Reserved)	

* Changes to 0103 FFFEh when the buffer fills. ** Clears automatically. *** Clear by writing LOW, or by reset.

Table 3.6.1.1. Channel Groups

CHANNEL GROUP	6-CHAN BOARD	4-CHAN BOARD
0	Channels 00-01	00, 01
1	Channels 02-05	02, 03

Table 3.6.1.2-1. Rate Assignments Register

Offset: 0000 000Ch **Default: 0000 0000h**

BIT FIELD	DESIGNATION	CHANNEL GROUP
D[03..00]	GROUP 0 RATE SOURCE	0
D[07..04]	GROUP 1 RATE SOURCE	1
D[31..08]	(Reserved)	---

Table 3.6.1.2-2. Rate Generator Assignment Codes

ASSIGNMENT CODE	RATE CLOCK SOURCE
0	Rate Generator-A
1	Rate Generator-B
2	(Reserved)
3	(Reserved)
4	External Sample Clock (as Rate-A generator input)
5	Direct External Sample Clock (routed directly to ADC)
6-7	None (Disabled)
8-15	(Reserved)

Table 3.6.1.3. Rate Divisor Register

Offset: 0000 0010h **Default: 0000 0505h**

BIT FIELD:	GROUP DIVISOR
D[07..00]	RATE DIVISOR 0 (**Ndiv**): 0 - 25
D[15..08]	RATE DIVISOR 1 (**Ndiv**): 0 - 25
D[31..16]	(Reserved)

Table 3.6.1.4-1. PLL Rate Control Registers

Offset: Rate-A: 0004h, Rate-B: 0008h **Default: 0040 0032h ***

BIT FIELD	MODE	DESIGNATION	FUNCTION
D[09..00]	R/W	VCO FACTOR **(Nvco)**	PLL VCO factor; 30-1000.
D[15..10]	R/W	(Reserved)	---
D[25..16]	R/W	REF FACTOR **(Nref)**	PLL Reference factor; 30-1000.
D[31..26]	R/W	(Reserved)	---

* Both rate generators default to 25.6MHz.

Table 3.6.1.4-3. Summary of PLL Sample Rate Control Parameters

PARAMETER	NOTATION	RANGE
VCO Factor	**Nvco**	30-1000
Reference Factor	**Nref**	30-1000
Rate Divisor	**Ndiv**	0 - 25
Reference Frequency	**Fref**	Standard value = 32.768MHz

Table 3.6.1.6. Direct External Clocking

Sample Rate Fsamp (KSPS)	External Clock Frequency	Divisor Integer Ndiv
2-50	256 * Fsamp	**2 thru 25**
50-100	128 * Fsamp	**1**
100-200	64 * Fsamp	**0**

Table 3.8.1. Interrupt Event Selection

INTERRUPT A[2:0]	INTERRUPT EVENT CONDITION
0	Initialization completed. Default state.
1	(Reserved)
2	Channels Ready
3	Data Buffer threshold flag, LOW-to-HIGH transition
4	Data Buffer threshold flag, HIGH-to-LOW transition
5	(Reserved)
6	(Reserved)
7	(Reserved)

Table 3.9.1. Typical DMA Register Configuration; DMA Channel-0

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0030h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.10.1. Channel Order (Active channels 00-05)

	CHANNEL ORDER	
SAMPLE EVENT	NON-SYNCHRONIZED SCANS (Typical)	SYNCHRONIZED SCANS
Tn	345012	012345
Tn+1	501234	012345
Tn+2	012345	012345
Tn+3	450123	012345
Tn+4	123450	012345

Table 3.11.1. Board Configuration Register

Offset: 0000 0024h **Default: 00XX XXXXh**

BIT FIELD	DESCRIPTION
D00-D15	Firmware Revision
D16	High if 6 channels are available; Low for 4 channels.
D17-18	Indicates Input Voltage Range: 0 => ±10V 1 => ±5V 2 => ±2.5V 3 => (Reserved)
D19-20	Indicates Image Filter frequency: 0 => 270kHz (Standard) 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D21	High for extended temperature operation, Low for commercial.
D22	Model identification flag. High only for xxx_24DSI6LN
D23-D31	(Reserved)

Table 3.12.1. GPS Synchronization Control Register

Offset: 001Ch **Default: 0000 2000h**

BIT FIELD	MODE	DESIGNATION	DEFAULT	DESCRIPTION
D00-D19	R/W	TARGET SAMPLE RATE	0 2000h	Required (target) number of ADC samples per second.
D20	R/W	ENABLE GPS SYNC	0	When HIGH, enables synchronization to a 1PPS GPS input on the EXT SYNC INP HI connector pin. The GPS input is treated as a standard external sync input (3.6.3) when this bit is LOW.
D21	R/W	SELECT WIDE TOLERANCE	0	When HIGH, increases the correction tolerance for a lock condition from one sample per GPS cycle to five.
D22	R/W	NEGATIVE GPS SYNC	0	The GPS input is synchronized to the positive (low-to-high) edge of the signal when this bit is low, or to the negative (high-to-low) edge when this bit is HIGH.
D23	R/W	(Reserved)	0h	---
D24	RO	GPS LOCK	0	Indicates that the 1PPS GPS input has been detected and verified.
D25	RO	SAMPLE RATE LOCK	0	Indicates that the ADC sample rate is locked to the GPS input signal.
D26-31	RO	(Reserved)	0h	---

MIGRATION FROM PC104P-24DSI12

Appendix B

Migration From PC104P-24DSI12

Operation of the PC104P-24DSI6LN is very similar to that of the PC104P-24DSI12. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 provides a brief comparison of PC104P-24DSI12 and PC104P-24DSI6LN features.

Table B.1. PC104P-24DSI12 and PC104P-24DSI6LN Features Comparison

Feature	PC104P-24DSI12	PC104P-24DSI6LN
Number of Input Channels	**12**	**6**
Input Ranges	**±10V, ±5V or ±2.5V,** Software-controlled	**±10V, ±5V or ±2.5V,** Factory-configured
Calibration	**On-Demand Autocalibration**	**Fixed**
Conversion Resolution	24 Bits	24 Bits
Input Configuration	Differential	Differential
Local Clock	30 MHz	30 MHz
Data Buffer	256K-Sample FIFO	256K-Sample FIFO
Buffer Data Field	32 Active bits	32 Active bits
PCI Interface	PCI 2.3; D32; 33MHz/66MHz	PCI 2.3; D32; 33MHz/66MHz

B.2. Migration Issues

Section 2.0. Installation and Maintenance:

The number of input channels has changed, but the I/O pinout is a subset of the PC104P-24DSI12 pinout. Also, the internal reference is not implemented in this configuration, and the section pertaining to reference verification has been deleted.

Tables 3.1 and 3.2:

The default value for the BCR has changed. Those fields pertaining to the input mode, the input range, autocalibration, and filter selection have been redesignated as 'reserved'.

Paragraphs 3.4 and 3.7:

References to the input mode, the input range, or to autocalibration have been deleted.

Table 3.6.1.1. Channel Groups

Channel grouping has been modified for 4-channel and 6-channel configurations.

Paragraph 3.6.1.4: Rate Generator Control:

References to the legacy rate generator have been removed.

Table 3.10.1. Channel Order:

The example has been modified to reflect a 6-Channel configuration.

Table 3.11.1. Board Configuration:

Option fields have been modified to reflect the available ordering options.

Development Revision Record:

07-10-2008: Origination as preliminary draft.

08-11-2008: Table 3.3.1: Reduced the Initialization interval from 5 seconds to 1 second.
Table 3.11.1: Added model identification flag.
Table 3.6.1:1 Revised for 4 and 6-Channel configurations.

09-11-2008: Table 3.2: New control bit D22.
Paragraph 3.6.4: New paragraph.

01-05-2009: Table 3.2: New control bit D23.
Paragraph 3.6.3.3: New paragraph.

Additional copies of this manual or other General Standards Co. literature may be obtained from:

General Standards Corp.
8302A Whitesburg Dr.
Huntsville, Alabama 35802
Telephone: (256) 880-8787
FAX: (256) 880-8788

General Standards Corporation

High Performance Bus Interface Solutions

General Standards Corporation
Ph:(256)880-8787 FAX:(256)880-8788 Email: Solutions@GeneralStandards.com Web Site: http://www.GeneralStandards.com

MAN-PC104P-24DSI6LN