General Standards Corporation

High Performance Bus Interface Solutions

Rev: 081713

PCIe-16AO64C

16-Bit, 64/32-Channel, 500KSPS PCI Express Analog Output Board

With optional Outputs-Disconnect

REFERENCE MANUAL

--- PRELIMINARY ---

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PCIe-16AO64C board provides precision 16-bit high-speed analog output capability for PMC applications. 64 analog output channels offer either single-ended or balanced differential output ranges of ±10V and ±5V, or optionally 0 to +10V and 0 to +5V, and can be clocked simultaneously at rates up to 500 KSPS (Kilosamples per second) per channel. The board is functionally and mechanically compatible with the PCI Express Specification revision 1.0a.

Power requirements consist of +12 VDC and +3.3 VDC from the PCI Express bus in accordance with the specification, and operation over the specified temperature range is achieved with conventional cooling. Specific details of physical characteristics and power requirements are contained in the PCIe-16AO64C product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

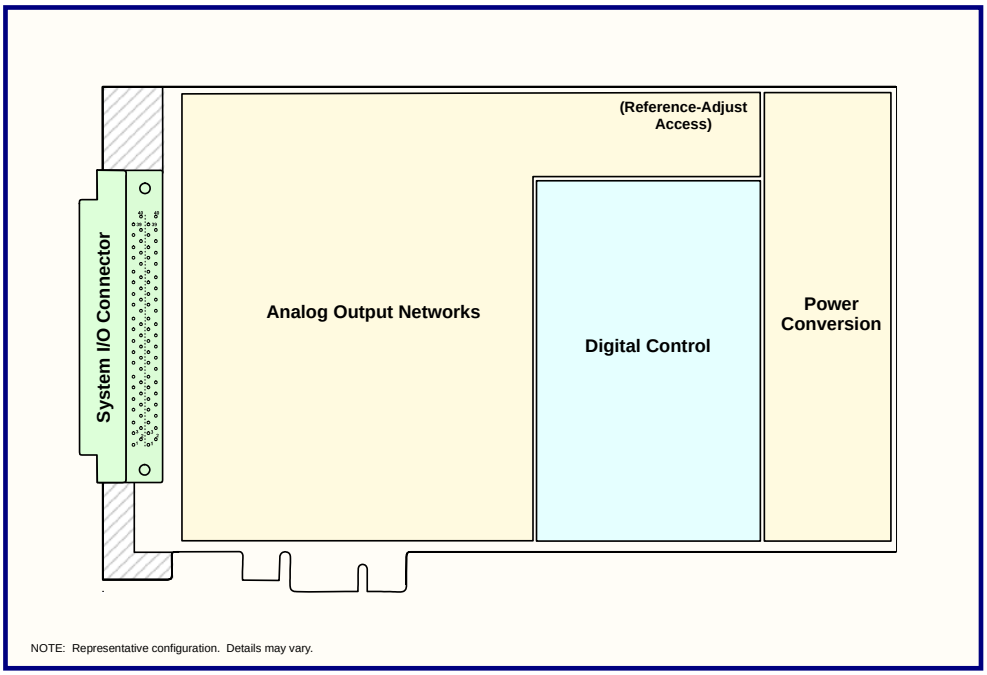

Figure 1.1-1. Physical Configuration

1.2 Functional Overview

Figure 1.2-1 outlines the internal functional organization of the board. The output clocking rate can be controlled by an internal rate generator, or by an external clock source. Each analog output channel implements an R-2R DAC, which minimizes latency and has no minimum clocking rate.

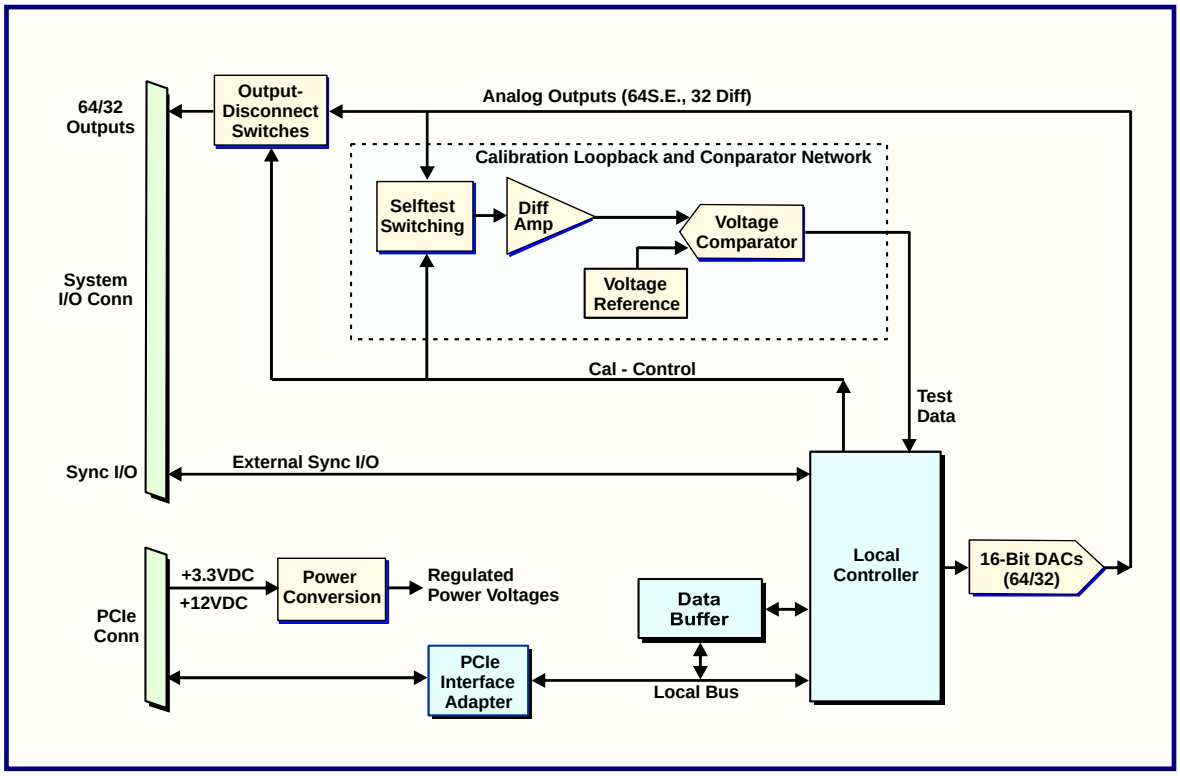

Figure 1.2-1. Functional Organization

An optional outputs-disconnect feature allows the outputs to be disconnected from the system I/O connector under software control. Internal selftest networks support on-demand autocalibration, which uses a single internal voltage reference to calibrate the offset and gain of each channel.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping package, carefully press the board into position on the host. Verify that the PCIe connector has mated completely and is seated against the host board.

Secure the PCIe/PCI bracket screw carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-080S-TG. The insulation displacement (IDC) Robinson Nugent cable connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connector Pin Functions

Single-Ended Signal *		
Pin	Row-A	Row-B
1	OUT00	OUT34
2	OUT01	OUT35
3	OUT02	OUT36
4	OUT03	OUT37
5	OUT04	OUT38
6	OUT05	OUT39
7	OUT06	OUT40
8	OUT07	OUT41
9	OUT08	OUT42
10	OUT09	OUT43
11	OUT10	OUT44
12	OUT11	OUT45
13	OUT RTN	OUT RTN
14	OUT RTN	OUT RTN
15	OUT12	OUT46
16	OUT13	OUT47
17	OUT14	OUT48
18	OUT15	OUT49
19	OUT16	OUT50
20	OUT17	OUT51
21	OUT18	OUT52
22	OUT19	OUT53
23	OUT20	OUT54
24	OUT21	OUT55
25	OUT22	OUT56
26	OUT23	OUT57
27	OUT RTN	OUT RTN
28	OUT RTN	OUT RTN
29	OUT24	OUT58
30	OUT25	OUT59
31	OUT26	OUT60
32	OUT27	OUT61
33	OUT28	OUT62
34	OUT29	OUT63
35	OUT30	OUT RTN
36	OUT31	OUT RTN
37	OUT32	DIG RTN
38	OUT33	CLK I/O
39	OUT RTN	DIG RTN
40	REM GND	TRIG I/O

Differential Signal *		
Pin	Row-A	Row-B
1	OUT00 HI	OUT17 HI
2	OUT00 LO	OUT17 LO
3	OUT01 HI	OUT18 HI
4	OUT01 LO	OUT18 LO
5	OUT02 HI	OUT19 HI
6	OUT02 LO	OUT19 LO
7	OUT03 HI	OUT20 HI
8	OUT03 LO	OUT20 LO
9	OUT04 HI	OUT21 HI
10	OUT04 LO	OUT21 LO
11	OUT05 HI	OUT22 HI
12	OUT05 LO	OUT22 LO
13	OUT RTN	OUT RTN
14	OUT RTN	OUT RTN
15	OUT06 HI	OUT23 HI
16	OUT06 LO	OUT23 LO
17	OUT07 HI	OUT24 HI
18	OUT07 LO	OUT24 LO
19	OUT08 HI	OUT25 HI
20	OUT08 LO	OUT25 LO
21	OUT09 HI	OUT26 HI
22	OUT09 LO	OUT26 LO
23	OUT10 HI	OUT27 HI
24	OUT10 LO	OUT27 LO
25	OUT11 HI	OUT28 HI
26	OUT11 LO	OUT28 LO
27	OUT RTN	OUT RTN
28	OUT RTN	OUT RTN
29	OUT12 HI	OUT29 HI
30	OUT12 LO	OUT29 LO
31	OUT13 HI	OUT30 HI
32	OUT13 LO	OUT30 LO
33	OUT14 HI	OUT31 HI
34	OUT14 LO	OUT31 LO
35	OUT15 HI	OUT RTN
36	OUT15 LO	OUT RTN
37	OUT16 HI	DIG RTN
38	OUT16 LO	CLK I/O
39	OUT RTN	DIG RTN
40	REM GND	TRIG I/O

* Outputs can be factory-configured for either single-ended or differential operation. In the differential configuration, odd-numbered channels become the 'LO' inputs of differential channel pairs.

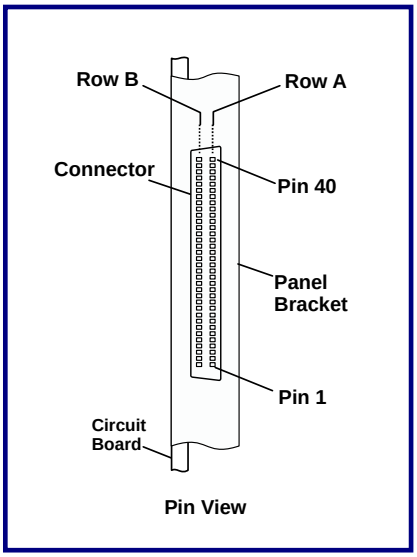

Figure 2. System I/O Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080S-TG** or equivalent.

2.3 System Configuration

2.3.1 Output Considerations

2.3.1.1 Output Configurations

The 64 analog output channels can be factory-configured either as 32 balanced 3-wire differential outputs or as 64 single-ended outputs.

Balanced differential outputs (Figure 2.3-1a) provide the highest immunity to system noise and interference, and are recommended in all systems in which the loads will accept differential inputs. Each of the HI and LO outputs carries one-half of the output signal, with the two halves operating as complementary signals of equal amplitude and opposite polarity. Since radiated interference usually affects both output lines simultaneously, the coupled interference appears as a common mode signal which will be attenuated in a differential load.

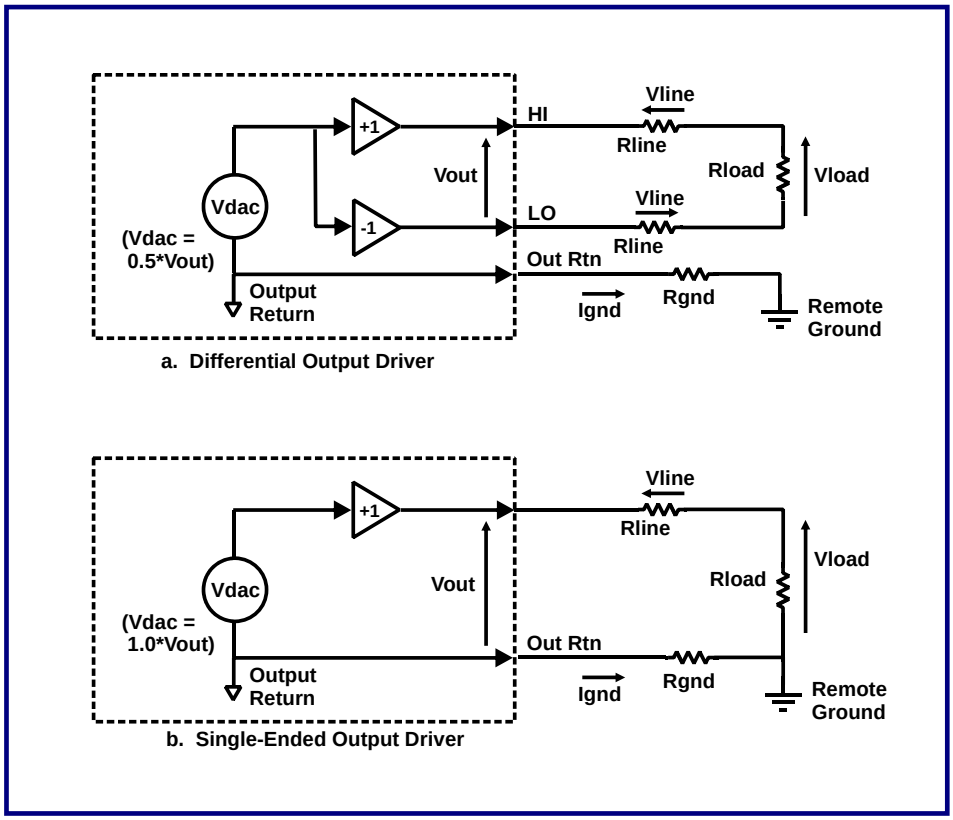

Figure 2.3-1. Output Configurations

For applications requiring single-ended outputs (Figure 2.3-1b), the output signal from each channel appears on the associated HI output pin, and is generated with reference to the output return pin. In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other

2.3.1.2 Line Losses

The voltage drop in ribbon cable can be a significant source of error in 16-bit systems, even with relatively short cables driving low-current loads. Figure 2.3-2 shows the effect of load current on the voltage drop in copper wire of various sizes. A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors in a 16-bit system, in which 1 LSB may represent only 153 microvolts (zero to +10V range). High impedance loads however, generally do not produce significant DC line loss errors.

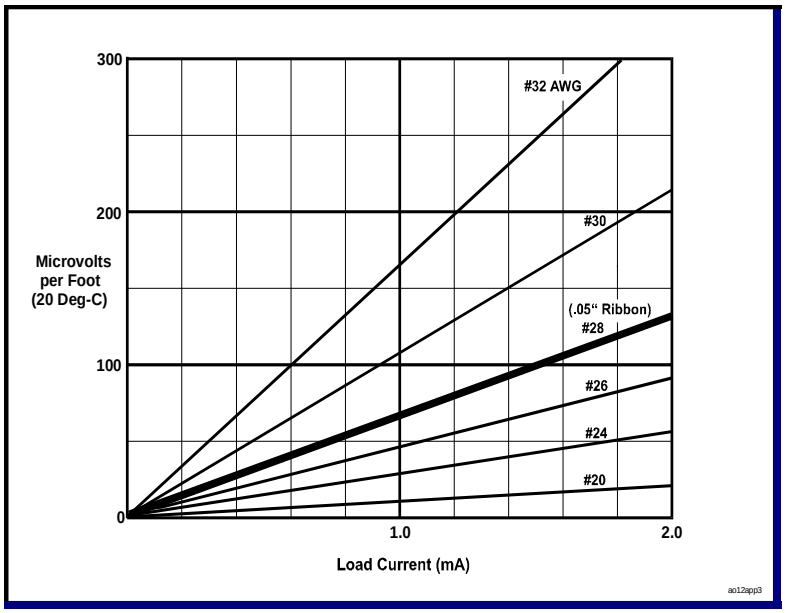

Figure 2.3-2. Line Loss Versus Load Current

2.3.1.3 Remote Ground Sensing

In single-ended applications, if a significant potential difference is expected between the ground connection at the load and the output return from the board, the use of remote ground sensing should be considered. When remote ground sensing is enabled through application software, the input signal at the REM GND pin in the I/O connector adjusts the output voltages of single-ended channels to compensate for a ground potential at the load.

To provide correction for the potential difference between the analog output return and the remote system ground, the REM GND input must be connected to the remote system ground, and remote sensing must be enabled by the control software. If remote ground sensing is not implemented, the REM GND input should be connected to OUT RTN.

The remote sensing input affects all analog output channels, and consequently can be a significant source of noise if not adequately protected from external interference.

NOTE: Remote ground sensing is disabled for differential output channels.

2.3.2 External Clock and Trigger I/O

External clock and trigger input and output signals are bidirectional single-ended TTL-compatible. When external clock and triggering are software-selected, the sample clock and burst trigger are routed through the CLK I/O and TRIG I/O pins in the system I/O connector.

2.3.2.1 Sample Clock I/O

When the board is operated as a***n Initiator***, the bidirectional CLK I/O signal generates an 120-180ns low-going TTL pulse each time the analog outputs are updated, and can be used to synchronize the analog output clocking of multiple *clock target* boards to a single clock initiator.

In the ***target*** mode, the CLK I/O pin becomes an input that can accept an external input to clock the analog outputs. The input must be a low-going TTL pulse with a minimum width of 100ns. Longer pulses are edge-detected on the low-going transition.

2.3.2.2 Burst Trigger I/O

If burst triggering is enabled by the control software, and the board is configured as a ***target,*** an external TTL input signal can initiate a data burst by applying a HIGH-to-LOW transition on the TRIG I/O pin in the I/O connector. In order for the trigger input to be acknowledged, the external input signal must go low for a minimum interval of 100 nanoseconds.

When the board is operated as an ***initiator***, the TRIG I/O pin is a TTL output pulse which goes low for 120-180 nanoseconds at the beginning of each triggered burst executed by the board.

2.3.3 Multiboard Synchronization

If multiple boards are to be synchronized together, the CLK I/O and/or the TRIG I/O pins from one board, the ***initiator***, are connected to the corresponding pins of one or more ***target*** boards (Figure 2.3-3). The controlling software determines specific clocking and burst triggering functions. The maximum number of targets depends upon both static loading and cable characteristics, and can vary from four to as many as eight.

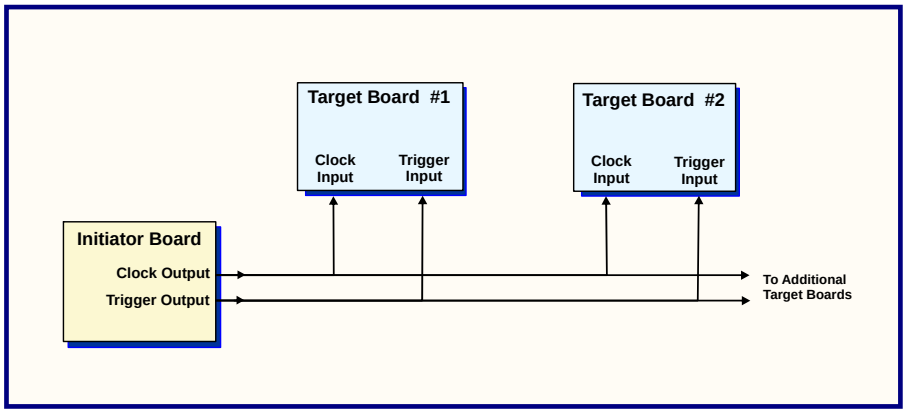

Figure 2.3-3. Multiboard Synchronization

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year should be sufficient. In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and input signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that is suspected to be defective should be returned to the factory for problem analysis and repair.

2.5 Reference Verification

All output channels are software-calibrated to a single internal voltage reference by an embedded autocalibration firmware utility. The verification procedure presented here describes the adjustment of the reference. For applications in which the system must not be powered down, the board can be calibrated under normal operating conditions while installed in the existing host.

2.5.1 Equipment Required

Table 2.5-1 lists the minimum equipment requirements for verifying and adjusting the internal voltage reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host computer with PCI Express slot	(Existing host)	---

2.5.2 Verification Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification.

Adjustment of the internal reference is performed with a single adjustment trimmer that is located at the top edge of the board. The adjustment seal on the trimmer should be removed before beginning the procedure, and the trimmer should be resealed with a suitable sealing agent after the adjustment has been completed. Thread-locking agents *should not* be used.

This procedure assumes that the board to be verified is installed in a suitable host. The board can be operating in any mode when the adjustment is performed.

1. Connect the digital multimeter between Pin-1(+) and Pin-3(-) of test connector J4 located at the top edge of the board (Figure 1.1-1).
2. If power has been removed from the board, apply power now and wait at least ten minutes before proceeding.
3. The digital multimeter indication should indicate +9.9000 ±0.0009 VDC. If the indication is not within this range, adjust the reference trimmer until an in-range indication is obtained.
4. Reference verification or adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PCIe-16AO64C is compatible with the PCI Express local bus specification revision 1.0a, and a PLX^{tm} PEX8311 adapter controls the one-lane interface. Configuration space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space.

After initialization has been completed, communication between the PCI Express bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All local data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers to the output data buffer. To ensure compatibility of applications with subsequent product upgrades, reserved bits should be written LOW.

Table 3.1-1. Control and Data Registers

Offset (Hex)	Register	Mode*	Default	Primary Function	Ref
00	BOARD CONTROL (BCR)	R/W	0000_4814h	Board Control Register (BCR)	3.2
04-08	(Reserved)	RO	0000_0000h	---	---
0C	BUFFER OPERATIONS	R/W	0000_1400h	Buffer control and status flags	3.4.2.1
10	ASSEMBLY CONFIGURATION	RO	00XX_XXXXh	Firmware revision and hardware options	3.10
14	Autocal Values **	R/W	0000_0XXXh	---	---
18	OUTPUT DATA BUFFER	WO	0000_0000h	Analog output FIFO buffer	3.4.2
1C	BUFFER SIZE	RO	0000_0000h	Number of data values in the buffer.	3.4.2.1
20	BUFFER THRESHOLD	R/W	0003_FFFEh	Buffer status-flag threshold value	3.4.2.1
24	RATE-A GENERATOR	R/W	0000_00C0h	Divisor for the Rate-A generator	3.4.3.1.2
28	RATE-B GENERATOR	R/W	0000_C000h	Divisor for the Rate-B generator	3.4.4.2.1
2C-3F	(Reserved)	RO	0000_0000h	---	---

* R/W = Read/Write; RO = Read-only; WO = Write-only . ** Maintenance register; shown for reference.

3.2 Board Control Register

The Board Control Register (BCR) controls primary board functions, including burst control, autocalibration, and interrupt event selection. Table 3.2-1 provides a brief description of each bit field in the BCR, as well as indicating an associated section in the text.

Table 3.2-1. Board Control Register

Offset: 0000h **Default: 0000_ 4814h [1]**

Bit	Mode	Designation	Def	Description	Ref
D00	R/W	CLOCK INITIATOR	0	Configures the CLK I/O pin as an output when HIGH.	3.4.3.1
D01	R/W	TRIGGER INITIATOR	0	Configures the TRIG I/O pin as an output when HIGH.	3.4.4.2.1
D02	R/W	DISCONNECT OUTPUTS	1 (1)	Disconnects all outputs from the system I/O connector when HIGH. (Active only if the Outputs Disconnect option is installed).	3.4.1.5
D03	R/W	REMOTE GROUND SENSE	0	Enables the remote-ground sense feature when HIGH.	3.7
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.	3.4.1.3.2
D05	R/W	ENABLE RATE-A	0	Enables the Rate-A generator when HIGH.	3.4.3.1.2
D06	R/W	ENABLE RATE-B	0	Enables the Rate-B generator when HIGH.	3.4.3.1.2
D07	R/W	(Reserved)	0	---	---
D08-D10	R/W	INTERRUPT A0-A2	0	Interrupt event selection.	3.6
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board asserts an interrupt request. Clears the request when cleared LOW by the bus.	
D12	R/W	BUFFER THRESHOLD FLAG	0	High when the number of values in the buffer exceeds the selected threshold value. (Duplicated in the buffer threshold register.)	3.4.2
D13	R/W	AUTOCALIBRATION [1]	0	Initiates autocalibration. Completion is available as an interrupt condition.	3.5
D14	RO	AUTOCAL PASS FLAG	1	Records the status of autocalibration; HIGH for pass, LOW for fail.	
D15	R/W	INITIALIZE [1]	0	Initializes the board when set HIGH. Sets all defaults for all registers.	3.3.2
D16	R/W	OUTPUT RANGE	0	Selects the output voltage range as: 0 => ±10V, or 0 to +10V * 1 => ±5V, or 0 to +5V * * With the Unipolar outputs option.	3.4.1.4
D17-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

[1] D02 is forced LOW and **the default value is 0000_4810h** if the Outputs-Disconnect option is not installed.

[2] Cleared automatically when operation is completed.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's.

Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI Express bus reset, and should be required only once after the initial application of power. PCI register configuration terminates with the PCI interrupts disabled. Configuration of internal local controller logic can require up to 100 milliseconds to complete.

Board configuration terminates with the local bus interrupt asserted. Attempts to access the local bus during configuration should be avoided until initialization is completed.

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked (3.3.1).
- All analog outputs are set to zero-level.
- All channels are active (3.4.1.1).
- Data coding format is offset binary (3.4.1.3.2).
- The highest available output range is selected (3.4.1.4).
- The analog output buffer is reset to empty (3.4.2.1).
- Buffer configuration is open (3.4.2.1.1).
- Internal clocking and burst triggering is selected (3.4.3.1, 3.4.4.2.1).
- The clocking Rate-A generator is adjusted to 256KSPS, and is disabled (3.4.3.1.2).
- The burst-trigger Rate-B generator is adjusted to 1 kHz, and is disabled (3.4.4.2.1).
- Sampling mode is continuous (3.4.4.1).
- The local interrupt request is asserted (3.6).
- Remote ground sensing is disabled (3.7).
- Outputs are disconnected from the I/O connector, if this option is installed (3.4.1.5).

Upon completion of initialization, the INITIALIZE control bit in the BCR is cleared automatically.

3.4 Analog Output Control

This section describes those operations that control the movement of data from the control bus through the analog output buffer. These functions include the selection of active channels, the organization of data within the buffer, and the clocking of data from the buffer to the analog outputs. The principal parameters associated with controlling the analog output channels are summarized below in Table 3.4-1. Section 3.8 provides detailed examples of analog output operations.

Table 3.4-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Active Channels; **Channel Group**	A single set of all active output channels constitutes an ***Active Channel Group***. Active channels are selected under a channel mask.
	Data Frame	All data values in the buffer comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator, at a rate determined by the sample rate control register.
Clocking Mode	Simultaneous	At each clock occurrence, the next channel group (i.e.: a single group of all active channel values) in the output buffer is transferred to the respective analog output channels. All outputs are updated simultaneously.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

3.4.1 Data Organization

3.4.1.1 Active Channels

Analog output data values are loaded into the output buffer in discrete groups or frames, of channel data. An active ***channel group*** consists of a single set of output values for all active channels. A ***data frame*** consists of a contiguous set of channel groups that are related by common channel numbers, and which collectively represent a ***single function***.

Only active output channels receive data from the output buffer. An inactive channel retains the last value that was received by the channel. During initialization, all channels are set to zero output level.

3.4.1.1.1 Selection

Each data value loaded into the buffer is accompanied by the associated channel number, and the channel number identifies that channel as ***active***. All channels not specifically represented in the buffer are ***inactive***.

3.4.1.1.2 Loading

Channel data values are loaded into the output buffer in ascending order of active channels. Channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Each data value is accompanied by the associated channel number.

Table 3.4-2 illustrates a loading example that represents three active channels with 100 values per channel. Each channel group consists of active channels 3, 9 and 60. A 'LAST CHANNEL TAG is appended to each Channel-60 value, and an END-OF-FRAME (EOF) tag is appended as well to the last Channel-60 data value.

Channels must be loaded in ascending order, beginning with the lowest-numbered channel and proceeding to the highest-numbered channel.

NOTE: ***The LAST CHANNEL TAG control bit causes the data values for all channels in the associated data group to be sent serially to their respective output registers. A subsequent output clock then transfers all of these data values simultaneously to the output DACs.***

The EOF tag indicates 'End of Function' in function-concatenation operations, or 'End of Burst' for triggered bursts.

Table 3.4-2. Typical Buffer Loading Sequence

Loading Sequence	Value Loaded		Last Chan Tag	EOF Tag	
0 (First)	Chan-3	1st value			1st Channel Group
1	Chan-9				
2	Chan-60		✓		
3	Chan-3	2nd value			2nd Group
4	Chan-9				
5	Chan-60		✓		
(Intermediate Values)					
297	Chan-3	Last value			Last Group
298	Chan-9				
299	Chan-60		✓	✓	

Channels 3, 9, and 60 Active; 100 Values per Channel

3.4.1.2 Data Frame

A *data frame* consists of an integral number of contiguous channel groups.

For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated as the *end-of-frame* (EOF). The EOF designation is applied by setting the EOF tag (D23) HIGH when loading the last channel value into the buffer. Thereafter, the EOF tag follows the last channel value through the buffer. *(The EOF tag is equivalent to an 'End of Function' tag.)*

3.4.1.3 Output Data

3.4.1.3.1 Data Format

Analog output data values are written in word-serial sequence from the control bus to the Data Buffer register shown in Table 3.4-3. Bits D00-D15 represent the output data value, and bits D24-D29 represent the associated channel number. D30 is set HIGH to indicate the last channel in a data group, while D31 is the end-of-frame (EOF) tag (equivalent to 'End-of-Function' tag). ***Bits D16-D23 must be written as all-zero***. Access to the output buffer is supported for both single-longword transfers and single-address multiple-longword DMA transfers. This write-only register reads back all-zero.

Table 3.4-3. Output Data Buffer

Offset: 0018h **Default: N/A (Write-Only)**

Bit	Mode	Designation	Description
D00	WO	DATA 00	Least significant data bit
D01-D14	WO	DATA 01 - DATA 14	Intermediate data bits
D15	WO	DATA 15	Most significant data bit
D16-D23	WO	---	***Always write as All-Zero.***
D24-D29	WO	CHANNEL IDENT	Channel number; 00-3Fh
D30	WO	LAST CHANNEL TAG	Last-channel tag (End of group)
D31	WO	EOF TAG	End-of-frame (EOF) tag

3.4.1.3.2 Data Coding

Analog output data can be coded either in 16-bit offset binary format (Table 3.4-4) by asserting the OFFSET BINARY control bit HIGH in the BCR, or in two's complement format by clearing the control bit LOW. Analog output data transactions are D32 (32 bits), but the data significance is 16 bits.

Table 3.4-4. Output Data Coding; D15..D00

	Digital Value (Hex)	
Analog Output Level	**Offset Binary**	**Two-s Complement**
Positive Full Scale minus 1 LSB	XXXX FFFF	XXXX 7FFF
Zero plus 1 LSB	XXXX 8001	XXXX 0001
Zero	XXXX 8000	XXXX 0000
Zero minus 1 LSB	XXXX 7FFF	XXXX FFFF
Negative Full Scale plus 1 LSB	XXXX 0001	XXXX 8001
Negative Full Scale	XXXX 0000	XXXX 8000

Positive Full Scale is a positive level that equals the range option defined for the board (e.g.: +10.000 Volts for the unipolar 0 to +10V range). *Negative Full Scale* is the most negative value available for the selected range (zero-Volts for the 0 to +10V range). *Full-scale Range* (FSR*)* is the total voltage range for the output channel . One LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the 0 to +10V unipolar range).

3.4.1.4 Voltage Range Selection

If the bipolar range option is installed, the output voltage range for all channels is selected as ±10V by clearing the OUTPUT RANGE control bit LOW in the BCR, or as ±5V by setting the bit HIGH.

If the unipolar range option is installed, the output voltage range for all channels is selected as 0 to +10V by clearing the OUTPUT RANGE control bit LOW in the BCR, or as 0 to +5V by setting the bit HIGH.

NOTE: For maximum accuracy, autocalibration should always be performed after a new output range is selected.

3.4.1.5 Outputs Disconnect

For boards equipped with the Outputs Disconnect option, setting the DISCONNECT OUTPUTS control bit HIGH in the BCR disconnects all outputs from the system I/O connector. *This bit is forced LOW and ignored if the disconnect-option is not installed.*

NOTE: The DISCONNECT OUTPUTS control bit defaults HIGH in order to avoid multiple output conflicts when implementing multiple-board redundancy, and is forced LOW if the Outputs-Disconnect option is not installed. If the outputs-disconnect feature is installed, the outputs are disconnected during autocalibraton (3.5).

3.4.2 Data Buffer

The output buffer consists of a 24-bit wide FIFO that has a capacity of 256K output values. Each output value is 16 bits wide and occupies a single location within the FIFO. Data values are transferred from the control bus to the analog output channels through the output buffer.

Table 3.4-5. Buffer Operations Register

Offset: 000Ch **Default: 0000_1400h**

Bit	Mode	Designation	Def	Description	Ref
D00	R/W	EXTERNAL CLOCK	0	Selects external clock when HIGH, or the internal Rate-A generator when LOW. Default is LOW (internal rate generator).	3.4.3.1
D01	R/W	EXTERNAL TRIGGER	0	Selects external trigger when HIGH, or the internal Rate-B generator when LOW. Default is LOW (internal rate generator).	3.4.4.2.1
D02	R/W	ENABLE BURST	0	Selects burst-mode if HIGH, continuous-mode if LOW.	3.4.4.2
D03	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.	3.4.4.2
D04	R/W	SW BURST TRIGGER [1]	0	Software burst trigger, asserted HIGH. Active only when ENABLE BURST control bit is asserted.	3.4.4.2.1
D05	R/W	ENABLE CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.4.3
D06	RO	CLOCK READY	0	Indicates when HIGH that a hardware or software clock will be accepted. If LOW, indicates that the output is not ready to accept a clock.	3.4.3
D07	R/W	SW CLOCK [2]	0	Produces a single output clock event when asserted. Clears LOW automatically when the clock event is completed. Active at all times if Enable Clocking is HIGH.	3.4.3.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.4.2.1.2
D09	R/W	LOAD REQUEST [1]	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.4.6.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available as an interrupt condition. Defaults HIGH.	3.4.6.3
D11	R/W	CLEAR BUFFER [1]	0	Resets the buffer to empty.	3.4.2.1
D12	RO	BUFFER EMPTY	1	Data buffer status flags.	3.4.2.1
D13-D14	RO	(Reserved)	0		
D15	RO	BUFFER FULL	0		
D16	R/W	BUFFER OVERFLOW [2]	0	Set HIGH when data is written to a full buffer.	
D17	R/W	FRAME OVERFLOW [2]	0	Set HIGH when data is written to a closed buffer.	
D18-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

[1] Clears LOW automatically when operation is completed.

[2] Remains HIGH until cleared by a direct write as LOW, or by initialization.

3.4.2.1 Buffer Control

The Buffered Output Operations register (Table 3.4-5) controls and monitors the flow of data through the analog output data buffer. Asserting the CLEAR BUFFER control bit HIGH clears, or empties, the buffer.

The BUFFER OVERFLOW flag is set HIGH if data is written to a full buffer, and the FRAME OVERFLOW flag indicates that an attempt was made to write data to a closed buffer. Both flags indicate data loss. Each of these flags, once set, remains HIGH until written LOW directly from the bus, or by initialization .

The BUFFER EMPTY flag indicates that the buffer contains no output data. The BUFFER FULL flag is asserted when the buffer is full. Data written to a full output buffer is discarded.

The Output Buffer Size register shown in Table 3.4-6 contains the number of output data values present in the buffer, and is updated continuously.

Table 3.4-6. Output Buffer Size Register

Offset: 001Ch **Default: 0000 0000h**

Bit	Mode	Designation	Def	Description
D00-D18	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D19-D31	RO	(Inactive)	0	---

The Buffer Threshold register (Table 3.4-7) specifies the buffer size value above which the BUFFER THRESHOLD FLAG is asserted HIGH. This status flag is duplicated in the Buffered Operations register, and is supported by two interrupt events (Table 3.6-1).

Table 3.4-7. Buffer Threshold Register

Offset: 0020h **Default: 0003 FFFEh**

Bit	Mode	Designation	Def	Description
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	(Reserved)	0	---
D20	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold. Duplicated in the BCR.
D21	RW	(Reserved)	0	Diagnostic control bit. Always write LOW.
D22-D31	RO	(Reserved)	0	---

NOTE: Internal buffer read-access slows considerably if the buffer is 'almost empty', where 'almost empty' is defined as the buffer containing seven or fewer samples. Consequently, In the almost-empty condition, the maximum output clocking rate is reduced to approximately 70KSPS.

3.4.2.1.1 Open Buffer

Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing and will empty itself unless it is replenished from the bus. This mode of operation permits the continuous flow of data from the control bus to the analog outputs. A full buffer will discard additional data from the bus, while an empty buffer indicates that the outputs are idle.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.4-1 illustrates the movement of a single data frame through an open buffer.

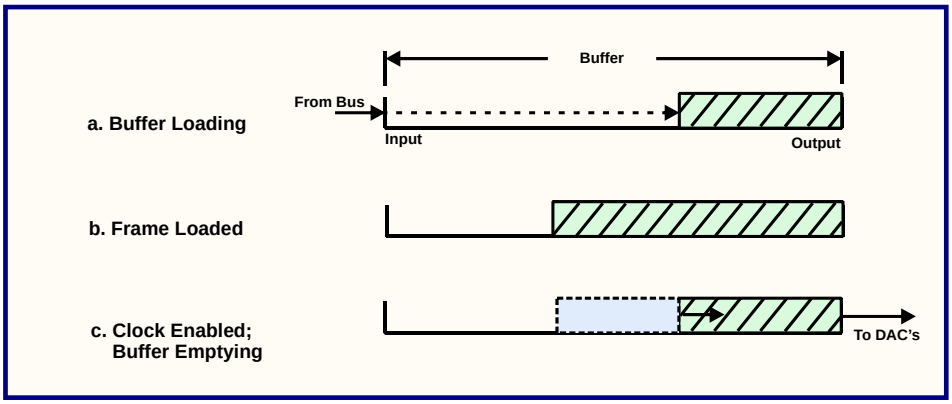

Figure 3.4-1. Open Buffer Data Flow

3.4.2.1.2 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the bus.

In Figure 3.4-2, a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

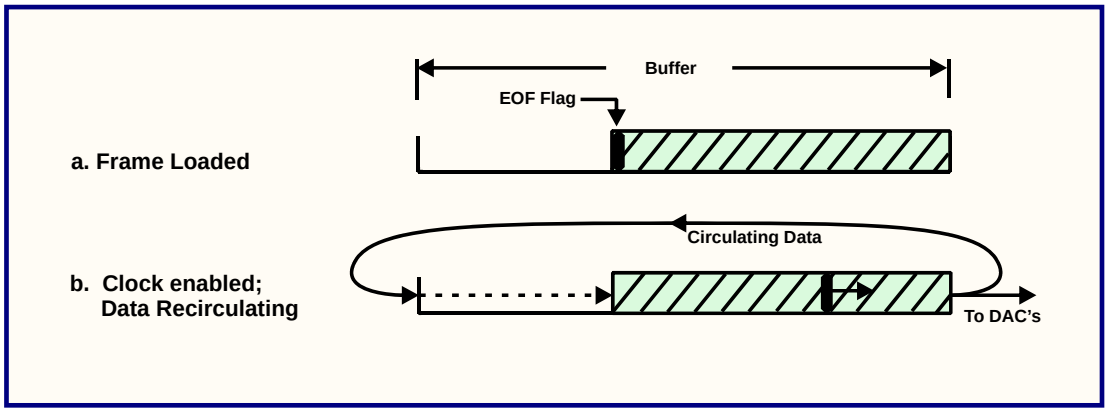

Figure 3.4-2. Circular Buffer Data Flow

An end-of-frame (EOF) flag accompanies the end-point, or last value in a data frame. The EOF flag is D23 in the buffer, and is set HIGH when the last value in a data frame is loaded. This flag is used during a triggered burst to define the last value in the burst. Multiple contiguous burst functions can reside in the buffer simultaneously.

3.4.3 Output Clocking

When the ENABLE CLOCKING control bit in the buffer operations register is asserted HIGH, clocking of the outputs is enabled, and the outputs will update at each occurrence of the selected output clock. Output clocking is disabled when the ENABLE CLOCKING control bit is LOW. The CLOCK READY status flag in the Buffer Operations register is HIGH when the board is ready to accept a clock.

3.4.3.1 Clock Source

The source of the output clock is determined by the EXTERNAL CLOCK control bit in the Buffer Operations register. When this bit is LOW, the clock source is the internal Rate-A generator.

A single software clock can be generated at any time, regardless of the states of the CLOCK INITIATOR in the BCR and the EXTERNAL CLOCK control bit in the Buffer Operations register (BOR), by setting the SW CLOCK control bit HIGH. The SW CLOCK bit clears automatically.

3.4.3.1.1 Clocking Initiators and Targets

When the CLOCK INITIATOR control bit is HIGH in the BCR, the board becomes a ***clock initiator***, and the CLK I/O pin generates an output pulse simultaneously with each internally generated output clock. This output pulse can be used for clocking outputs simultaneously on clock target boards. If CLOCK INITIATOR is LOW, the board is a ***clock target***, and the output clock can be obtained as an input through the CLK I/O pin in the system I/O connector by setting the EXTERNAL CLOCK control bit HIGH in the BOR. External clock inputs are detected on the HIGH-to-LOW logic transition.

3.4.3.1.2 Internal Rate-A, Rate-B Generators

The internal Rate-A generator provides an output clock that is adjustable by the 24-bit NRATE control field in the Rate-A Generator control register (Table 3.4-8). **The Rate-A generator is inactive unless the ENABLE RATE-A control bit is set HIGH in the BCR.**

Table 3.4-8. Rate-A, Rate-B Generator Control Registers

Rate-A: Offset: 0024h **Default: 0000_00C0h**
Rate-B: Offset: 0028h **Default: 0000_C000h**

Data Bit	Mode	Designation	Description
D00-D23	R/W	NRATE	Rate Generator divisor.
D24-D31	RO	(Reserved)	Inactive. Returns all-zero.

The output clocking, or sampling, rate **Fsamp** is calculated from the relationship:

Fsamp (Hz) = Fclk / Nrate ,

where **Fclk** is the frequency of the board's master clock frequency (Table 3.10-1), and **Nrate** is the decimal equivalent of NRATE_A. Table 3.4-9 illustrates the effect of **Nrate** on the output clock rate using the standard value of 49.152MHz for **Fclk**. Clocking rates above **510 KSPS** can produce unpredictable results and are not recommended. Each rate generator remains inactive until the associated ENABLE RATE-A, RATE-B control bit is asserted HIGH in the BCR.

Table 3.4-9. Rate Generator Rate Selection Examples

Nrate		Clocking Rate Fsamp *
(Dec)	**(Hex)**	(Sample clocks per Second)
98	00_0062	501,551
99	00_0063	496,485
---	---	Fsamp (Hz) = 49,152,000 / Nrate
49152	00_C000	1,000
16777215	FF_FFFF	2.93

* ±0.015 percent.

NOTE: Internal buffer read-access slows considerably if the buffer is 'almost empty', where 'almost empty' is defined as the buffer containing seven or fewer samples. Consequently, with the buffer in the almost-empty condition, the maximum output clocking rate is reduced to approximately 70KSPS.

3.4.3.2 Simultaneous Clocking

The 16AO64C implements *Simultaneous Clocking,* which is characterized by having all active output channels update simultaneously in response to each output clock. Consequently, all analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the sampling clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective sample rate for each channel equals the sample rate **Fsamp**. The EOF bit defines the last channel in a simultaneous group.

3.4.3.3 Sequential Clocking Emulation

Sequential clocking is emulated by setting the LAST CHANNEL TAG bit HIGH for each value in the buffer. At each clock occurrence then, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately. Channel values are read from the buffer beginning with the lowest-numbered active channel in a channel group, and proceeding upward through the highest-numbered active channel. When operating in this mode, the effective sample rate for each channel equals the output clocking rate *divided by the number of active channels*.

3.4.4 Sampling Mode

3.4.4.1 Continuous Sampling

When the *continuous sampling* mode is selected, data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that a sample clock is present. In order for a sample clock to be present, the ENABLE CLOCKING control bit in the Buffer Operations control register must be HIGH. Continuous sampling is selected when the ENABLE BURST control bit in the Buffer Operations register (BOR) is LOW.

3.4.4.2 Data Bursts

During a *triggered burs*t, data is transferred continuously from the buffer to the analog outputs until either the ***buffer goes empty, or an end-of-frame (EOF) tag (equivalent to 'end-of-burst' tag in this context) is encountered***. In the triggered-burst sampling mode, a burst trigger initiates the transfer of data from the output buffer to the output channels. **For triggered burst operation, the ENABLE BURST control bit in the BOR must be HIGH.** The BURST READY status flag in the BOR is HIGH when the board is ready to accept a burst trigger.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used. The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

3.4.4.2.1 Trigger Source

The source of the output clock is determined by the EXTERNAL TRIGGER control bit in the Buffer Operations register. When this bit is LOW, the trigger source is the internal Rate-B generator. The Rate-B generator is controlled by the **NRATE** divisor field in the Rate-B Generator control register (Table 3.4-8) **and the ENABLE RATE-B control bit in the BCR**.

A single software trigger can be generated at any time, regardless of the states of the TRIGGER INITIATOR bit in the BCR and the EXTERNAL TRIGGER control bit, by setting the SW BURST TRIGGER control bit HIGH in the BOR. The SW BURST TRIGGER bit clears automatically.

3.4.4.2.2 Burst Sync Initiators and Targets

When the TRIGGER INITIATOR control bit is HIGH in the BCR, the board becomes a ***trigger initiator***, and the TRIG I/O pin generates an output pulse at the internal initiation of each burst. This output pulse can be used for initiating simultaneous bursts on sync target boards. If TRIGGER INITIATOR is LOW, the board is a ***trigger target***, and the burst trigger can be obtained as an input through the TRIG I/O pin in the system I/O connector by setting the EXTERNAL TRIGGER control bit HIGH in the BOR. External trigger inputs are detected on the HIGH-to-LOW logic transition.

NOTE: Clock and trigger sources can be selected independently. For example, a board can be both a *clock initiator* and a *trigger target* simultaneously.

3.4.5 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal.

The maximum number of boards that can be synchronized directly, without additional external drivers, depends upon both static loading and cable characteristics, and can vary from four to as many as eight.

3.4.5.1 Synchronous Clocking

To ***clock-synchronize*** multiple boards together, the CLK I/O from one board, designated the *clock-initiator*, is connected to the CLK I/O pins of one or *more clock-target* boards. In this case, the clock-targets are configured for external clocking.

If the external clock source is not a PCIe-16AO64C board, then all boards would be configured as clock targets.

3.4.5.2 Synchronous Bursts

To ***burst-synchronize*** a group of boards, the TRIG I/O pin on one board, designated the *burst-initiator*, is connected to the TRIG I/O pins of a group *of burst-target* boards. Each burst-target, when operated in the triggered-burst mode, initiates a single burst from its buffer each time the burst-initiator initiates a burst.

If the external trigger source is not a PCIe-16AO64C board, then all boards would be configured as trigger targets.

3.4.6 Function Generation

3.4.6.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous sampling and circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly. Clocking is enabled when the ENABLE CLOCKING control bit in the buffer operations register is HIGH.

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform is retained in the buffer and can be reproduced repeatedly by subsequent triggers.

3.4.6.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions will be flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions will be retained in the buffer, and the series of functions will be repeated indefinitely.

3.4.6.3 Function Sequencing (Concatenation)

A new function (data frame) can be concatenated to the end of an existing function in a circular buffer, while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output.

The introduction of the new function commences by setting the LOAD REQUEST flag HIGH in the buffer operations register, and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame. Assertion of LOAD READY is selectable as an interrupt event (Section 3.6).

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag (data bit D16 set HIGH). The EOF flag of the existing function causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. **Notice that the loading of the new function into the buffer must be completed before the existing function terminates.** The HIGH-to-LOW transition of LOAD READY also is selectable as an interrupt event.

In Figure 3.4-3, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

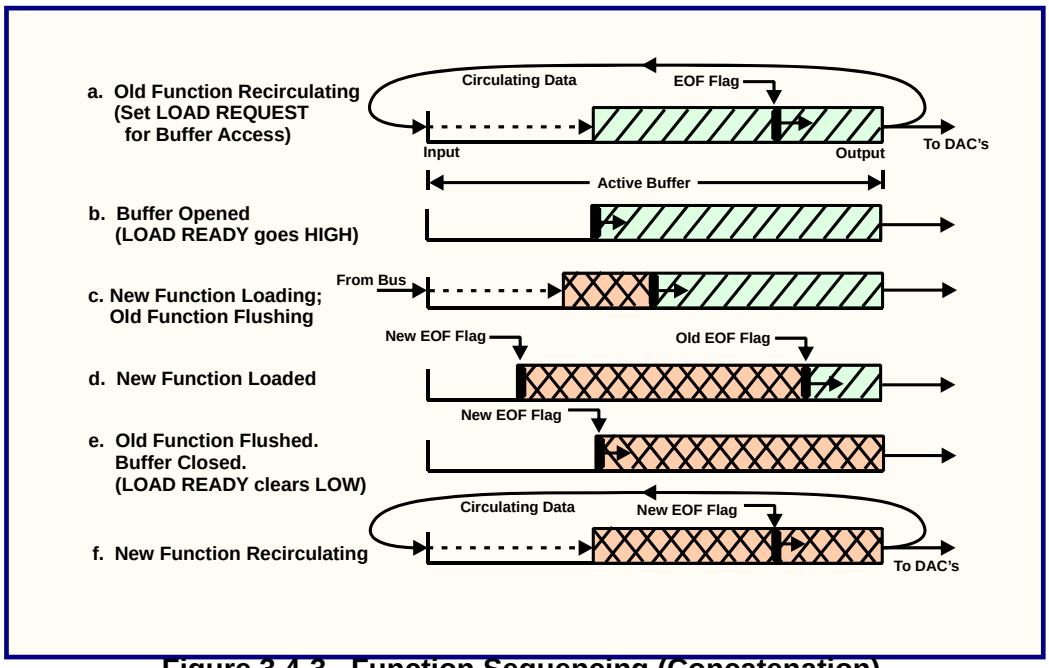

Figure 3.4-3. Function Sequencing (Concatenation)

NOTE: If the loading of a new function extends beyond the LOAD-READY interval, the FRAME OVERFLOW flag is set HIGH in the Buffer Operations register, indicating data loss. Once set, this flag remains HIGH until written LOW directly from the bus, or by initialization.

3.5 Autocalibration

Autocalibration is invoked setting by the AUTOCALIBRATION control bit HIGH in the BCR. The control bit returns LOW when the calibration of all output channels is completed.

Autocalibration has a maximum duration of approximately 15 seconds. Completion of the operation can be detected either by polling the AUTOCALIBRATION control bit for a zero-state, or by selecting the 'Autocalibration completed' interrupt event (Section 3.6) and waiting for the interrupt request. Write-accesses from the PCI bus should be avoided during autocalibration, and the board should be initialized after autocalibration is completed.

NOTE: For boards not equipped with the outputs-disconnect feature (3.4.1.5), the analog outputs are active during autocalibration, and fluctuate between zero-level and positive fullscale. If the outputs-disconnect feature is installed, the outputs are disconnected during autocalibraton.

All outputs assume zero-levels upon autocal completion.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs immediately after power is applied.

*Calibration correction values are retained until a power-up reset occurs or until autocalibration is repeated, and c*orrection values are retained during a software initialization (3.3.2). If a board is defective, the autocalibration process may be unable to successfully calibrate all output channels. If this situation occurs, the AUTOCAL PASS FLAG bit in the BCR will be cleared LOW at the end of the autocalibration interval, and will remain LOW until a subsequent initialization or autocalibration occurs. The AUTOCAL PASS FLAG remains HIGH unless an autocalibration failure occurs.

NOTE: To ensure maximum output accuracy, autocalibration should be performed when a new output range is selected.

3.6 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI Express interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.6.2.

3.6.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The source condition for the request is selected as shown in Table 3.6-1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until either (a) the control bus clears the BCR request flag, or (b) the associated interrupt condition is deasserted. A local interrupt request is generated automatically at the end of initialization.

Table 3.6-1. Interrupt Event Selection

BCR Bits D08-D10 **Default: 0000_0000h**

Interrupt	Interrupt Event
0	Idle. Interrupt disabled unless initializing. Default state.
1	Autocalibration completed
2	Output buffer empty
3	Buffer threshold flag Low-to-High transition
4	Buffer threshold flag High-to-Low transition
5	Burst Trigger Ready
6	Load Ready (LOW-to-HIGH transition)
7	End Load Ready (HIGH-to-LOW transition of Load Ready)

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.6.2 Enabling the PCI Express Interrupt

A local interrupt request will not produce an interrupt on the PCI Express bus unless the PCI Express interrupt is enabled. Refer to the PEX-8311 reference manual for information pertaining to the handling of interrupts.

3.7 Remote Ground Sensing

Remote ground sensing for single-ended outputs is enabled when the REMOTE GROUND SENSE control bit in the BCR is HIGH, and is disabled when the control bit is LOW. Unless specific wiring provisions have been made to implement remote sensing, the remote sense control bit should be left in the default (LOW) disabled state.

NOTE: Differences between ground potentials do not significantly affect the integrity of differential signals, and introducing a ground-sense correction signal can actually degrade accuracy. For this reason, remote ground sensing is disabled for differential outputs.

3.8 Application Examples

Specific operating modes and procedures vary widely according to the unique requirements of each application. The examples presented in this section illustrate basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally apply to a single output channel for simplicity of explanation. However, each active channel represents an independent set of function values, and all channels share a common output clock.

Table 3.8-1. Summary of Operation Examples

Operation Example	Description
Simultaneous Outputs	Data values accumulate in the output data buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously when clocked.
Continuous Function	An extension of Simultaneous Outputs, in which the buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.8-2 have already been performed.

Table 3.8-2. Initial Operations

Operation	Default Value
The board has been reset or initialized.	---
The active channel group has been defined .	All channels active
The required output coding has been selected.	Offset binary

The remaining operational parameters are assumed to be in the following *default* states initially:

Parameter	Default
Buffer mode:	Open
Buffer status:	Empty
Clocking rate:	96KSPS
Clocking mode:	Sequential

Parameter	Default
Clock source:	Rate-A Generator
Clock status:	Disabled
Trigger source:	Rate-B Generator
Trigger status:	Disabled

3.8-1 Simultaneous Direct (Single Group) Outputs

Table 3.8-3. Simultaneous Outputs Example (Single Group)

Operation	PCI Bus Action	Board Response
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-A control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Clear the output buffer.	Set the CLEAR BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the output value for the first active channel.	Write the first value to the output data buffer.	First active value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active values are accumulated in the buffer. When the last active value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

3.8-2 Continuous Function

Table 3.8-4. Continuous Function Example

Operation	PCI Bus Action	Board Response
Set the buffer threshold flag to 1/4 of the expected block size.	Write 1/4 block size to the threshold register.	The threshold flag will go LOW when the buffer contents drop below the threshold.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Enable clocking	Set the ENABLE CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-A control bit HIGH in the BCR.	Clocking is enabled at the selected rate. The internal rate generator is enabled, if internal clocking is required.
Clear the output buffer.	Set the CLEAR BUFFER bit in the output operations register.	The output buffer clears to empty.
Write a block of values to all active channels. To avoid discontinuities in the output functions, the effective loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 50MSPS during DMA transfers.	Write function values for all active channels to the output data buffer.	All active channels produce their respective output functions.
Wait for the buffer threshold flag to go LOW. (See Note 1).	Monitor the analog output buffer threshold flag until LOW.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:
1. Response to the threshold flag must be fast enough to prevent the buffer from going empty.

3.8.3 Periodic Function

Table 3.8-5. Periodic Function Example

Operation	PCI Bus Action	Board Response
Clear the output buffer.	Set the CLEAR BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. (Note 1)	Write all function values for all active channels to the output buffer.	Function values for all active channels accumulate in the buffer.
Set the end-of-frame (EOF) flag.	Set the EOF flag HIGH when writing the data value for the last channel in the last group.	The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Select the circular buffer mode.	Set CIRCULAR BUFFER in the buffer operations register.	The output buffer is closed (circular).
Enable the output clock.	Set ENABLE CLOCKING in the buffer operations register. Set the ENABLE RATE-A GENERATOR control bit HIGH in the BCR.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:

1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.8.4 Function Burst

Table 3.8-6. Function Burst Example

Operation	PCI Bus Action	Board Response
Clear the output buffer.	Set the CLEAR BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the function values for all active channels. Set the end-of-frame (EOF) flag.	Write all function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	Function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
Select the clocking rate.	Write the required sample clocking rate to the Rate-A generator control register.	The output clocking rate is selected.
Select the triggering rate.	Write the required triggering rate to the Rate-B generator control register.	The burst triggering rate is selected.
Select triggered-burst mode.	Set ENABLE OUTPUT BURST in the buffer operations register.	The triggered-burst operating mode is selected.
Prepare the buffer operations register for burst mode:	Write to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
Enable the output clock.	Set ENABLE CLOCKING	Output clocking is enabled.
Enable the internal rate generators.	Set the ENABLE RATE-A and RATE-B control bits in the BCR.	Required internal rate generators are enabled.
For external burst triggering, or internal rate-generator triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each trigger.

3.8.5 Function Sequencing (Concatenation)

Table 3.8-7. Function Sequencing (Concatenation) Example

Operation	PCI Bus Action	Board Response
Establish the generation of a periodic function. The following operations will replace the original ('old') function in each channel with a 'new' function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request buffer access	Set LOAD REQUEST in the buffer operations register.	The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Monitor the LOAD READY status flag. The buffer is open when this flag goes HIGH.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode when the EOF flag for the old function is detected, indicating that the last data value in the original function set has left the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes.

3.9 Buffer DMA Operation

DMA transfers to the analog output FIFO buffer are supported in either **block-mode** or **demand-mode**, with the board operating as bus master. Demand mode operation requires the ***slow terminate*** mode. Refer to the PEX-8311 reference manual for a detailed description of the associated DMA configuration registers.

3.10 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.10-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.10-1. Assembly Configuration Register

Offset: 0010h **Default: 00XX XXXXh**

Bit Field	Description
D00-D15	Firmware Revision
D16-D17	Number of output channels: 0 => 64 Single-ended output channels 1 => 32 Single-ended output channels 2 => 32 Differential output channels 3 => 16 Differential output channels.
D18-D19	Output Scale: 0 => Unipolar: 0 to +10V and 0 to +5V 1 => Bipolar: ±10V and ±5V 2 => (Reserved) 3 => (Reserved).
D20-D21	Output Filters: 0 => 100kHz 1 => 10kHz 2 => No filter (>200kHz) 3 => (Reserved).
D22-D23	Master Clock Frequency: 0 => 49.152MHz (Standard) 1-3 => (Reserved).
D24	Outputs-Disconnect Feature: Low (0) => No outputs-disconnect. High (1) => Feature installed.
D25-D26	(Reserved bit field; returns all-zero)

3.11 Clock and Trigger I/O Configurations

Tables 3.11-1 and 3.11-2 summarize the behavior of the output clock and burst trigger under control of the initiator control bits in the BCR and the source control bits (External Clock/Trigger) in the BOR.

Table 3.11-1. Clocking I/O configurations

External Clock BOR: D00	Clock Initiator BCR: D00	CLK IO Pin; System I/O Connector	Output Clock to DACs
0	0	Input (Ignored)	Rate-A Gen
0	1	Output; Rate-A Gen	Rate-A Gen
1	0	Input	CLK IO input Pin
1	1	Invalid (Recursive)	

Table 3.11-2. Triggering I/O configurations

External Trigger BOR: D01	Trigger Initiator BCR: D01	TRIG IO Pin; System I/O Connector	Burst Trigger
0	0	Input (Ignored)	Rate-B Gen
0	1	Output; Rate-B Gen	Rate-B Gen
1	0	Input	TRIG IO input Pin
1	1	Invalid (Recursive)	

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PCIe-16AO64C contains 64 D/A converters (16-Bit DAC's), and all supporting functions necessary for adding precision high-speed analog output capability to a PCI Express application. As Figure 4.1-1 illustrates, a PCI Express interface adapter provides the interface between the controlling PCI Express bus and an internal local controller. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

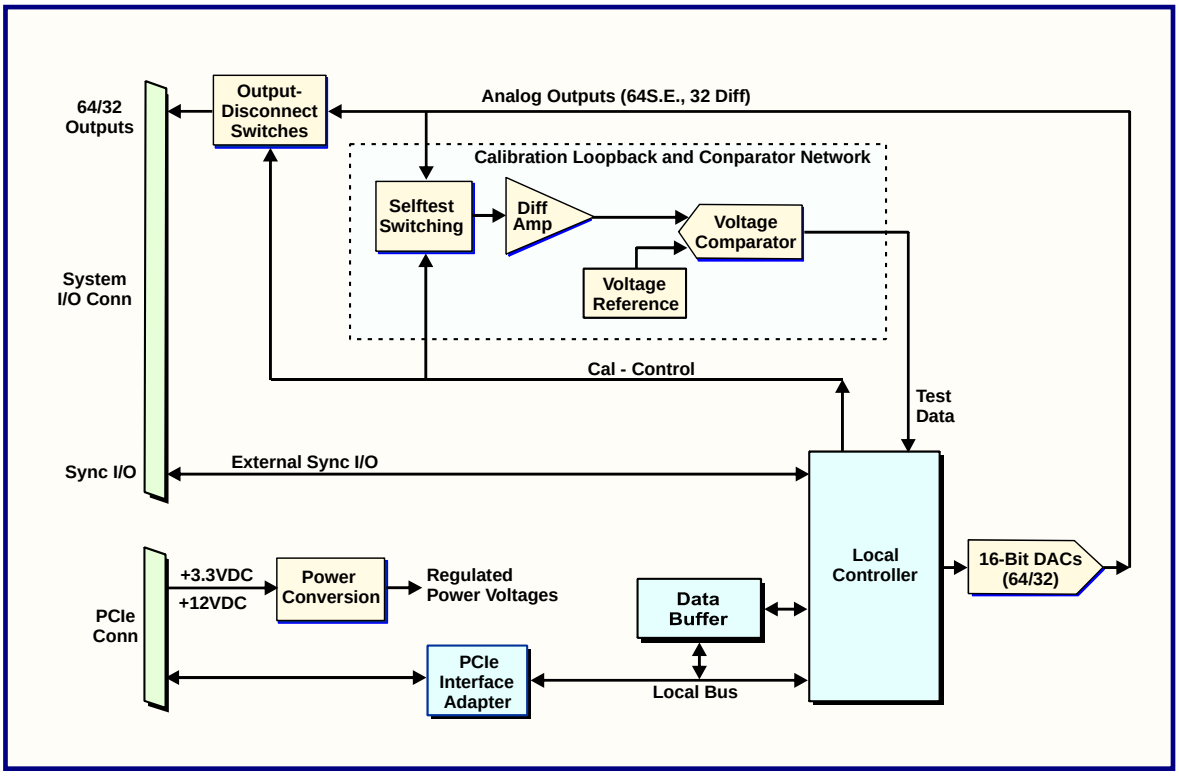

Figure 4.1-1. Functional Block Diagram

During normal operation, analog output data values are written from the PCI Express bus to the output buffer. The data values subsequently are serialized and transferred to the respective analog output DAC's. Remote sensing of remote ground potentials is software selectable and affects all outputs simultaneously.

External control inputs and outputs accept burst-trigger and sample-clock inputs, and provide the digital signals necessary for multiboard synchronization.

Selftest networks allow the controller to compare the analog levels from all output channels against the internal voltage reference, and are used to establish the internal connections necessary during autocalibration. All channels are calibrated with respect to a single precision voltage reference, which is available for verification at a board-edge test connector.

Offset and gain corrections for each output channel are determined during on-demand autocalibration, and are used to cancel offset and gain errors in the channel. Autocalibration provides the adjustment functions that otherwise would be associated with 128 manual trimmers in conventional analog configurations. Calibration control values are determined and stored in internal memory during autocalibration, and are applied in real-time during operation. The calibration values are retained until the PCI bus is reset or autocalibration is executed again.

4.2 Analog Outputs

Each of the 64 analog output channels consists of a 16-bit output DAC and an output buffer amplifier. The local controller reads the 16-bit channel data value for each channel from the analog output buffer, and sends the value serially to the associated output DAC. The output DAC deserializes the data to obtain the original 16-bit data word, and holds that word in an internal buffer until commanded to transfer the data to the output register that drives the DAC output.

All active output channels are updated simultaneously. An optional outputs-disconnect feature permits the outputs to be disconnected from the system I/O connector under software control.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The calibration algorithm drives the output of each channel under calibration alternately to ground and to 99-percent of fullscale, and successively iterates the value of a 16-Bit gain (or offset) correction value to match the reference or ground voltage. A high-gain loopback voltage comparator provides a one/zero test output in response to the output channel under test.

The gain and offset corrections for each channel are adjusted in a series of second-level fullscale/offset adjustment iterations, in which each iteration reduces the adjustment error in a convergent sequence. Each iteration adjusts the gain first, and then the offset. In the first iteration for each channel, the gain adjustment is performed with the offset caldac adjusted to midrange.

The final value for each gain and offset Calibration DAC is stored in volatile calibration memory, as well as in the DAC itself, and is retained until a system reset occurs or until autocalibration is executed again.

4.4 Power Control

Well-regulated and noise-free supply voltages of +5 Volts and ±14 Volts are required by the analog networks, and are derived from the PCI Express Bus +12-Volt and 3.3-Volt inputs through a DC/DC converter. To obtain optimum regulation and minimum noise from the internal supplies, all analog power voltages employ linear postregulation.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers and principal control-bit fields that appear in Section 3.

Table 3.1-1. Control and Data Registers

Offset (Hex)	Register	Mode*	Default	Primary Function	Ref
00	BOARD CONTROL (BCR)	R/W	0000_4814h	Board Control Register (BCR)	3.2
04-08	(Reserved)	RO	0000_0000h	---	---
0C	BUFFER OPERATIONS	R/W	0000_1400h	Buffer control and status flags	3.4.2.1
10	ASSEMBLY CONFIGURATION	RO	00XX_XXXXh	Firmware revision and hardware options	3.10
14	Autocal Values **	R/W	0000_0XXXh	---	---
18	OUTPUT DATA BUFFER	WO	0000_0000h	Analog output FIFO buffer	3.4.2
1C	BUFFER SIZE	RO	0000_0000h	Number of data values in the buffer.	3.4.2.1
20	BUFFER THRESHOLD	R/W	0003_FFFEh	Buffer status-flag threshold value	3.4.2.1
24	RATE-A GENERATOR	R/W	0000_00C0h	Divisor for the Rate-A generator	3.4.3.1.2
28	RATE-B GENERATOR	R/W	0000_C000h	Divisor for the Rate-B generator	3.4.4.2.1
2C-3F	(Reserved)	RO	0000_0000h	---	---

* R/W = Read/Write; RO = Read-only; WO = Write-only . ** Maintenance register; shown for reference.

Table 3.2-1. Board Control Register

Offset: 0000h **Default: 0000_ 4814h [1]**

Bit	Mode	Designation	Def	Description	Ref
D00	R/W	CLOCK INITIATOR	0	Configures the CLK I/O pin as an output when HIGH.	3.4.3.1
D01	R/W	TRIGGER INITIATOR	0	Configures the TRIG I/O pin as an output when HIGH.	3.4.4.2.1
D02	R/W	DISCONNECT OUTPUTS	1 (1)	Disconnects all outputs from the system I/O connector when HIGH. (Active only if the Outputs Disconnect option is installed).	3.4.1.5
D03	R/W	REMOTE GROUND SENSE	0	Enables the remote-ground sense feature when HIGH.	3.7
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.	3.4.1.3.2
D05	R/W	ENABLE RATE-A	0	Enables the Rate-A generator when HIGH.	3.4.3.1.2
D06	R/W	ENABLE RATE-B	0	Enables the Rate-B generator when HIGH.	3.4.3.1.2
D07	R/W	(Reserved)	0	---	---
D08-D10	R/W	INTERRUPT A0-A2	0	Interrupt event selection.	3.6
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board asserts an interrupt request. Clears the request when cleared LOW by the bus.	
D12	R/W	BUFFER THRESHOLD FLAG	0	High when the number of values in the buffer exceeds the selected threshold value. (Duplicated in the buffer threshold register.)	3.4.2
D13	R/W	AUTOCALIBRATION [1]	0	Initiates autocalibration. Completion is available as an interrupt condition.	3.5
D14	RO	AUTOCAL PASS FLAG	1	Records the status of autocalibration; HIGH for pass, LOW for fail.	
D15	R/W	INITIALIZE [1]	0	Initializes the board when set HIGH. Sets all defaults for all registers.	3.3.2
D16	R/W	OUTPUT RANGE	0	Selects the output voltage range as: 0 => ±10V, or 0 to +10V * 1 => ±5V, or 0 to +5V * * With the Unipolar outputs option.	3.4.1.4
D17-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

[1] D02 is forced LOW and **the default value is 0000_4810h** if the Outputs-Disconnect option is not installed.

[2] Cleared automatically when operation is completed.

Table 3.4-2. Typical Buffer Loading Sequence

Loading Sequence	Value Loaded		Last Chan Tag	EOF Tag	
0 (First)	Chan-3	1st value			
1	Chan-9				1st Channel Group
2	Chan-60		✓		
3	Chan-3	2nd value			
4	Chan-9				2nd Group
5	Chan-60		✓		
(Intermediate Values)					
297	Chan-3	Last value			
298	Chan-9				Last Group
299	Chan-60		✓	✓	

Channels 3, 9, and 60 Active; 100 Values per Channel

Table 3.4-3. Output Data Buffer

Offset: 0018h **Default: N/A (Write-Only)**

Bit	Mode	Designation	Description
D00	WO	DATA 00	Least significant data bit
D01-D14	WO	DATA 01 - DATA 14	Intermediate data bits
D15	WO	DATA 15	Most significant data bit
D16-D23	WO	---	***Always write as All-Zero.***
D24-D29	WO	CHANNEL IDENT	Channel number; 00-3Fh
D30	WO	LAST CHANNEL TAG	Last-channel tag (End of group)
D31	WO	EOF TAG	End-of-frame (EOF) tag

Table 3.4-4. Output Data Coding; D15..D00

	Digital Value (Hex)	
Analog Output Level	**Offset Binary**	**Two-s Complement**
Positive Full Scale minus 1 LSB	XXXX FFFF	XXXX 7FFF
Zero plus 1 LSB	XXXX 8001	XXXX 0001
Zero	XXXX 8000	XXXX 0000
Zero minus 1 LSB	XXXX 7FFF	XXXX FFFF
Negative Full Scale plus 1 LSB	XXXX 0001	XXXX 8001
Negative Full Scale	XXXX 0000	XXXX 8000

Table 3.4-5. Buffer Operations Register

Offset: 000Ch **Default: 0000_1400h**

Bit	Mode	Designation	Def	Description	Ref
D00	R/W	EXTERNAL CLOCK	0	Selects external clock when HIGH, or the internal Rate-A generator when LOW. Default is LOW (internal rate generator).	3.4.3.1
D01	R/W	EXTERNAL TRIGGER	0	Selects external trigger when HIGH, or the internal Rate-B generator when LOW. Default is LOW (internal rate generator).	3.4.4.2.1
D02	R/W	ENABLE BURST	0	Selects burst-mode if HIGH, continuous-mode if LOW.	3.4.4.2
D03	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.	3.4.4.2
D04	R/W	SW BURST TRIGGER [1]	0	Software burst trigger, asserted HIGH. Active only when ENABLE BURST control bit is asserted.	3.4.4.2.1
D05	R/W	ENABLE CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.4.3
D06	RO	CLOCK READY	0	Indicates when HIGH that a hardware or software clock will be accepted. If LOW, indicates that the output is not ready to accept a clock.	3.4.3
D07	R/W	SW CLOCK [2]	0	Produces a single output clock event when asserted. Clears LOW automatically when the clock event is completed. Active at all times if Enable Clocking is HIGH.	3.4.3.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.4.2.1.2
D09	R/W	LOAD REQUEST [1]	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.4.6.3
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available as an interrupt condition. Defaults HIGH.	3.4.6.3
D11	R/W	CLEAR BUFFER [1]	0	Resets the buffer to empty.	3.4.2.1
D12	RO	BUFFER EMPTY	1	Data buffer status flags.	3.4.2.1
D13-D14	RO	(Reserved)	0		
D15	RO	BUFFER FULL	0		
D16	R/W	BUFFER OVERFLOW [2]	0	Set HIGH when data is written to a full buffer.	
D17	R/W	FRAME OVERFLOW [2]	0	Set HIGH when data is written to a closed buffer.	
D18-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

[1] Clears LOW automatically when operation is completed.

[2] Remains HIGH until cleared by a direct write as LOW, or by initialization.

Table 3.4-6. Output Buffer Size Register

Offset: 001Ch **Default: 0000 0000h**

Bit	Mode	Designation	Def	Description
D00-D18	RO	BUFFER SIZE	0 0000h	Number of values in the output buffer
D19-D31	RO	(Inactive)	0	---

Table 3.4-7. Buffer Threshold Register

Offset: 0020h **Default: 0003 FFFEh**

Bit	Mode	Designation	Def	Description
D00-D18	RW	OUTPUT BUFFER THRESHOLD	3 FFFEh	Specifies the number of values in the output buffer, above which the threshold flag is asserted HIGH.
D19	RO	(Reserved)	0	---
D20	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the output buffer *exceeds* the specified buffer threshold. Duplicated in the BCR.
D21	RW	(Reserved)	0	Diagnostic control bit. Always write LOW.
D22-D31	RO	(Reserved)	0	---

Table 3.4-8. Rate-A, Rate-B Generator Control Registers

Rate-A: Offset: 0024h **Default: 0000_00C0h**
Rate-B: Offset: 0028h **Default: 0000_C000h**

Data Bit	Mode	Designation	Description
D00-D23	R/W	NRATE	Rate Generator divisor.
D24-D31	RO	(Reserved)	Inactive. Returns all-zero.

Table 3.4-9. Rate Generator Rate Selection Examples

Nrate		Clocking Rate Fsamp *
(Dec)	(Hex)	(Sample clocks per Second)
98	00_0062	501,551
99	00_0063	496,485
---	---	Fsamp (Hz) = 49,152,000 / Nrate
49152	00_C000	1,000
16777215	FF_FFFF	2.93

* ±0.015 percent.

Table 3.6-1. Interrupt Event Selection

BCR Bits D08-D10 **Default: 0000_0000h**

Interrupt	Interrupt Event
0	Idle. Interrupt disabled unless initializing. Default state.
1	Autocalibration completed
2	Output buffer empty
3	Buffer threshold flag Low-to-High transition
4	Buffer threshold flag High-to-Low transition
5	Burst Trigger Ready
6	Load Ready (LOW-to-HIGH transition)
7	End Load Ready (HIGH-to-LOW transition of Load Ready)

Table 3.11-1. Assembly Configuration Register

Offset: 0010h **Default: 00XX XXXXh**

Bit Field	Description
D00-D15	Firmware Revision
D16-D17	Number of output channels: 0 => 64 Single-ended output channels 1 => 32 Single-ended output channels 2 => 32 Differential output channels 3 => 16 Differential output channels.
D18-D19	Output Scale: 0 => Unipolar: 0 to +10V and 0 to +5V 1 => Bipolar: ±10V and ±5V 2 => (Reserved) 3 => (Reserved).
D20-D21	Output Filters: 0 => 100kHz 1 => 10kHz 2 => No filter (>200kHz) 3 => (Reserved).
D22-D23	Master Clock Frequency: 0 => 49.152MHz (Standard) 1-3 => (Reserved).
D24	Outputs-Disconnect Feature: Low (0) => No outputs-disconnect. High (1) => Feature installed.
D25-D26	(Reserved bit field; returns all-zero)

Table 3.11-1. Clocking I/O configurations

External Clock BOR: D00	Clock Initiator BCR: D00	CLK IO Pin; System I/O Connector	Output Clock to DACs
0	0	Input (Ignored)	Rate-A Gen
0	1	Output; Rate-A Gen	Rate-A Gen
1	0	Input	CLK IO input Pin
1	1	Invalid (Recursive)	

Table 3.11-2. Triggering I/O configurations

External Trigger BOR: D01	Trigger Initiator BCR: D01	TRIG IO Pin; System I/O Connector	Burst Trigger
0	0	Input (Ignored)	Rate-B Gen
0	1	Output; Rate-B Gen	Rate-B Gen
1	0	Input	TRIG IO input Pin
1	1	Invalid (Recursive)	

APPENDIX B

MIGRATION FROM THE PMC66-16AO16

APPENDIX B

MIGRATION FROM THE PMC66-16AO16

Operation of the PCIe-16AO64C is similar to that of the PMC66-16AO16. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a comprehensive list of requirements.

B.1. Comparison of Features

Table B.1 lists the principal differences between PMC-16AO16 and PCIe-16AO64C characteristics.

Table B.1. PMC66-16AO16, PCIe-16AO64C Features Comparison

Parameter	PMC66-16AO16	PCIe-16AO64C
Form Factor	Single-Width PMC	**PCI Express short card**
Maximum Output Channels	16	**64**
Output Configuration	Balanced Differential or Single-Ended (Factory Options)	Balanced Differential or Single-Ended (Factory Options)
Output Ranges	±10V, ±5V, ±2.5V or ±1.25V	**±10V, ±5V, or optional unipolar ranges of 0 to +10V, 0 to +5V**
Output Range Selection	Software-selectable	Software-selectable
Max Clocking Rate	450KSPS	**500KSPS**
Maximum Buffer Size	256K-Samples	**256K-Samples**
Sync I/O Logic Levels	Software-selected; LVDS or TTL	**TTL**
Clocking Mode	Simultaneous or Sequential	**Simultaneous, with sequential emulation**
Control Bus	PCI: D32; 33MHz or 66MHz	**PCI Express; Single-lane**
Local Clock Frequency	45MHz	**49.152MHz**
Internal Rate Divider	18 Bits	**24 Bits**

B.2. Principal Migration Issues, from PMC66-16AO16

Paragraph 2.2 Installation:

System I/O connector is modified.

Table 3.1-1 Control and Data Registers:

Channel Selection, Sample Rate and Adjustable Clock registers are deleted.
Firmware and Options register is renamed Assembly Configuration.
Buffer Size and Buffer Threshold registers are added.
Rate-A and Rate-B Divisor registers are added.

Table 3.2-1 BCR:

Watchdog control bits D22, D23 are deleted.
Burst controls D00-02 are relocated to the Buffer Operation Register D02-04.
D05 and D06 are revised to 'Enable Rate-A/B'.
D07 is revised from 'Simultaneous Outputs' to 'Reserved'.
D12 is assigned as the Threshold Flag.
D14 polarity is reversed.
The Output Range field is reduced to a single bit D16.
D17 and D18 are revised to Enable Rate-A and Enable Rate-B.

Paragraph 3.4.2 (Channel) Selection:

Active channels are indicated by appending the channel number to each associated data value, rather than assignment under a common channel mask. This arrangement improves flexibility by allowing different channel assignments simultaneously among multiple functions.

Paragraph 3.4.1.4 Voltage Range Selection

The range-select field is reduced to a single control bit in the BCR.

Paragraph 3.4.2 Data Buffer

The active buffer is replaced with a fixed-size 256 K-Sample buffer.
New Buffer Size and Buffer Threshold registers have been added.

Paragraph 3.4.3 Output Clocking

External clocking operations are modified to eliminate possible tristate conflicts on the CLK I/O line.

Paragraph 3.4.4.2 Data Bursts

External burst triggering operations are modified to eliminate possible tristate conflicts on the TRIG I/O line.

Table 3.4-5 Buffer Operations Register:

The Buffer Size function D00-03, and flags D13-14 are deleted.
Control bits are reassigned as:

D00: Initiator
D01: External Sync
D02: Enable Burst
D03: Burst Ready
D04: SW Burst Trigger

Paragraph 3.5 Autocalibration

D14 in the BCR is now HIGH for autocal -pass, and Low for fail.

Table 3.4-6. Buffer Size Register; Table 3.4-7. Buffer Threshold Register:

New registers.

Paragraph 3.6.1. Local Interrupt Request:

Buffer High/Low Quarter flags are replaced with threshold flag events..

Paragraph 3.10-1; Table 3.10-1 Assembly Configuration Register:

Replaces deleted Paragraph 3.10. Production-option bit-fields are revised.

Developmental Revision History:

08-29-2012: Origination as preliminary draft.

09-19-2012: Figures 1.2-1, 4.1-1; Updated functional diagram.

01-19-2012: Table 2.2-1: Revised differential input channel numbering to agree with software references.
Table 3.4-7: Added control bit 'Turbo Prefetch'.
Para 3.5. Revised output states upon autocal completion.
App-B: Updated migration parameters.

11-14-2012: Figure 3.4-1: Deleted figure.
Figure 3.4-2 to 3.4-4: Renumbered with regard to deleted Figure 3.4-1.
Table 3.4-2: Inserted new Table.
Table 3.4-7: Reversed polarity of D21 (Turbo Prefetch). Categorized as 'Reserved'.
Table 3.11-1: Corrected references.

04-09-2013: Para 3.4.1.2, 3.4.2, 3.4.2.1.2, 3.5: Editorial corrections.
Para 3.11; Figures 3.11-1,2. Added new section and tables.

06-10-2013: Para 3.4.3.1.2: Removed restriction on Fclk max with more than 32 channels active.

08-17-2013: Para 3.4.1.3.1, Table 3.4-3: Revised bit sequence.

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