



4000

S E R I E S

PROTECTION RELAY
USER MANUAL

V 1.8.2

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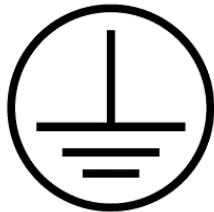
IV. WARNINGS



DANGER: High-voltage terminals. Any contact with the terminals when the device is connected could result in electric shock and cause injury or death. The device must be disconnected from high voltage before handling.



DANGER: Before disconnecting any current input, make sure that the current loop has previously been short circuited. Failure to follow this practice could result in electric shock and cause injury or death.



DANGER: Make sure you have a protective conductor connected to the screw or the terminal marked with this symbol at all times. Refer to the Installation section for more information. Failure to follow this practice could result in electric shock and cause injury or death. Make sure this conductor is connected before handling the device.

DANGER: This device is equipped with a Class 1 laser. The use of this device for purposes other than specified herein may result in hazardous radiation exposure.

V. CONTACT INFORMATION



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VI. SYMBOLS

SYMBOLS	DESCRIPTION
	Normally open dry contact
	Normally closed dry contact
	Digital input
	Analog current input
	Analog voltage input
	Direct current
	Alternative current
	Direct current and alternative current
	Protective earth terminal
	Dual inputs comparator: if input + is greater than input -, the output switches to logical state 1
	Logical AND between two inputs
	Protection elements internal timers: -T _O is the operating time -T _H is the hold time -T _R is the return time
	Dual inputs multiplexor : if S = 0, R = A; else, R = B
	Logical OR between two inputs
	Proportional step integrator

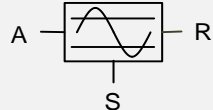
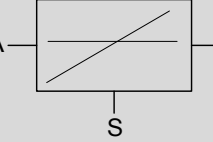
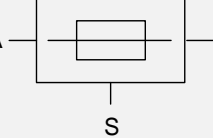

	<p>Counter: Counts the number of valid peaks in a cycle</p>
	<p>Counter : Switches to 1 if the number of consecutive events is greater than S.</p>
	<p>Sliding window: Switches to 1 if 'x' out of the last 'y' events are 1.</p>
	<p>Absolute value ($R = A$)</p>

Table 1 Symbols used in the manual

1 INTRODUCTION

This document includes instructions for the installation, commissioning and use of your new ALP-4000 series multifunction protection relay.

The relays of the ALP-4000 series are microprocessor-based systems used to protect electrical equipment by closely analyzing current and voltage signals. In addition to the protection elements, the relay includes metering, automation and reporting functions. Thus, it allows the user to protect their equipment and remotely transmit its state. The relays of the ALP-4000 series have a large storage space and a web server requiring very little setup. They are reliable devices, enhanced with their simplicity of setup and use.

2

OPERATING ENVIRONMENT

2 OPERATING ENVIRONMENT

This chapter presents the operating environment of the protection relays of the ALP-4000 series. It shows various physical setups with the electrical equipment to protect, as well as the setup with an external communication device.

The relays of the ALP-4000 series has six three-phase current inputs. Each input can also be used as a single-phase input. The relays also have two three-phase voltage inputs, sixteen inputs, eight high-speed power outputs and sixteen outputs.

2.1. TRANSFORMER PROTECTION

The multiple inputs and outputs of the relays of the ALP-4000 series allow for many different transformer protection schemes.

Wye-delta transformer with a grounding bank: It is possible to add a grounding transformer to a wye winding. It is also possible to limit ground faults in the wye winding by using a grounding inductance and/or resistance. However, this additional element in the circuit increases the fault risk and localization. The relay can protect the transformer with its differential protection as well as supervise the grounding bank overcurrent, as shown on Figure 1.

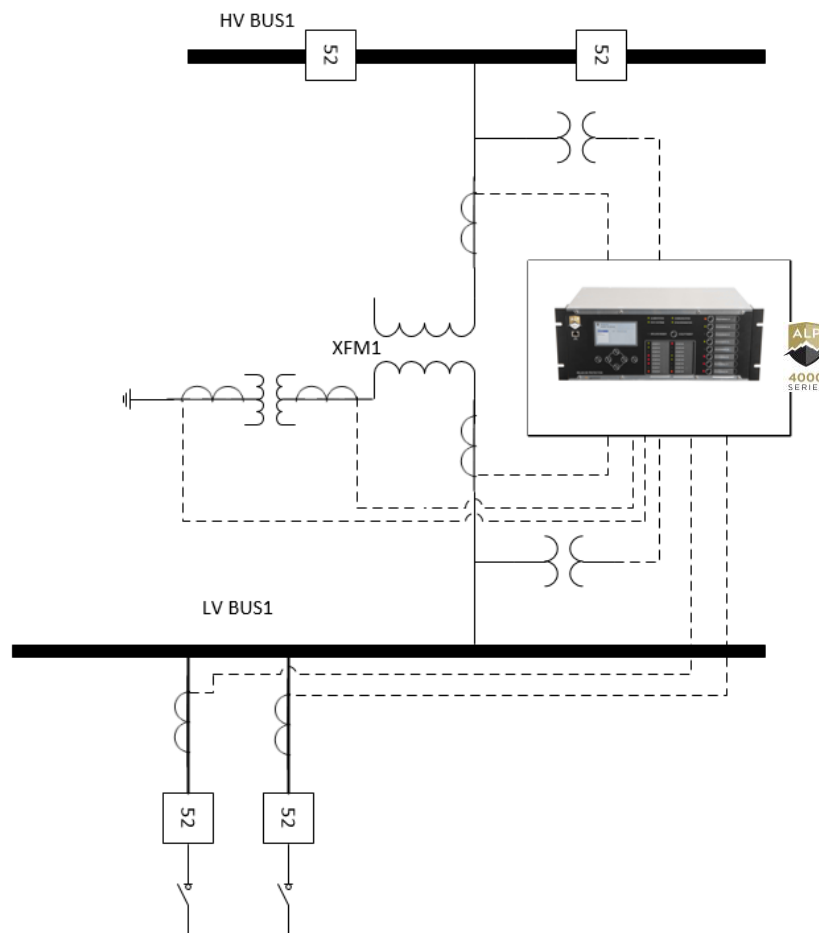


Figure 1 Δ -Y transformer protection line diagram

Three-phase autotransformer: It is possible to use 5 three-phase current transformers to protect a three-phase autotransformer and include neutral supervision. The two three-phase voltage inputs can supervise the high and low voltages, as shown on Figure 2.

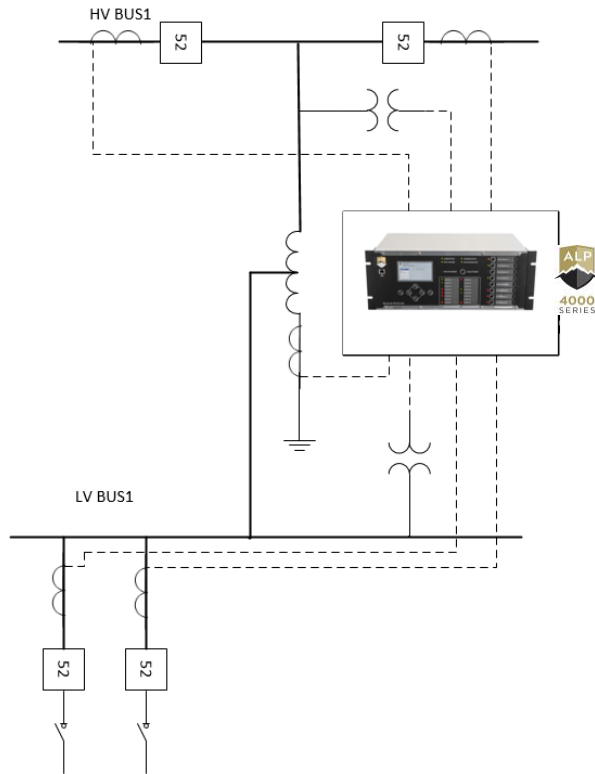


Figure 2 Autotransformer protection line diagram

Autotransformer with a tertiary winding: Autotransformers can use a loaded tertiary winding as an auxiliary power supply for the substation and VAR reactive compensation, amongst others. The winding can also be buried to stabilize the current and to provide a path for zero sequence and third harmonic currents. In the case of a loaded tertiary, a three-phase current input can be used to supervise the current.

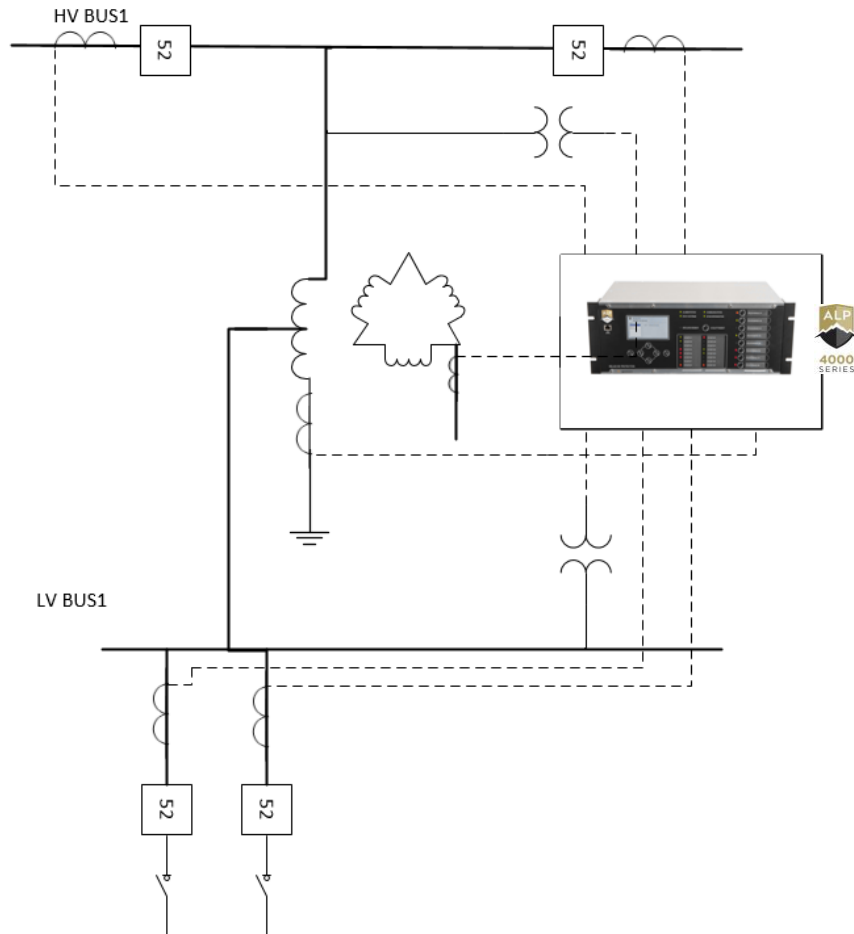


Figure 3 Three-phase autotransformer with loaded tertiary winding protection line diagram

Transformer bank built from 3 single-phase autotransformers with compensation tertiary winding: The supervision of the entire bank using single-phase autotransformers is possible by individually supervising each A, B and C phase while protecting the loaded tertiary winding.

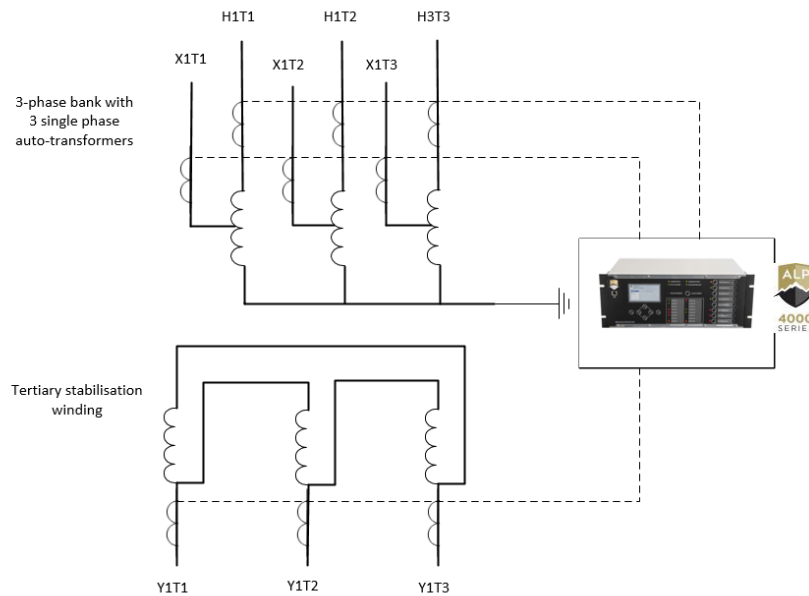


Figure 4 Transformer bank built from 3 single-phase autotransformers with loaded tertiary windings protection line diagram

2.2. COMMUNICATION NETWORK

Communication: Uses DNP3 for data point monitoring and remote control in a SCADA system.

Time synchronization: Supports modulated and demodulated IRIG-B time synchronization.

Web server access: Communicates with the HTTPS server via an Ethernet link.

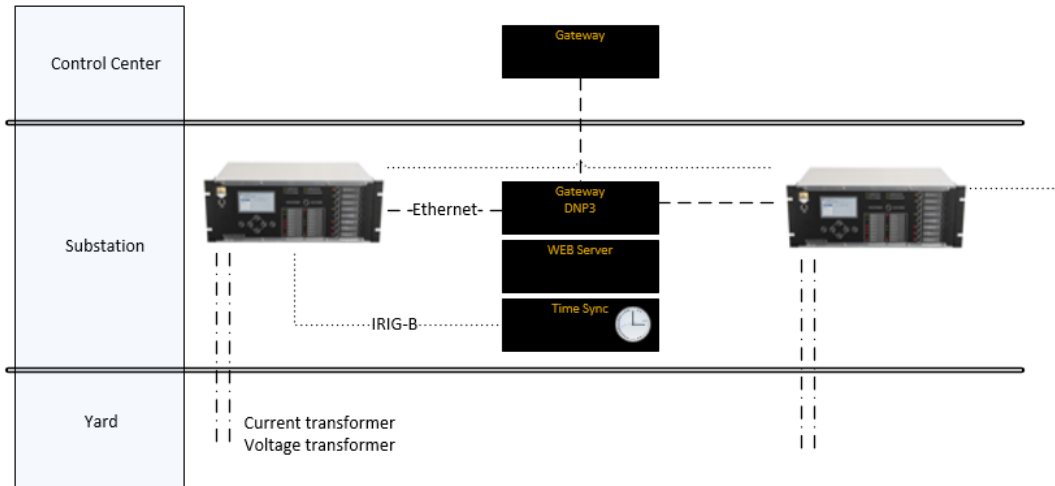


Figure 5 ALP-4000 series cabled network

The communication ports of the relay are on the front and the back of the housing: a maintenance copper Ethernet port is located on the front while two optical Ethernet ports are on the back. Only two ports can be simultaneously active. The relay real-time clock can be synchronized with a modulated or demodulated IRIG-B signal connected to a port on the back of the device. The ALP-4000 series supports DNP3 communication complying to interoperability subset level 2. It also has a built-in secure web server to remotely monitor and configure the device.

2.3. ALP-4000 SERIES FUNCTION OVERVIEW

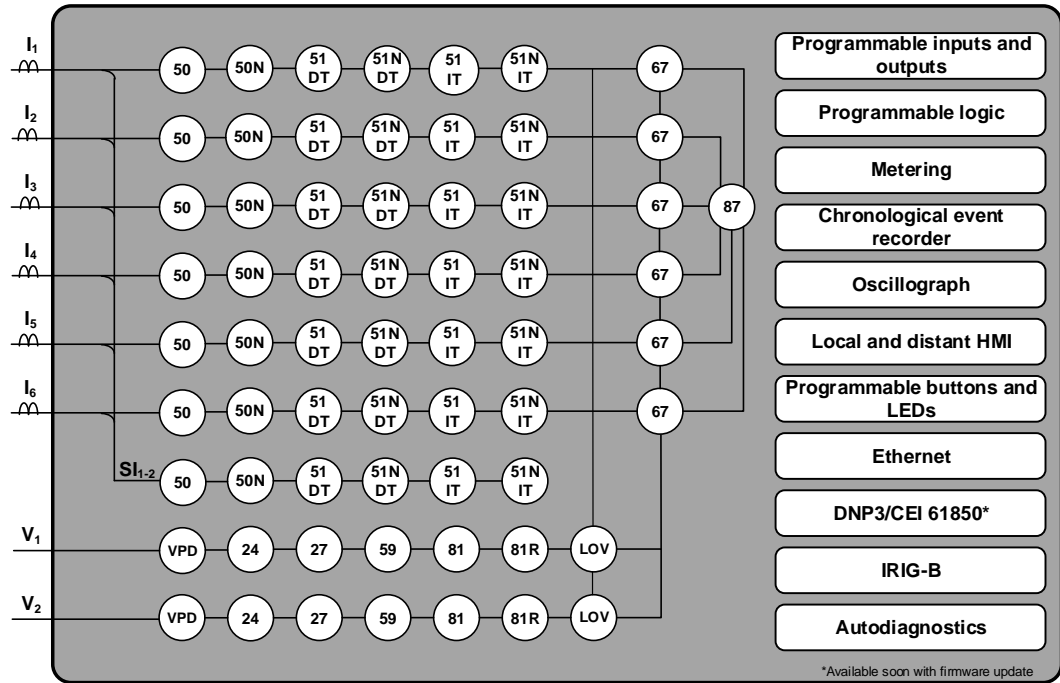


Figure 6 ALP-4000 series function overview

CURRENT TRANSFORMER COMPENSATION

Each input can be independently compensated for phase and magnitude. It is therefore unnecessary to use additional current transformers.

TRANSFORMER DIFFERENTIAL PROTECTION ELEMENTS

The relays of the ALP-4000 series are equipped with the most used transformer differential protection elements: unrestrained differential element (87U) and percent restrained differential element (87R) with harmonic restraint, traditional harmonic blocking or secure harmonic blocking. Up to six three-phase current inputs can be used. Each current input is independently compensated for phase and magnitude. The restrained differential protection element protects from false trips during transformer inrush and overexcitation conditions. In contrast, the unrestrained differential protection element does not account for these phenomena and reacts more quickly.

OVERCURRENT PROTECTION ELEMENTS

The relays of the ALP-4000 series also provide overcurrent protection for the transformer either via instantaneous trip (50/50N), definite time (51 DT/51N DT) and/or inverse time protection elements (51 IT/51N IT). These elements work simultaneously.

PHASE DIRECTIONAL ELEMENT

The relays of the ALP-4000 series can also determine the direction of the current flow as a mean to control other protection elements via their blocking setting. It is therefore possible to configure a phase directional overcurrent element (67) by combining the phase directional element (DIR) to a phase overcurrent protection element (50/51DT/51IT).

VOLTS PER HERTZ PROTECTION ELEMENTS

Volts per Hertz (24) protection elements are available to detect transformer overexcitation.

OVER- AND UNDERVOLTAGE PROTECTION ELEMENTS

The relays of the ALP-4000 series also monitor voltage levels via undervoltage (27) and overvoltage protection elements (59).

FREQUENCY PROTECTION ELEMENTS

Under/over-frequency (81) and rate-of-change-of-frequency protection elements (81R) are available to protect the transformer during network frequency deviations.

PEAK VOLTAGE DETECTOR

The relays of the ALP-4000 series include a voltage peak detection element which analyzes sampled raw values before filtering. This element identifies non-conventional electrical phenomena which are undetected by traditional protection functions.

LOSS OF VOLTAGE DETECTION ELEMENT

Loss of voltage detection elements (LOV) are available to control protection elements which use voltage inputs in their decision process.

PROGRAMMABLE INPUTS AND OUTPUTS

Outputs of the relays of the ALP-4000 series can be configured individually to operate from the value of any of the relay's binary points (e.g. output of a function, timer, latch, logic equation etc.). Similarly, inputs of the relay can be used in any element using a binary point as an input (e.g. a logic equation).

HIGH-SPEED POWER OUTPUTS

The relays of the ALP-4000 series feature 8 high-speed power outputs based on a parallel combination of optocoupled transistors and mechanical relays.

METERING AND MONITORING

Real-time measurements are taken from raw voltages and currents with a sampling rate of 7,680 Hz. The relay can be configured to track the frequency of the network by adjusting its sampling rate to 128 samples per network cycle.

PROGRAMMABLE LOGIC AND EQUATIONS

Up to 50 logic equations can be configured. Latches, timers and logic functions are available to build complex equations.

RUNTIME SANITY CHECKS

The runtime sanity check continuously verifies system integrity in order to effectively detect any hardware malfunction in the device.

CHRONOLOGICAL EVENT RECORDER

Up to 1,000 different kinds of events (Protection, Security, Configuration, Maintenance) can be recorded in the ALP-4000. Each event may provide details of the system status at the time of the event.

OSCILLOGRAPH

The relays of the ALP-4000 series have 10 configurable oscillographs. The oscillograms have a maximum duration of 5 seconds and are saved either in IEEE C37.111-1999 or IEEE C37.111-2013 formats, as chosen by the user.

SECURE ACCESS

Three access levels are available to secure the access to the relay interfaces.

COMMUNICATION

The protection relay is equipped with 3 Ethernet ports (copper or optical). It conforms to DNP3 Level 2 Subset Definitions requirements. The secure web interface of the relay uses SSL/TLS transport protocol to secure its communications. It allows easy access to the relay from a computer connected to the same IP network.

3

DEVICE OVERVIEW

3 DEVICE OVERVIEW

This section describes the different features available on the relays of the ALP-4000 series.

3.1. FRONT AND BACK PANEL DESCRIPTION

The following features are found on the front panel:

- Maintenance copper Ethernet port.
- LCD display.
- Control buttons for LCD menus.
- 4 LEDs to reflect the system health.
- 1 trip LED.
- 16 programmable LEDs.
- 1 acknowledge button.
- 8 programmable buttons.
- 8 programmable button LEDs.

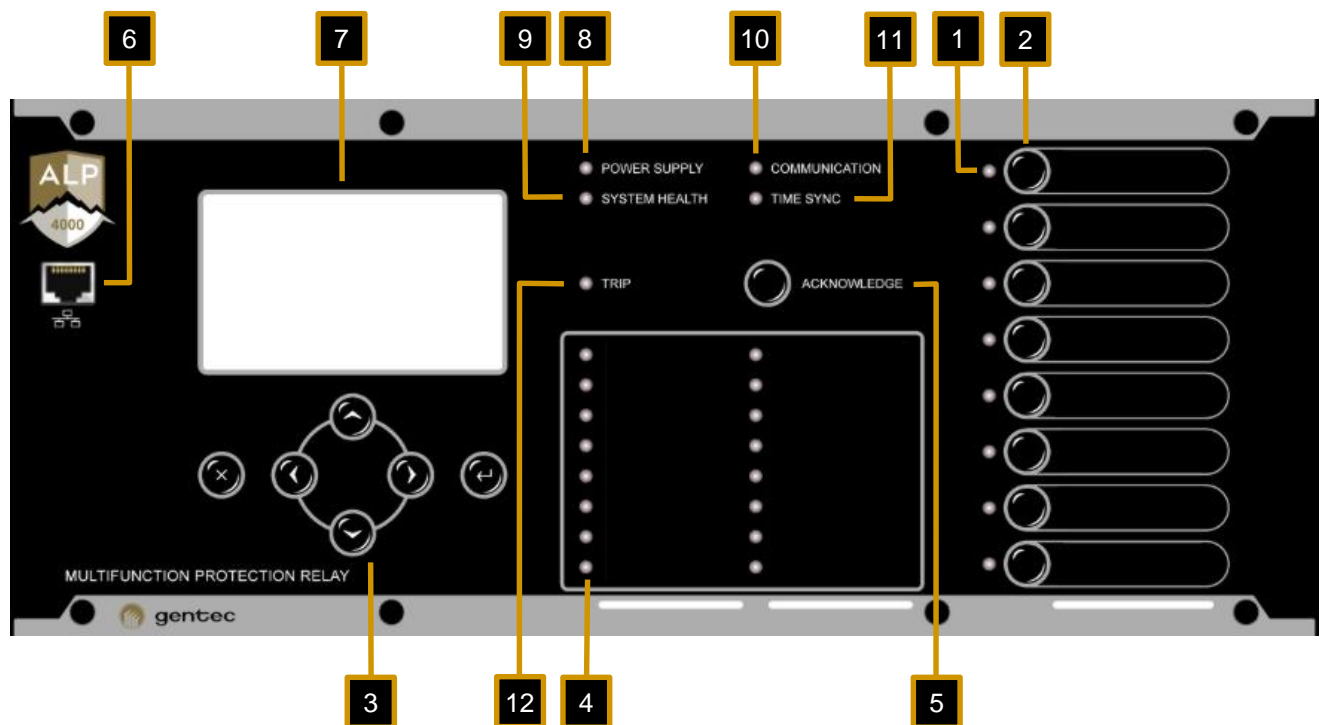


Figure 7 ALP-4000 series front panel.

NUMBER	DESCRIPTION			
1	Programmable button LEDs			
2	Programmable button			
3	Navigation buttons			
4	Programmable LEDs			
5	Trip acknowledgement			
6	Maintenance copper Ethernet port			
7	Operator screen			
NUMBER	GREEN	RED	AMBER	OFF
8	Normal power	Power failure	Relay starting	---
9	No fault	Relay locked	Active warning	Relay starting
10	At least one port is linked to a network	---	---	No port linked to a network
11	IRIG-B source connected	IRIG-B source disconnected	---	Relay starting
12	---	Trip requiring acknowledgement. It stays red until acknowledged.	---	No trip since last acknowledgement.

Table 2 ALP-4000 series front panel details

The following features are found on the back panel:

- Connectors for the inputs.
- Screw terminals for the analog current inputs.
- Screw terminals for the analog voltage inputs.
- Connectors for the outputs.
- Connectors for the high-speed power outputs.
- Connector for the alarm relay output.
- Connector for the IRIG-B input.
- Connector for the optical Ethernet links.
- 125 Vdc / 120 Vac power terminals.
- Ground connection screw.
- Material safety data sheet.

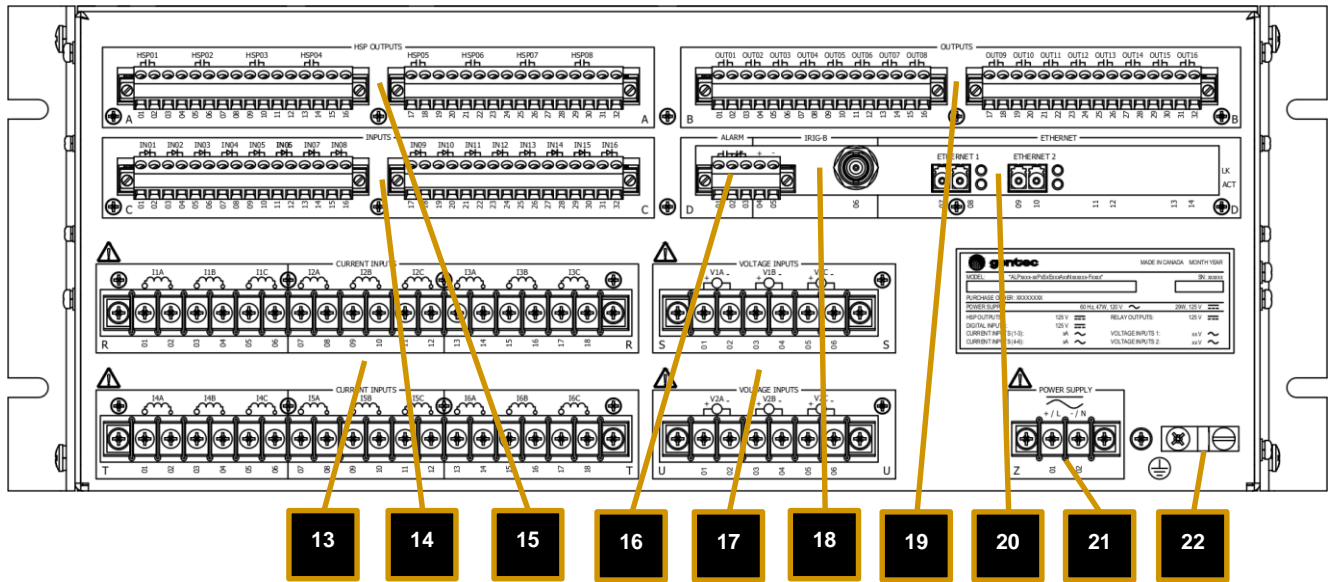


Figure 8 ALP-4100 protection relay back panel

NUMBER	DESCRIPTION
13	Current analog inputs
14	Inputs
15	High-speed, power outputs
16	Alarm relay output, normally closed
17	Voltage analog inputs
18	IRIG-B time synchronization ports
19	Outputs
20	Optical Ethernet ports
21	Power supply
22	Ground terminal

Table 3 ALP-4000 Protection relay back panel description

3.2. INPUTS/OUTPUTS DESCRIPTION

3.2.1. HIGH-SPEED POWER OUTPUTS

The relays of the ALP-4000 series have 8 high-speed power outputs. These outputs use a hybrid technology, consisting of a parallel combination of optocoupled transistors and mechanical relays giving them a high closure and cutoff power, as well as a fast closure. The high-speed power outputs are of type Normally Open (NO). They are independently isolated from one another. The high-speed power output was designed to work in both polarity wirings.

3.2.2. OUTPUTS

The relays of the ALP-4000 series have 16 Normally Open (NO) dry contact outputs built from mechanical relays. They are independently isolated from one another. Each output can work in both polarity wirings.

3.2.3. INPUTS

The relays of the ALP-4000 series have 16 all or nothing inputs. The inputs are isolated from one another by optocouplers. They are also polarized; for their installation, refer to section 4.4.3. The inputs were designed to work at 125 Vdc. They also have an adjustable debounce timer. This timer can have a value of 4 to 8 ms. It is important to note that this time is valid at 60 Hz. If frequency tracking is enabled, it will vary with the grid frequency.

3.2.4. ALARM OUTPUT

The relays of the ALP-4000 series provide a Normally Closed (NC) dry contact alarm output. This output is isolated from all other inputs and outputs. The alarm output is not polarized, therefore it can be powered in both polarities.

3.2.5. IRIG-B INPUT

The ALP-4000 protection relay accepts modulated IRIG-B time synchronization on a single port. The ALP-4100 model has the choice between a modulated or demodulated signal on one of two ports. The IRIG-B ports are isolated by an isolation transformer.

3.2.6. ETHERNET LINKS

The relays of the ALP-4000 series have two independent optical ports located on the back panel. These optical ports are 100Base-FX or 1000Base-SX (optional).

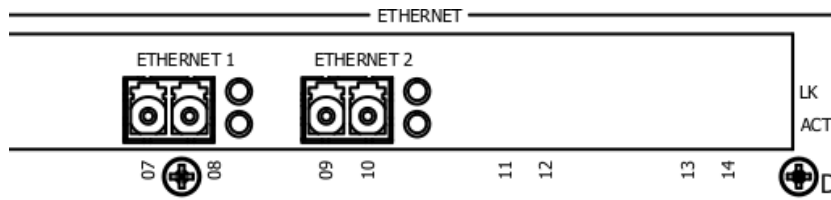


Figure 9 Optical Ethernet ports LEDs

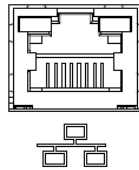


Figure 10 Copper Ethernet port LEDs

Two LEDs are available with each Ethernet port: LINK and ACTIVITY. For the optical Ethernet port, the LINK LED can be identified by the LK acronym, while for the copper Ethernet port, it is located on the left of the RJ45 connector. The LINK LED informs the user about the state and speed of the Ethernet link. For the optical Ethernet port, the ACTIVITY LED is identified by the acronym ACT, while for the copper Ethernet port, it is located on the right of the RJ45 connector. The ACTIVITY LED informs the user of the transmission and reception activity on the Ethernet link. Note that the ACTIVITY LED is always green.

ETHERNET LED DESCRIPTION			
LINK LED STATE	LINK LED COLOR	ACTIVITY LED STATE	DESCRIPTION
OFF	-	OFF	No link detected
ON	Amber	OFF	100 Mbps link detected, no activity
ON	Amber	Blinking	100 Mbps link detected, with activity
ON	Green	OFF	1000 Mbps link detected, no activity
ON	Green	Blinking	1000 Mbps link detected, with activity

Table 4 Description of the states of the Ethernet LEDs

Note: On the ALP-4000 model, the copper Ethernet port is internally connected to the second optical Ethernet port. On the ALP-4100 model, the copper Ethernet port is internally connected to the first optical Ethernet port. Therefore, they cannot be used simultaneously. To activate the copper Ethernet port, refer to section 4.6.1.

3.2.7. CURRENT INPUTS

The relays of the ALP-4000 series feature six three-phase current inputs. The current inputs are designed using current transformers. They are independently isolated from one another.

3.2.8. VOLTAGE INPUTS

The relays of the ALP-4000 series feature two three-phase voltage inputs. The voltage inputs are designed using voltage transformers. They are independently isolated from one another.

3.3. MODEL CONFIGURATION AND DETAIL

Table 5 details the available model configurations for the ALP-4000 series.

	ALP	4	0	0	0	E	X	P	1	S	1	E	1	2	X	A	2	2	N	30	20	10	
Model																							
Height		4																					
2UM : 2																							
4UM : 4																							
Option #1			0																				
0 : Processing unit M0																							
1 : Processing unit M1																							
Option #2				0																			
0 : Aucun																							
Option #3					0																		
0 : Aucun																							
Language						E																	
F : French																							
E : English																							
Conformal coating							X																
X : Without coating																							
C : With coating (tropicalization)																							
Power supply								P															
1 : 120Vac/125Vdc									1														
Time synchronization										S													
1 : IRIG-B modulated											1												
2 : IRIG-B demodulated																							
Ethernet												E											
Front port													1										
1 :100/1000 Base-Tx																							
Location 1														2									
1 :2x1000Base-Sx (fiber)																							
2 :2x100Base-Fx (fiber)																							
Unavailable location															X								
X : None																							
Analog inputs																A							
Inputs C1, C2, C3, V1																	2						
1 : 1A, 1A, 1A, 70V																							
2 : 5A, 5A, 5A, 70V																							
Inputs C4, C5, C6, V2																		2					
1 :1A, 1A, 1A, 70V																							
2 : 5A, 5A, 5A, 70V																							
Inputs/outputs																			N				
Inputs/outputs #1																					30		
30 : 8x high-speed power outputs																							
125Vdc																							
Inputs/outputs #2																						20	
20 : 16x digital outputs 125Vdc																							
Inputs/outputs #3																							10
10 : 16x inputs																							

Table 5 Available model configurations for the ALP-4000 series

4

INSTALLATION

4 INSTALLATION

4.1. INSPECTION CHECKLIST

Please verify that the product is free from any damage that may have occurred during transport. Also, make sure that none of the items listed below are missing from the box.

4.1.1. BOX CONTENTS

- ALP-4000 series protection relay.
- Installation CD for the ALP-4000 series software suite.
- 6 pluggable 16-pole screw connectors.
- 1 pluggable 2-pole screw connector.

4.2. DEVICE MOUNTING

The relays of the ALP-4000 series were designed to be assembled in a 19-inch rack. The rack must have a height of 4U (7 inches/17.8 cm). Mount the relay in a 19-inch rack using 4 rack screws on the frame brackets located on both sides of the relay.

4.3. HOUSING DIMENSIONS

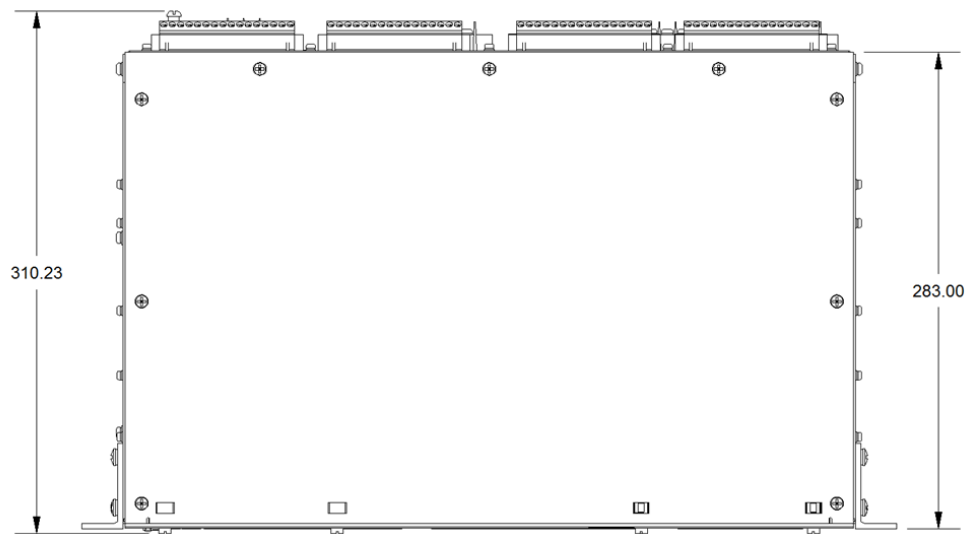


Figure 11 Housing dimensions - View from above – ALP-4000 series

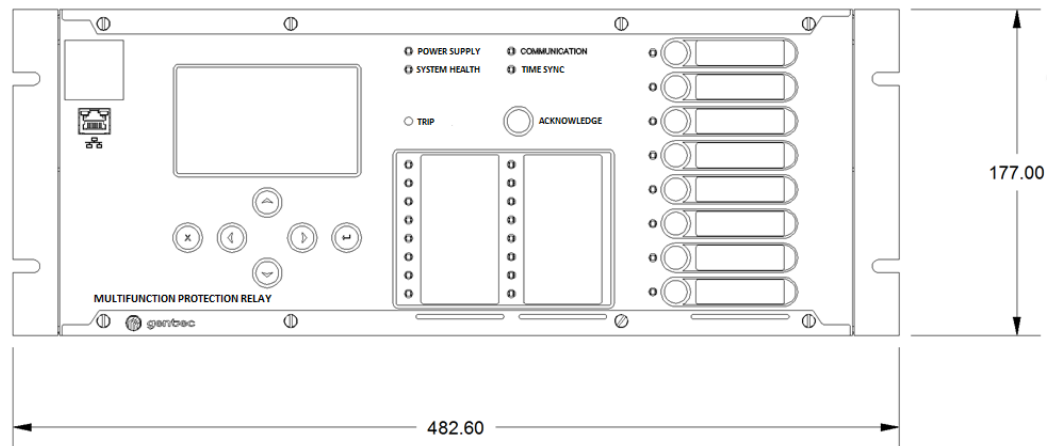


Figure 12 Housing dimensions - Front view – ALP-4000 series

4.4. CONNECTIONS



DANGER: Make sure you have a protective conductor connected to the screw of the terminal marked with this symbol at all times. Refer to the Installation section for more information. Failure to follow this practice could result in electric shock and cause injury or death. Make sure this conductor is connected before handling the device.

RECOMMENDED WIRE GAUGES AND TIGHTENING TORQUES		
Branch point	Recommended gauge	Recommended tightening torque
Power supply	12-22AWG	-
Ground	6-12AWG	Screw 6-32 (1Nm) Terminal (2.4Nm)
Current input	12-22AWG	-
Voltage input	12-22AWG	-
Input	14-22AWG	0.55Nm
High-speed power output	14-22AWG	0.55Nm
Output	14-22AWG	0.55Nm
Alarm	14-22AWG	0.55Nm
Connector	-	0.55Nm

Table 6 Recommended wire gauges and tightening torques

4.4.1. POWER SUPPLY AND PROTECTIVE GROUNDING

Power is supplied to the protection relay with a screw terminal with 2 positions located on the bottom right of the rear panel. The power cable wire gauge must be between 22 AWG and 12 AWG. However, the gauge used must be selected according to the current that will flow through the cable and must respect the local electric code.

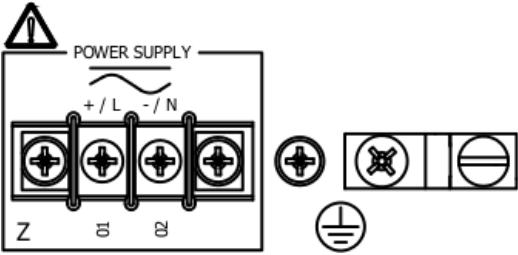


Figure 13 Power supply and protective grounding connectors

There are two ways to connect the protective conductor to the ground. You may use the #6-32 grounding screw or the grounding terminal, both connected to the frame of the protection relay. Both components are located to the right of the power supply connector. A low-impedance (<0.1 ohm) protective grounding must be connected at all times to the

ground screw or the ground terminal. A tightening torque of 1 Nm for #6-32 ground screw and 2.4 Nm on the ground terminal must be observed during installation. A ground conductor with a gauge between 2 AWG and 6 AWG must be used.

PINOUT FOR THE POWER SUPPLY CONNECTOR		
Signal	Description	Pin
+ / L	Positive power supply (DC) / Line (AC)	Z01
- / N	Power return (DC) / Neutral (AC)	Z02

Table 7 Pinout for the power connector

4.4.2. CURRENT AND VOLTAGE INPUTS

The protection relay has six three-phase current inputs, as shown on Figure 15. These six current inputs are divided into 18-pole screw terminals. The three-phase current inputs are identified by numbers 1 to 6, while the 3 phases of a current input are identified by letters A, B and C. A tightening torque of 1 Nm must be observed during installation. A feed wire gauge between 22 AWG and 12 AWG may be used. However, the gauge used must be selected according to the current that will flow through the cable and must respect the local electric code.



DANGER: Before disconnecting any current input, make sure that the current loop has previously been short circuited. Failure to follow this practice could result in electric shock and cause injury or death.

The current inputs are polarized. In order to comply with the angle between the phases of the three-phase current, it is important to respect the input polarity. The positive polarity is indicated by an empty circle to the left of the symbol, while the negative polarity is represented by a solid black circle to the right of the symbol, as shown on Figure 14.



Figure 14 Current input polarities

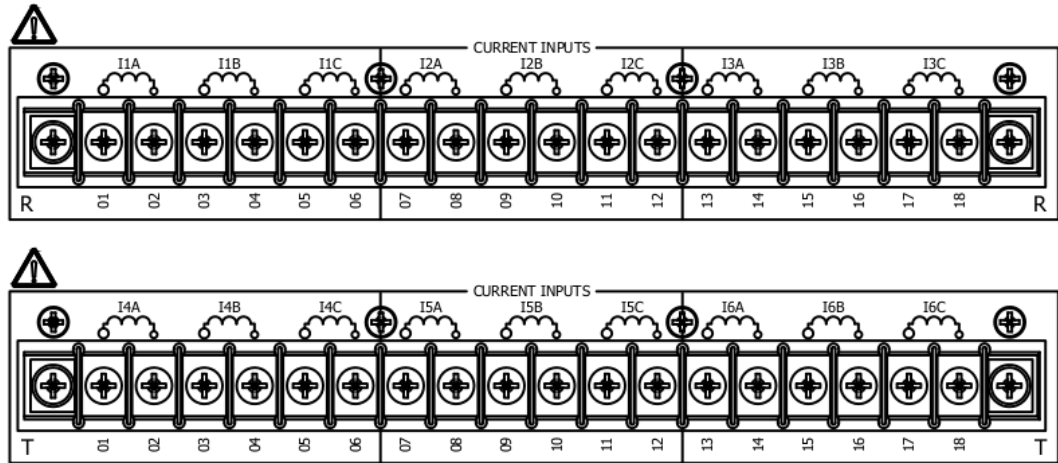


Figure 15 Current inputs connectors

CURRENT INPUTS 1-3 PINOUT

Signal	Description	Pin
I1A+	Three-phase current input 1, phase A, positive polarity	R01
I1A-	Three-phase current input 1, phase A, negative polarity	R02
I1B+	Three-phase current input 1, phase B, positive polarity	R03
I1B-	Three-phase current input 1, phase B, negative polarity	R04
I1C+	Three-phase current input 1, phase C, positive polarity	R05
I1C-	Three-phase current input 1, phase C, negative polarity	R06
I2A+	Three-phase current input 2, phase A, positive polarity	R07
I2A-	Three-phase current input 2, phase A, negative polarity	R08
I2B+	Three-phase current input 2, phase B, positive polarity	R09
I2B-	Three-phase current input 2, phase B, negative polarity	R10
I2C+	Three-phase current input 2, phase C, positive polarity	R11
I2C-	Three-phase current input 2, phase C, negative polarity	R12
I3A+	Three-phase current input 3, phase A, positive polarity	R13
I3A-	Three-phase current input 3, phase A, negative polarity	R14
I3B+	Three-phase current input 3, phase B, positive polarity	R15
I3B-	Three-phase current input 3, phase B, negative polarity	R16
I3C+	Three-phase current input 3, phase C, positive polarity	R17
I3C-	Three-phase current input 3, phase C, negative polarity	R18

CURRENT INPUTS 4-6 PINOUT		
Signal	Description	Pin
I4A+	Three-phase current input 4, phase A, positive polarity	T01
I4A-	Three-phase current input 4, phase A, negative polarity	T02
I4B+	Three-phase current input 4, phase B, positive polarity	T03
I4B-	Three-phase current input 4, phase B, negative polarity	T04
I4C+	Three-phase current input 4, phase C, positive polarity	T05
I4C-	Three-phase current input 4, phase C, negative polarity	T06
I5A+	Three-phase current input 5, phase A, positive polarity	T07
I5A-	Three-phase current input 5, phase A, negative polarity	T08
I5B+	Three-phase current input 5, phase B, positive polarity	T09
I5B-	Three-phase current input 5, phase B, negative polarity	T10
I5C+	Three-phase current input 5, phase C, positive polarity	T11
I5C-	Three-phase current input 5, phase C, negative polarity	T12
I6A+	Three-phase current input 6, phase A, positive polarity	T13
I6A-	Three-phase current input 6, phase A, negative polarity	T14
I6B+	Three-phase current input 6, phase B, positive polarity	T15
I6B-	Three-phase current input 6, phase B, negative polarity	T16
I6C+	Three-phase current input 6, phase C, positive polarity	T17
I6C-	Three-phase current input 6, phase C, negative polarity	T18

Table 8 Current inputs pinout

The protection relay also has two three-phase voltage inputs, as shown on Figure 16. The two voltage inputs are divided into 6-pole screw terminals. The three-phase voltage inputs are identified by numbers 1 and 2, while the 3 phases of a voltage input are identified by letters A, B and C.

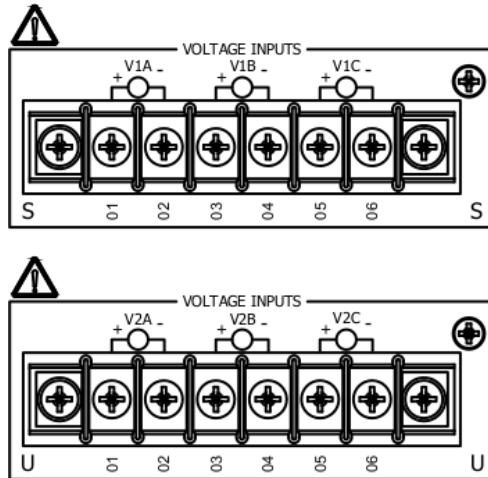


Figure 16 Voltage inputs connectors

The voltage inputs are polarized. In order to comply with the angle between the phases of the three-phase voltage inputs, it is important to respect the input polarity. The positive polarity is indicated by “+” to the left of the symbol, while the negative polarity is represented by a “-” to the right of the symbol, as shown on Figure 17.

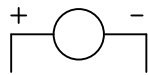


Figure 17 Voltage input polarities

A tightening torque of 1 Nm must be respected during installation. A feed wire gauge between 22 AWG and 12 AWG may be used. However, the gauge used must be selected according to the current that will flow through the cable and must respect the local electric code.

VOLTAGE INPUT 1 PINOUT

Signal	Description	Pin
V1A+	Three-phase voltage input 1, phase A, positive polarity	S01
V1A-	Three-phase voltage input 1, phase A, negative polarity	S02
V1B+	Three-phase voltage input 1, phase B, positive polarity	S03
V1B-	Three-phase voltage input 1, phase B, negative polarity	S04
V1C+	Three-phase voltage input 1, phase C, positive polarity	S05

V1C-	Three-phase voltage input 1, phase C, negative polarity	S06
VOLTAGE INPUT 2 PINOUT		
Signal	Description	Pin
V2A+	Three-phase voltage input 2, phase A, positive polarity	U01
V2A-	Three-phase voltage input 2, phase A, negative polarity	U02
V2B+	Three-phase voltage input 2, phase B, positive polarity	U03
V2B-	Three-phase voltage input 2, phase B, negative polarity	U04
V2C+	Three-phase voltage input 2, phase C, positive polarity	U05
V2C-	Three-phase voltage input 2, phase C, negative polarity	U06

Table 9 Voltage inputs pinout

4.4.3. INPUTS AND OUTPUTS

The protection relay has eight Normally Open (NO) dry contact high-speed power outputs. Connection is done using two pluggable screw connectors. Each high-speed power output is identified by a number from 1 to 8. As these outputs are not polarized, they can be wired in both polarities. Notice the output configuration on *Figure 18*: some terminals are deliberately unused. These terminals must be left floating at all time. They have coded pins that prevent interchange between identical connectors of similar or different technology.

A tightening torque of 0.55 Nm must be respected during installation. A wire gauge between 24 AWG and 14 AWG may be used. However, the gauge used must be based on the current that will flow through the cable and it must respect the local electric code. The operating voltage of this wire must be of at least 300V. The pluggable connectors must be secured on the device by screwing the two screws on either side of the connector with a tightening torque of 0.55 Nm.

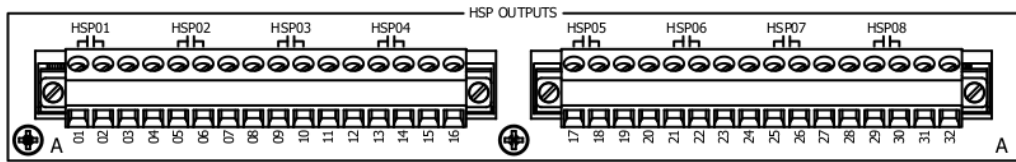


Figure 18 High-speed power outputs connectors

HIGH-SPEED POWER OUTPUTS CONNECTOR 1 PINOUT

Signal	Description	Pin
HSP01_1	High-speed power output 1, contact 1	A01
HSP01_2	High-speed power output 1, contact 2	A02
-	Unused	A03
-	Unused	A04
HSP02_1	High-speed power output 2, contact 1	A05
HSP02_2	High-speed power output 2, contact 2	A06
-	Unused	A07
-	Unused	A08
HSP03_1	High-speed power output 3, contact 1	A09
HSP03_2	High-speed power output 3, contact 2	A10
-	Unused	A11
-	Unused	A12
HSP04_1	High-speed power output 4, contact 1	A13
HSP04_2	High-speed power output 4, contact 2	A14
-	Unused	A15
-	Unused	A16

HIGH-SPEED POWER OUTPUTS CONNECTOR 2 PINOUT

Signal	Description	Pin
HSP01_1	High-speed power output 5, contact 1	A17
HSP01_2	High-speed power output 5, contact 2	A18
-	Unused	A19
-	Unused	A20
HSP02_1	High-speed power output 6, contact 1	A21
HSP02_2	High-speed power output 6, contact 2	A22
-	Unused	A23
-	Unused	A24
HSP03_1	High-speed power output 7, contact 1	A25
HSP03_2	High-speed power output 7, contact 2	A26

-	Unused	A27
-	Unused	A28
HSP04_1	High-speed power output 8, contact 1	A29
HSP04_2	High-speed power output 8, contact 2	A30
-	Unused	A31
-	Unused	A32

Table 10 High-speed power outputs pinout

The protection relay has sixteen Normally Open (NO) dry contact outputs. The connection is done with two pluggable screw connectors. Each output is identified by a number from 1 to 16. As these outputs are not polarized, they can be wired in both polarities. They have coded pins that prevent interchange between identical connectors of similar or different technology.

A tightening torque of 0.55 Nm must be respected during installation. A wire gauge between 24 AWG and 14 AWG may be used. However, the gauge used must be selected according to the current that will flow through the cable and must respect the local electric code. The operating voltage of this wire must be at least 300V. The pluggable connectors must be secured on the device by screwing the two screws on either side of the connector with a tightening torque of 0.55 Nm.

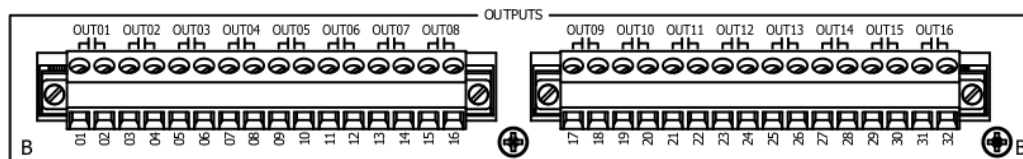


Figure 19 Outputs connectors

OUTPUTS CONNECTOR 1 PINOUT		
Signal	Description	Pin
OUT01_1	Output 1, contact 1	B01
OUT01_2	Output 1, contact 2	B02
OUT02_1	Output 2, contact 1	B03
OUT02_2	Output 2, contact 2	B04
OUT03_1	Output 3, contact 1	B05

OUT03_2	Output 3, contact 2	B06
OUT04_1	Output 4, contact 1	B07
OUT04_2	Output 4, contact 2	B08
OUT05_1	Output 5, contact 1	B09
OUT05_2	Output 5, contact 2	B10
OUT06_1	Output 6, contact 1	B11
OUT06_2	Output 6, contact 2	B12
OUT07_1	Output 7, contact 1	B13
OUT07_2	Output 7, contact 2	B14
OUT08_1	Output 8, contact 1	B15
OUT08_2	Output 8, contact 2	B16
OUTPUTS CONNECTOR 2 PINOUT		
Signal	Description	Pin
OUT09_1	Output 9, contact 1	B17
OUT09_2	Output 9, contact 2	B18
OUT10_1	Output 10, contact 1	B19
OUT10_2	Output 10, contact 2	B20
OUT11_1	Output 11, contact 1	B21
OUT11_2	Output 11, contact 2	B22
OUT12_1	Output 12, contact 1	B23
OUT12_2	Output 12, contact 2	B24
OUT13_1	Output 13, contact 1	B25
OUT13_2	Output 13, contact 2	B26
OUT14_1	Output 14, contact 1	B27
OUT14_2	Output 14, contact 2	B28
OUT15_1	Output 15, contact 1	B29
OUT15_2	Output 15, contact 2	B30
OUT16_1	Output 16, contact 1	B31
OUT16_2	Output 16, contact 2	B32

Table 11 Outputs pinout

The protection relay features 16 inputs. The connection is done with two pluggable screw connectors. Each input is identified by a number from 1 to 16. The inputs are polarized, so they must be connected in the direction represented by the diode as shown on Figure 20. The positive polarity (anode) connected to the terminal on the left of the symbol and the negative polarity (cathode) connected to the terminal on the right.

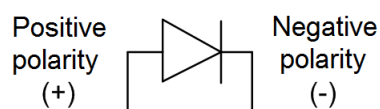


Figure 20 Inputs polarities

The connectors have coded pins that prevent interchange between identical connectors of similar or different technology. A tightening torque of 0.55 Nm must be respected during installation. A wire gauge between 24 AWG and 14 AWG may be used. The operating voltage of this wire must be at least 300V. The pluggable connectors must be secured on the device by screwing the two screws on either side of the connector with a tightening torque of 0.55 Nm.

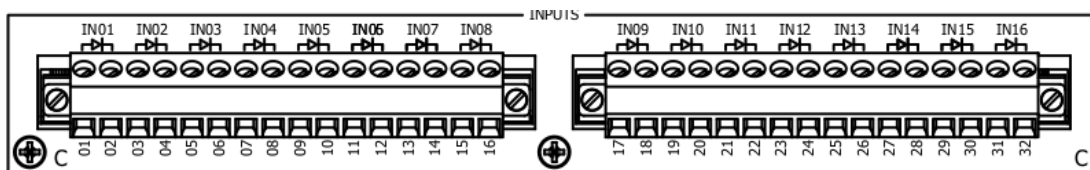


Figure 21 Inputs connectors

INPUTS CONNECTOR 1 PINOUT		
Signal	Description	Pin
IN01+	Input 1, positive polarity	C01
IN01-	Input 1, negative polarity	C02
IN02+	Input 2, positive polarity	C03
IN02-	Input 2, negative polarity	C04
IN03+	Input 3, positive polarity	C05
IN03-	Input 3, negative polarity	C06
IN04+	Input 4, positive polarity	C07

IN04-	Input 4, negative polarity	C08
IN05+	Input 5, positive polarity	C09
IN05-	Input 5, negative polarity	C10
IN06+	Input 6, positive polarity	C11
IN06-	Input 6, negative polarity	C12
IN07+	Input 7, positive polarity	C13
IN07-	Input 7, negative polarity	C14
IN08+	Input 8, positive polarity	C15
IN08-	Input 8, negative polarity	C16
INPUTS CONNECTOR 2 PINOUT		
Signal	Description	Pin
IN09+	Input 9, positive polarity	C17
IN09-	Input 9, negative polarity	C18
IN10+	Input 10, positive polarity	C19
IN10-	Input 10, negative polarity	C20
IN11+	Input 11, positive polarity	C21
IN11-	Input 11, negative polarity	C22
IN12+	Input 12, positive polarity	C23
IN12-	Input 12, negative polarity	C24
IN13+	Input 13, positive polarity	C25
IN13-	Input 13, negative polarity	C26
IN14+	Input 14, positive polarity	C27
IN14-	Input 14, negative polarity	C28
IN15+	Input 15, positive polarity	C29
IN15-	Input 15, negative polarity	C30
IN16+	Input 16, positive polarity	C31
IN16-	Input 16, negative polarity	C32

Table 12 Inputs pinout

4.4.4. TIME SYNCHRONIZATION

Time synchronization of the internal clock of the device is made by a modulated or demodulated signal, according to the chosen model, following the IRIG-B time code standard. The connection to the IRIG-B modulated or demodulated source must be done through a BNC cable with 50 ohms impedance. Model ALP-4100 has two IRIG-B connectors: BNC and twisted pair. Only one connector can be used, not both at the same time.

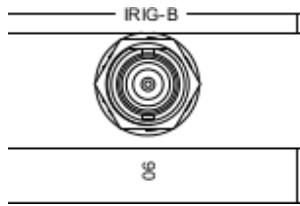


Figure 22 IRIG-B synchronization connector on the ALP-4000 model

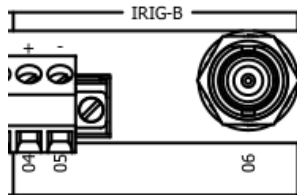


Figure 23 IRIG-B synchronization connectors on the ALP-4100 model

IRIG-B TIME SYNCHRONISATION PINTOUT		
Signal	Description	Pin
IRIGB_BNC	IRIG-B BNC input	D06
IRIGB+	IRIG-B input positive polarity (ALP-4100 only)	D04
IRIGB-	IRIG-B input negative polarity (ALP-4100 only)	D05

Table 13 IRIG-B time synchronisation pinout

4.4.5. ALARM OUTPUT

The relay features an alarm output built from a Normally Closed (NC) and/or Normally Open (NO) dry contact relay. The NO relay is only available for the ALP-4100 model. The connection is done through a 2-pole screw terminal. A tightening torque of 0.55 Nm must

be respected during installation. A wire gauge between 24 AWG and 14 AWG may be used. However, the gauge used must be selected according to the current that will flow through the cable and must respect the local electric code. The operating voltage of this wire must be at least 300V. The pluggable connector must be secured on the device by screwing the two screws on either side of the connector with a tightening torque of 0.55 Nm.

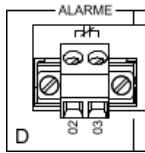


Figure 24 Alarm output connector on the ALP-4000 model

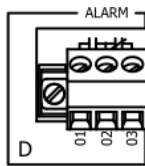


Figure 25 Alarm output connector on the ALP-4100 model

ALARM OUTPUT CONNECTOR PINOUT

Signal	Description	Pin
ALARM_1	Alarm output NO contact (ALP-4100 only)	D01
ALARM_2	Alarm output common contact	D02
ALARM_3	Alarm output NC contact	D03

Table 14 Alarm output pinout

4.4.6. COMMUNICATION PORTS

The protection relay features 3 communication ports: two 100Base-FX (1000Base-SX optional) fiber Ethernet ports located on the back panel and one 10/100/1000Base-TX copper Ethernet port on the front panel. The 100Base-FX fiber Ethernet ports have a nominal wavelength of 1300 nm, while 1000Base-SX have a 850 nm wavelength. In both cases, multimode 62.5/125 μm optical fiber with LC connectors should be used.

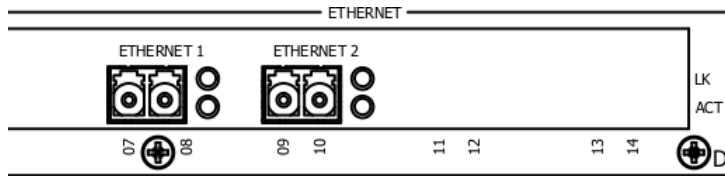


Figure 26 Optical Ethernet ports

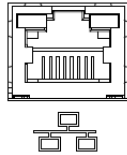


Figure 27 Copper Ethernet port

COMMUNICATION PORTS PINOUT		
Signal	Description	Broche
ETH_OPT1_TX	Optical Ethernet port 1, Tx connector	D07
ETH_OPT1_RX	Optical Ethernet port 1, Rx connector	D08
ETH_OPT2_TX	Optical Ethernet port 2, Tx connector	D09
ETH_OPT3_RX	Optical Ethernet port 2, Rx connector	D10
ETH_METAL	Copper Ethernet port	N/A

Table 15 Communication ports pinout

4.5. CUSTOM LABELS

Locations to insert custom labels can be found on the front panel of the relay. This section explains how to create the custom labels and how to insert them using material included with the relay. Figures 28 and 29 show the three slots at the bottom of each custom label location.

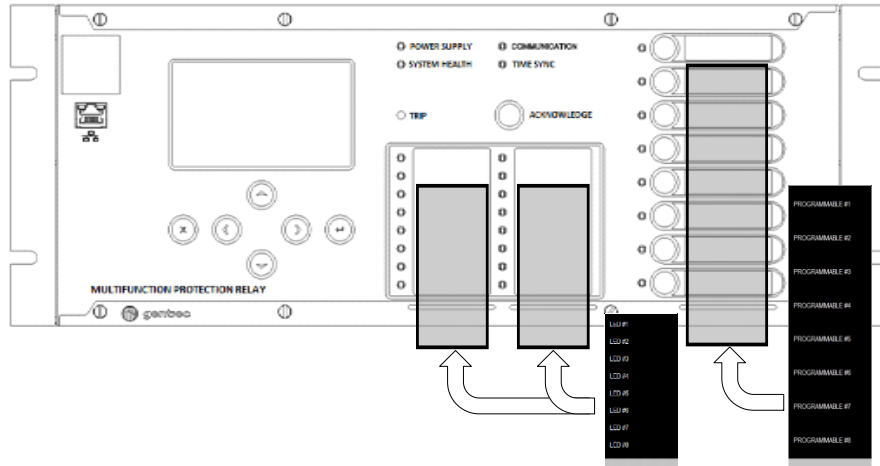


Figure 28 Custom label locations

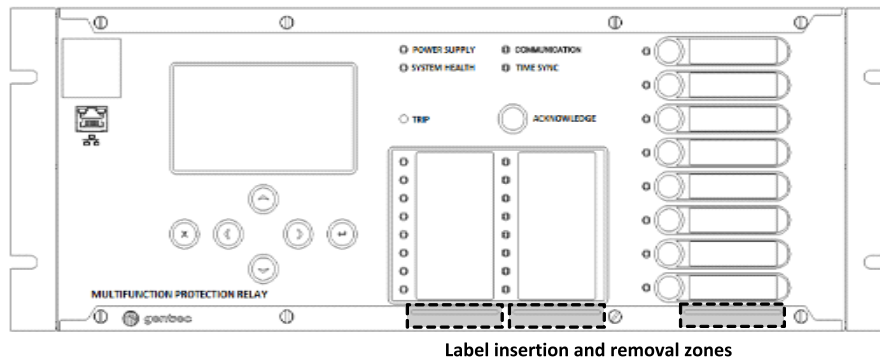


Figure 29 Custom label insertion and removal zones

4.5.1. CUSTOM LABEL CREATION

Using Microsoft Excel, it is possible to create a label containing the description of each button/LED of the relay. For this purpose, an Excel template is provided with the ALP-4000 series software suite. Simply open the Excel template and type the description at the appropriate places.

4.5.2. CUSTOM LABEL PRINTING

Before using the provided paper printing template, we suggest you first print a trial sheet to check the paper orientation. To do this, mark an 8 ½x11 blank sheet on its bottom right

corner and print the Excel template on this marked sheet. Compare this sheet with the provided paper template and place the paper template in your printer accordingly.

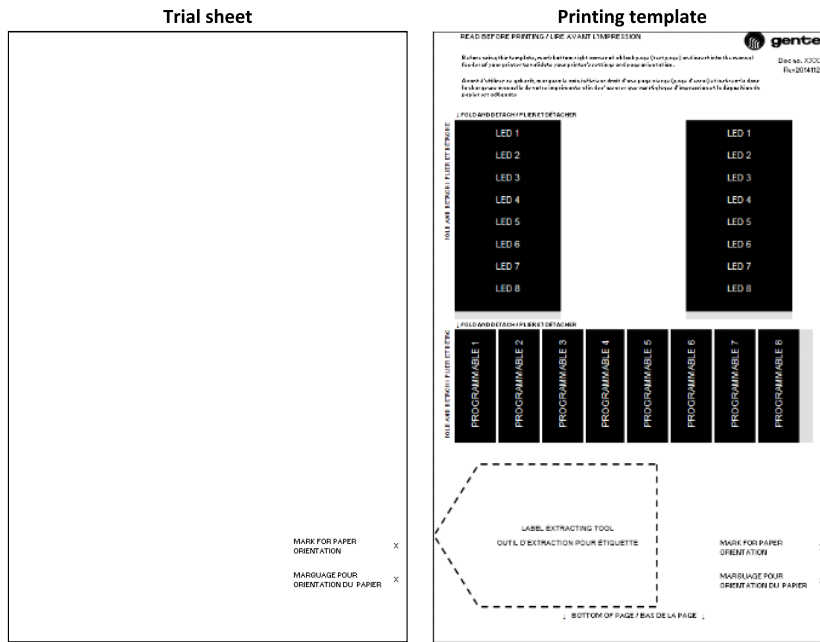


Figure 30 Printing the custom labels

4.5.3. CUSTOM LABEL REMOVAL

To help you remove the custom labels from the relay, use the removal tool by detaching it from the paper template provided with the relay, as seen on Figure 30. First insert the removal tool in the slot of the relay, under the label. Then push with your thumb on the bottom part of the label. Finally, with a down gesture, remove the label from the relay.

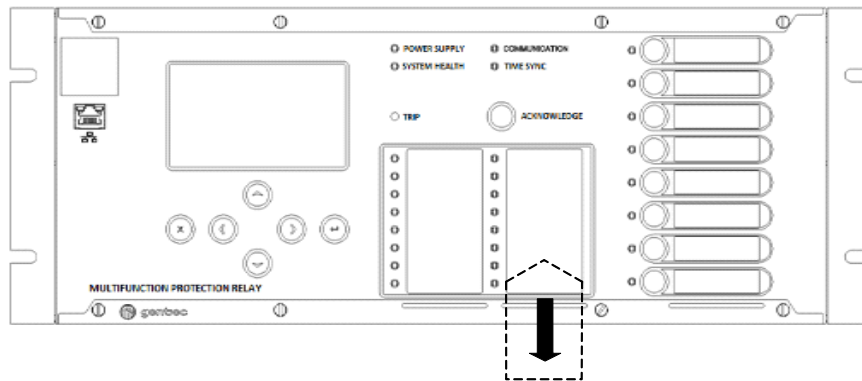


Figure 31 Custom label removal

4.6. SOFTWARE CONFIGURATION

Configuring the relays of the ALP-4000 series is a user-friendly operation. For the user, the main configuration effort lies in configuring the protection elements settings. The following sections present all software components that may require configuration when commissioning a relay.

4.6.1. ETHERNET CONFIGURATION

Before using the device after it has been connected, its Ethernet communication settings must be configured. This section first presents these settings and how to configure them. A procedure to follow for the initial connection to the relay is then explained. Finally, a troubleshooting section lists common checks to do in case a communication problem arises.

4.6.1.1. AVAILABLE ETHERNET COMMUNICATION SETTINGS

Before using the device after it has been connected, its Ethernet communication settings must first be configured. The Ethernet configuration is done from the local HMI located on the front panel. This section of the HMI is divided into 3 different pages: *Ethernet 1* for the first communication port, *Ethernet 2* for the second communication port and *Gateway* for both communication ports. Both *Ethernet* pages can be used to configure the IP address and network mask of the corresponding port number. The *Gateway* page can be used to configure the IP address of the default gateway that will be used by the device.

Any authenticated user can view the Ethernet configuration pages. However, only users with the *Settings* and *Administration* access levels can modify the Ethernet configuration. Figures 32 to 34 show the *Ethernet* and *Gateway* pages of the local HMI. Tables 16 and 17 show the modifiable parameters for these configuration pages.

Administration
ETHERNET #1

TCP/IP Settings

Address Enabled

Mask

< ENT > : Edit selection
< ESC > : Back to maintenance

Figure 32 *Ethernet 1* configuration page

Administration
ETHERNET #2

TCP/IP Settings

Address Enabled

Mask

Optical (back) Copper (front)

< ENT > : Edit selection
< ESC > : Back to maintenance

Figure 33 *Ethernet 2* configuration page

For the ALP-4000 relay, from the *Ethernet 2* configuration page, you may select which interface link will be used: *optical* or *copper*. For the ALP-4100 relay, this is done on the *Ethernet 1* configuration page. Both links are physically on the same communication bus, but only one can be activated at a time.

Administration
GATEWAY

TCP/IP Settings

Gateway

< ENT > : Edit selection
< ESC > : Back to maintenance

Figure 34 *Gateway* configuration page.

SETTING	RANGE	DESCRIPTION
Address	0.0.0.0 to 255.255.255.255	Ethernet port's IP address
Mask	0.0.0.0 to 255.255.255.255	Ethernet port's network mask

Table 16 Ethernet configuration settings

SETTING	RANGE	DESCRIPTION
Address	0.0.0.0 to 255.255.255.255	Gateway IP address

Table 17 Gateway configuration settings

4.6.1.2. INITIAL CONNECTION TO THE RELAY

The relays of the ALP-4000 series are delivered with default settings for the Ethernet port with a double interface. These settings are shown in Table 18.

SETTING	VALUE
Interface type	Copper (front)
Address	169.254.0.1
Mask	255.255.0.0

Table 18 Default Ethernet settings

This default configuration allows the relay to easily communicate with a computer. The following procedure should be followed to establish a connection:

1. Configure the network interface of the computer in mode "Obtain an IP address automatically" (or in "DHCP" mode).
2. Connect the computer directly to the relay via its front copper port.
3. Execute the command "ipconfig /renew" in a command prompt.
4. Start a browser of your choice on your computer
5. Type address "169.254.0.1" in the browser's address bar.

If the relay's Ethernet address is not the one set by default, please contact your network administrator so they can assign to your computer a valid address that will allow you to connect to the relay.

To return the relay to its default Ethernet settings, enter the settings shown in Table 18 in the appropriate Ethernet configuration page according to the relay model (see section 4.6.1.1 for more information).

4.6.1.3. TROUBLESHOOTING

There can be many causes for a communication problem with the relay. The following list shows a series of checks to do in order to isolate the problem.

1. Check that the LEDs of the Ethernet port are lit and that the ACTIVITY LED blinks (see Table 4 for more information on the Ethernet LEDs)
 - a. If applicable, check that the configured interface is the one being used to connect to the relay.
 - b. Check that the cable used to connect to the relay is in good operating condition.
2. Check that the Ethernet interfaces of the relay are not on the same subnet.
3. If the computer and relay are physically connected to the same subnet, check that their addresses are in fact in that subnet.

4.6.2. SECURE WEB SERVER

The second configuration step is done using an Internet browser¹. Access to the relay's web server is done by entering one of the IP addresses configured in the previous step in the address bar of your browser. The web server uses secure hypertext protocol (HTTPS) with 3 access levels: *Monitoring*, *Settings* and *Administration*. The web server is described in detail in chapter 9 . Figure 35 shows the web server login page.

¹ If you use *Microsoft Internet Explorer*, it is strongly recommended to run a version equal or higher to version 6.

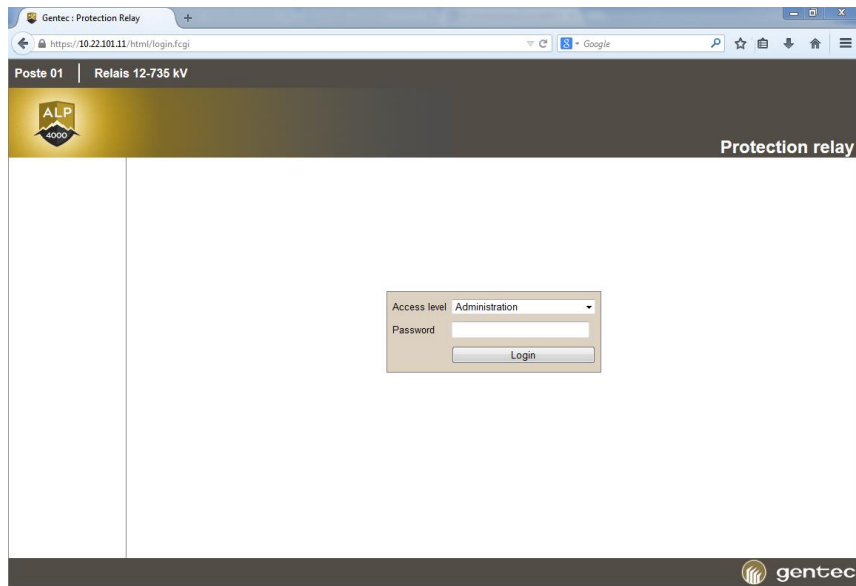


Figure 35 Web server login page

4.6.3. SETTINGS CONFIGURATION

The settings configuration software *ALP Config* can be installed from the software suite included with the delivery package of the relay or downloaded from our web site². It can be installed on any computer running at least a Windows XP operating system. Follow the directives provided with the CD to install the software suite.

The *ALP Config* software has a graphic interface based on a tree structure which allows easy configuration of all relay settings (except the Ethernet configuration). The software is explained in details in chapter 8 . The *ALP Config* software saves the configuration in an ICD-like file, based on the SCL format as specified in the IEC-61850-6 standard. This file is downloaded to the protection relay via the *Settings* page of the web server. Users of any access level may view this page. However, only users with access levels: *Settings* and *Administration* can download and retrieve a configuration file. To download the file on the relay, first browse for and select the desired file, and then click the *Transfer* button as shown on Figure 36. During the transfer, the relay validates the file conformance and then displays the transfer result. If it was successful, then the status “success” is shown. If an error occurred, its description will be shown.

² Contact your sales representative to obtain a link to the desired version of the software suite

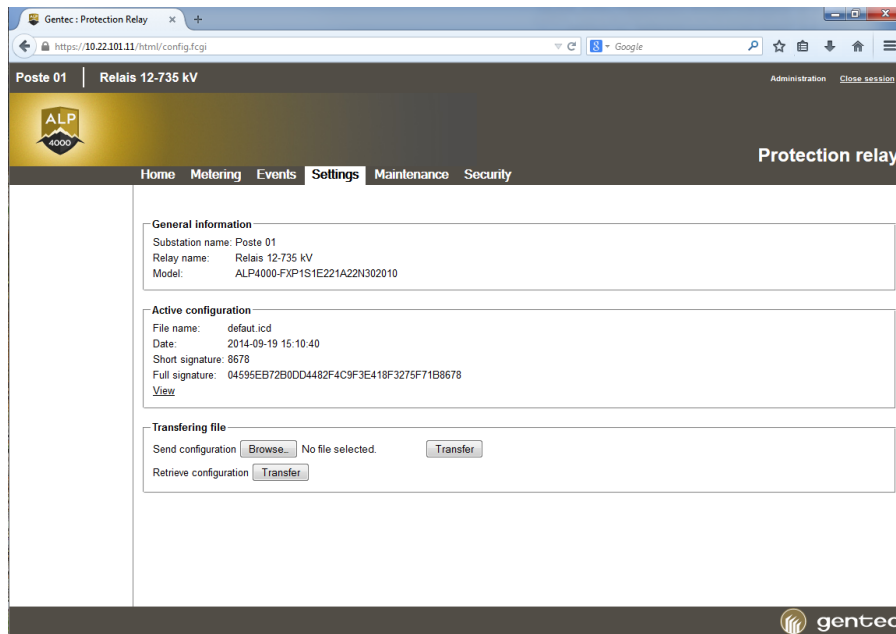


Figure 36 Web server Settings page

4.6.4. SOFTWARE UPDATE

The protection relay is delivered with the ordered software version. However, during the useful lifetime of the device, it will be possible to update the software as required via the web server. The software can be updated using the *Update* link of the *Maintenance* page. Only a user with an *Administration* access level can do this task. Users of other access levels can view the page, but cannot use the controls. To update the software, first browse for and select the desired file, and then click the *Transfer* button as shown on Figure 37.



IMPORTANT: After updating the software, the relay will automatically restart. So it is strongly recommended to perform this update only when the relay is decommissioned.

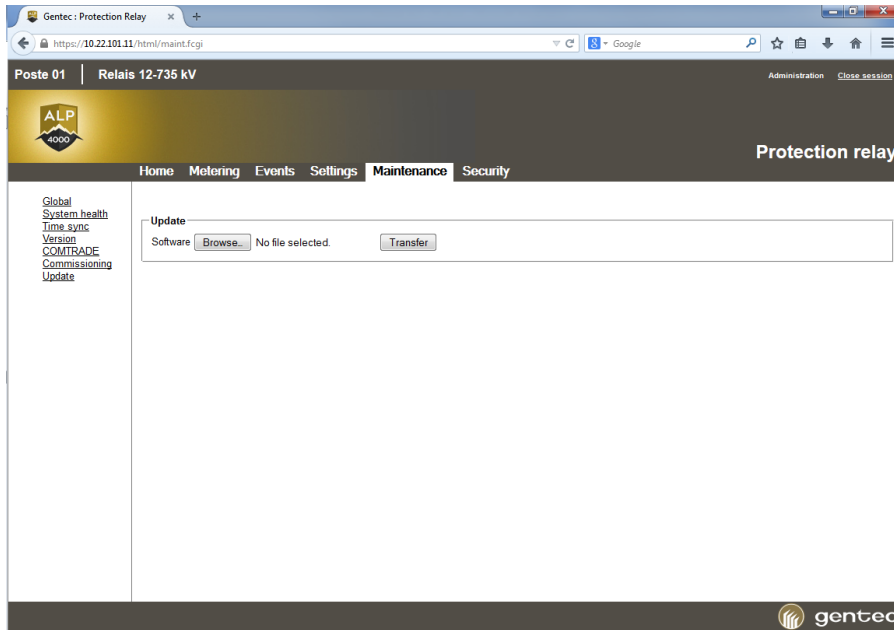


Figure 37 Web server Update page

4.6.5. BACK TO FACTORY DEFAULTS

It is possible to reset the relay back to its state at the time of delivery with the back to factory defaults functionality. To use this functionality, start by powering off the relay and then powering it back on. The acknowledge button must be continually held as soon as the relay starts to power back on. After a certain time, a confirmation page will be displayed on the LCD screen of the relay, as shown on Figure 38

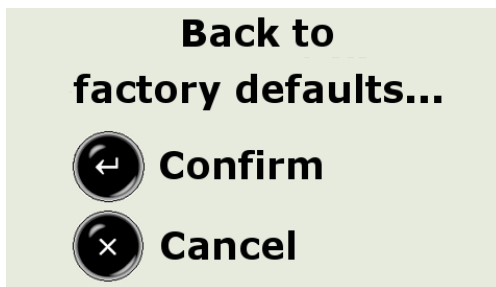


Figure 38 Confirmation page for the back to factory defaults functionality

5
SPECIFICATIONS

5 SPECIFICATIONS

AC CURRENT INPUTS

Quantity	6 three-phase groups
Nominal current	1 A or 5 A
Continuous maximum current	20 A
Measurable maximum current	40 A (1A nominal) 200 A (5A nominal)
Maximum current (1 sec thermal)	500 A
Maximum current (1 cycle thermal)	1250 Ac (peak)
Frequency response (-3dB)	1500 Hz
Burden	< 0.15 VA
Sampling	128 samples / cycle
Independent inputs	Dielectric strength between channels 2800 Vdc (1 min)

AC VOLTAGE INPUTS

Quantity	2 three-phase groups
Nominal voltage	70 V
Continuous maximum voltage	250 V
Measurable maximum voltage	300 V
Maximum voltage (10 sec thermal)	350 V
Frequency response (-3dB)	1500 Hz
Burden	< 0.15 VA
Sampling	128 samples / cycle
Independent inputs	Dielectric strength between channels 2800 Vdc (1 min)

DC INPUTS

Quantity	16
Nominal voltage	125 Vcc
Continuous maximum voltage	160 Vcc
Typical pickup voltage	88 Vcc @ 25°C
Typical dropout voltage	87 Vcc @ 25°C
Input impedance	33.3 kΩ @ 125 Vcc
Consumption per input	0.47 W @ 125 Vcc
Input filtering time	Between 4 and 8 ms (programmable) @ 60 Hz
Filtering precisio	10%
Sampling	128 samples / cycle
Independent inputs	Dielectric strength between channels 2800 Vdc (1 min)

OUTPUTS

Quantity	16
Operating nominal voltage	129 Vcc
Operating maximum voltage	160 Vcc
Minimum pickup voltage	60 Vcc
Continuous maximum current	5 A
Nominal closure power	30 A @ 129 Vcc
Nominal resistive cutoff power	0.3 A @ 129 Vcc
Nominal cutoff power	0.3 A @ 129 Vcc (L/R = 40 ms)
Pickup time	< 9 ms
Dropout time	< 4 ms
Number of mechanical operations	30 E 6 without load
Number of electrical operations	1 E 6 @ 129Vcc, I = 0.3A, L/R = 40ms
Independent outputs	Dielectric strength between channels 2800 Vdc (1 min)

HIGH-SPEED POWER OUTPUTS

Quantity	8
Operating nominal voltage	129 Vcc
Operating maximum voltage	160 Vcc
Minimum pickup voltage	60 Vcc
Continuous maximum current	10 A
Nominal closure power	30 A @ 129 Vcc
Nominal resistive cutoff power	10 A @ 129 Vcc
Nominal inductive cutoff power	10 A @ 129 Vcc (L/R = 40ms)
Pickup time	< 2 us
Dropout time	< 7 ms
Number of mechanical operations	30 E 6 without load
Number of electrical operations	54 000 @ 129Vcc, I = 10A, L/R = 40ms
Independent outputs	Dielectric strength between channels 2800 Vdc (1 min)

SYNCHRONIZATION

IRIG-B	Modulated IRIG-B (optional) or demodulated IRIG-B (model ALP-4100 only)
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COMMUNICATION

Front panel	1 10/100/1000Base-TX copper Ethernet port
Back panel	2 100Base-FX (1000BASE-SX optional) optical Ethernet ports
Communication protocols	HTTPS DNP3

POWER SUPPLY

Nominal voltage	125 Vdc	120 Vac
Power supply range	105 Vdc – 140 Vdc	85 Vac - 260 Vac @ 60 Hz
Power supply frequency range	-	47 to 67Hz
Typical power consumption	23 W	38 W

Maximum power consumption	30 W	50 W
Power supply metering accuracy	2%	
Time and date retention time after a power loss (powered by a supercapacitor)	10 days after power loss	
Inhibition threshold	90 Vdc	
Disinhibition threshold	92 Vdc	
Locking threshold	55 Vdc or Vac	
Unlocking threshold	60 Vdc or Vac	

MECHANICAL FOOTPRINT

Housing dimensions	482.6 mm (19.0 po) x 177.0 mm (7.0 po) x 310.2 mm (12.2 po)	
Weight	19.0 lbs (8.6Kg)	

ELECTROMAGNETIC COMPATIBILITY

DESCRIPTION	STANDARD	Level
Radiated emissions	CISPR 11 / CISPR 22	Class A
Conducted emissions	CISPR 22:2008	Class A
Electrostatic discharge immunity	CEI 61000-4-2:2008	±15 kV air ±8 kV contact
Radiated electromagnetic field immunity	CEI 61000-4-3:2006 A1:2008 A2:2010	20 V/m
Radiated electromagnetic field immunity	IEEE C37.90.2:2004	20 V/m
Electrical fast transient/burst immunity	CEI 61000-4-4:2004	±4 kV
Electrical fast transient/burst immunity	IEEE C37.90.1	±4 kV
Surge immunity	CEI 61000-4-5:2005	±4 kV L-PE ±2kV L-L POWER : ±2 kV L-PE ±1 kV L-L
Immunity to conducted disturbances	CEI 61000-4-6:2008	20V
Power frequency magnetic field immunity	CEI 61000-4-8:2009	100 A/m for 60s 1000 A/m for 3s (50Hz and 60Hz)
Pulsed magnetic field immunity	CEI 61000-4-9:1993 A1:2000	1000 A/m

Damped oscillatory magnetic field immunity	CEI 61000-4-10:1993 A1:2000	100 A/m for 2s (0.1MHz and 1MHz)
Voltage dips immunity	CEI 61000-4-11:2004 / CEI 61000-4-29:2000	0% for 52ms 40% for 200 ms 70% for 500 ms 0% for 5 cycles 40% for 12 cycles 70% for 30 cycles
Voltage interruptions on power supply voltage immunity	CEI 61000-4-11:2004 / CEI 61000-4-29:2000	DC 100% short-circuit for 5s DC 100% open circuit for 5s AC 100% for 5s
Gradual shut-down/start-ups	CEI 60255-26:2013	60s ramp 8h ramp
Immunity at the power frequency on the DC inputs	CEI 61000-4-16:2002	Inputs : 300 Vrms L-PE for 10s 60Hz 150 Vrms L-L for 10s 60Hz
Ripple on DC input power port immunity	CEI 61000-4-17:2009	15% at 105Vcc 15% at 125Vcc 15% at 140Vcc
Damped oscillatory wave immunity	CEI 61000-4-18:2006 A1:2011	2.5kV L-PE 1kV L-L IRIG-B : 1kV L-PE 0.5kV L-L 100kHz and 1MHz
Damped oscillatory wave immunity	IEEE C37.90.1:2002	2.5kV L-PE 2.5kV L-L

ATMOSPHERIC ENVIRONMENTAL CONDITIONS

DESCRIPTION	STANDARD	LEVEL
Dry heat – Functional	CEI 60068-2-2 :2007	+85°C, 16 hours
Cold – Functional	CEI 60068-2-1 :1990	-40°C, 16 hours
Dry heat – Storage	CEI 60068-2-2 :2007	+85°C, 16 hours
Cold – Storage	CEI 60068-2-1 :1990	-40°C, 16 hours
Cyclic temperatures	CEI 60068-2-14 :2009	-40°C to +85°C, 5 cycles
Damp heat, continuous	CEI 60068-2-78 :2012	+40°C, 10 days, 93% relative humidity
Damp heat, cyclic	CEI 60068-2-30 :2005	25°C to 55°C, 8 cycles, 95% relative humidity

MECHANICAL ENVIRONMENTAL CONDITIONS

DESCRIPTION	STANDARD	LEVEL
Behavior under vibrations and endurance (sinusoidal)	60255-21-1:1998	Class 1
Response to shocks, resistance to shocks and vibrations	60255-21-2 :1988	Class 1
Seismic tests	60255-21-3 :1993	Class 2

ENVIRONMENTAL OPERATING CONDITIONS

Housing protection	IP3X
Surge category	II
Pollution degree	2
Equipment class	1
Maximum elevation	< 2000 m
Maximum relative humidity	95% without condensation
Operating temperature	-40°C to +70°C

SECURITY

DESCRIPTION	STANDARD	LEVEL
Impulse voltage	60255-27:2013	5 kV, 0.5 J
Dielectric voltage	60255-27:2013	2800 Vcc Copper Ethernet port : 2250 Vcc
Insulation resistance	60255-27:2013	> 100M Ω after damp heat test (CEI 60068-2-78)
Protective bonding resistance	60255-27:2013	< 0.03 Ω
Thermal short time	60255-27:2013	4*In (20A) continuous 100*In (500A) for 1 s 1250Ac for 1 cycle

PROTECTION ELEMENTS

Phase/Neutral instantaneous overcurrent protection elements (50/50N)

Threshold	1A Nominal	5A Nominal
Range	0.05 – 20 A secondary in steps of 0.001 A	0.25 – 100 A secondary in steps of 0.001 A
Hysteresis	98% of threshold (at 25°C)	
Accuracy (steady state)	±3%, minimum of ±30 mA (at 25°C)	
Transient overreach	<2% up to X/R=240 (at 25°C)	
Pickup time	Total RMS	
10X threshold	<1.75 cycle (at 25°C)	
1.2X threshold	<2.5 cycles (at 25°C)	
Pickup time	Fundamental RMS	
10X threshold	<1 cycle (at 25°C)	
1.2X threshold	<2 cycles (at 25°C)	
Hold time³		
Range	0 – 100 s in steps of 1 ms	
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)	

Phase/Neutral definite time overcurrent protection elements (51 DT/51N DT)

Threshold	1A Nominal	5A Nominal
Range	0.05 – 20 A secondary in steps of 0.001 A	0.25 – 100 A secondary in steps of 0.001 A
Hysteresis	98% of threshold (at 25°C)	
Accuracy (steady state)	±3%, minimum of ±30 mA (at 25°C)	
Transient overreach	<2% up to X/R=240 (at 25°C)	
Pickup time	Total RMS	
10X threshold	<1.75 cycle (at 25°C)	
1.2X threshold	<2.5 cycles (at 25°C)	
Pickup time	Fundamental RMS	

³ Range and accuracy at 60Hz. If frequency tracking is enabled, this time will vary with the grid frequency.

10X threshold	<1 cycle (at 25°C)	
1.2X threshold	<2 cycles (at 25°C)	
Operating time³		
Range	0 – 100 s in steps of 1 ms	
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)	
Time overshoot	<1 cycle (at 25°C)	
Return time³		
Range	0 – 100 s in steps of 1 ms	
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)	
Hold time³		
Range	0 – 100 s in steps of 1 ms	
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)	
Phase/Neutral inverse time overcurrent protection elements (51 IT/51N IT)		
Threshold	1A Nominal	5A Nominal
Range	0.05 – 20 A secondary in steps of 0.001 A	0.25 – 100 A secondary in steps of 0.001 A
Hysteresis	98% of threshold (at 25°C)	
Accuracy (steady state)	±3%, minimum of ±30 mA (at 25°C)	
Transient overreach	3% (at 25°C)	
Pickup time	Total RMS	
10X threshold	<1.75 cycle (at 25°C)	
1.2X threshold	<2.5 cycles (at 25°C)	
Pickup time	Fundamental RMS	
10X threshold	<1 cycle (at 25°C)	
1.2X threshold	<2 cycles (at 25°C)	
Inverse time³		
Curves shapes	IEC Inverse IEC Very inverse IEC Extremely inverse IEC Long-Time Inverse IEEE Moderately inverse IEEE Very inverse IEEE Extremely inverse	
Curve dials	CEI : 0.05 – 1,1 in steps of 0.001 IEEE : 0.1 – 3,0 in steps of 0.001	

Accuracy (trip)	±1%, minimum of ±1.5 cycle (at 25°C)
Accuracy (return)	±1%, minimum of ±1.5 cycle (at 25°C)
Time overshoot	<1 cycle (at 25°C)
Response to time varying value of measured current	±3%, minimum of ±4,5 cycles (at 25°C)
Hold time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Transformer percent differential elements (87U/R)	
Current inputs	
Number of inputs	2 to 6
Tap range	0.7 – 174 in steps of 0.1
Restrained element	
Threshold	
Minimum threshold range	0.1 – 1 pu in steps of 0.001 pu
Slope 1 range	5 – 100 % in steps of 0.1 %
Slope 2 range	5 – 100 % in steps of 0.1 %
Accuracy	±5%, minimum of ±0.03 pu (at 25°C)
Harmonic detection (2nd, 4th et 5th)	
Range	5 – 100 % in steps of 0.1 %
Accuracy	±5%, minimum of ±0.03 pu (at 25°C)
Pickup time⁴	
Minimum	1.4 cycle (at 25°C)
Maximum	1.75 cycle (at 25°C)
Average	1.5 cycle (at 25°C)
Unrestrained element	
Threshold range	5 – 20 pu in steps of 0.001 pu
Accuracy	±5%, minimum of ±0.03 pu (at 25°C)
Pickup time	

⁴ The specified pickup times are valid for a minimum threshold (OpMin) value greater than 0.5 pu.

Minimum	0.6 cycle (at 25°C)
Maximum	1.6 cycle (at 25°C)
Average	1.1 cycle (at 25°C)
Volts per hertz protection element (24)	
Threshold	
Range	0.8 – 3 pu in steps of 0.001 pu
Hysteresis	98% of threshold (at 25°C)
Accuracy (steady state)	±1% (at 25°C)
Pickup time	
1.2X threshold	< 4.5 cycles
2X threshold	< 2.75 cycles
Operating time³	
Range	0 – 900 s in steps of 1 ms
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Operating time³	
Curves shapes	Curve 1 Curve 2 Curve 3
Curve dials	0.05-100 in steps of 0.001
Accuracy (trip)	±1%, minimum of ±1.5 cycle (at 25°C)
Return time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	±1%, minimum of ±1.5 cycle (at 25°C)
Hold time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Undervoltage protection element (27)	
Threshold	
Range	1 – 300 V in steps of 0.001 V
Hysteresis	102% of threshold (at 25°C)

Accuracy (steady state)	$\pm 3\%$, minimum of ± 2.1 V (at 25°C)
Pickup time	Total RMS
0.1X threshold	<1.9 cycle (at 25°C)
0.8X threshold	<2.5 cycles (at 25°C)
Pickup time	Fundamental RMS
0.1X threshold	<1 cycle (at 25°C)
0.8X threshold	<1.75 cycles (at 25°C)
Operating time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	$\pm 0.1\%$, minimum of ± 0.125 cycle (at 25°C)
Time overshoot	<1 cycle (at 25°C)
Hold time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	$\pm 0.1\%$, minimum of ± 0.125 cycle (at 25°C)
Overvoltage protection element (59)	
Pickup	
Range	1 – 300 V in steps of 0.001 V
Hysteresis	98% of threshold (at 25°C)
Accuracy (steady state)	$\pm 3\%$, minimum of ± 2.1 V (at 25°C)
Pickup time	Total RMS
10X threshold	<1.9 cycle (at 25°C)
1,2X threshold	<2.5 cycles (at 25°C)
Pickup time	Fundamental RMS
10X threshold	<1 cycle (at 25°C)
1.2X threshold	<1.75 cycles (at 25°C)
Operating time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	$\pm 0.1\%$, minimum of ± 0.125 cycle (at 25°C)
Hold time³	
Range	0 – 100 s in steps of 1 ms

Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Voltage peak detector (VPD)	
Threshold	
Range	0.250 – 425 V in steps of 0.001 V
Accuracy	±0.1%, minimum of ±10 mV (at 25°C)
Hold time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Under/overfrequency protection elements (81)	
Threshold	
Range	40 – 75 Hz in steps of 0.001 Hz
Accuracy	±0.04%, minimum of ±25 mHz (at 25°C)
Pickup time	
Average	<6 cycles (at 25°C)
Maximum	<12 cycles (at 25°C)
Operating time³	
Range	0 – 900 s in steps of 1 ms
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Hold time³	
Range	0 – 100 s in steps of 1 ms
Accuracy	±0.1%, minimum of ±0.125 cycle (at 25°C)
Frequency rate-of-change protection element (81R)	
Threshold	
Range	±0.1 à ±10 Hz/s in steps of 0.01 Hz
Accuracy	±3%, minimum of ±5 mHz/s (at 25°C)

CONTROL ELEMENTS

Phase directional element (DIR)

Minimum voltage threshold

Range	1 – 300 V in steps of 0.001 V
Hysteresis	98% of threshold (at 25°C)
Accuracy	±3%, minimum of ±2.1 V (at 25°C)

Minimum current threshold

Range	10% of the nominal current (1A or 5A)
Hysteresis	98% of threshold (at 25°C)
Accuracy	±3%, minimum of ±30 mA (at 25°C)

Element characteristic angle

Range	0 – 359.999°
Accuracy	± 2°

Operating time

Blocking	< 0.75 cycle (at 25°C)
Tripping	< 1.75 cycles (at 25°C)

Loss of voltage element (LOV)

Pickup time

Detection	< 7.6 ms
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Dropout time

Detection	< 27.9 ms
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SOFTWARE FEATURES

Logic equations

Number of logic equations 50

Logic elements

Element types Logic equation, binary point, logic operator

Total quantity 500

Logic operators AND, OR, NOT, XOR

RS latches

Number of latches 15

Timers

Number of timers 15

Pickup time

Range 0 – 100 s

Accuracy 2% of setting (at 25°C)

Dropout time

Range 0 – 100 s

Accuracy 2% of setting (at 25°C)

Chronological events recorder

Number of events 1000

Timestamp accuracy 1 ms

Oscillographs

Number of oscillographs 10

Sampling period

Raw data 128 samples/cycle

Filtered data 16 samples/cycle

Detection levels Positive/Rising, Negative/Falling, Both

Supported formats IEEE Std C37.111-1999, IEEE Std C37.111-2013

METERING

Note : Accuracy measured at 25 °C and at nominal frequency

Current

Total RMS 0.5 – 100 A : 0.2% ± 10mA

Phasor

Magnitude 0.5 – 100 A : 0.2% ± 10mA

Angle 0.5 – 100 A : ±1°

Symmetrical components

Magnitude 0.5 – 100 A : 0.2% ± 10mA

Angle 0.5 – 100 A : ±1°

Voltage

Total RMS 5 – 300 V : 0.1% ± 12mV

Phasor

Magnitude 5 – 300 V : 0.1% ± 12mV

Angle 5 – 300 V : ±1°

Symmetrical components

Magnitude 5 – 300 V : 0.1% ± 12mV

Angle 5 – 300 V : ±1°

Frequency

Nominal frequency 60 Hz

Accuracy ±0.001 Hz (at 60 Hz)

Frequency measurement

Range 30 – 90 Hz

Frequency tracking

Range 40 – 75 Hz

6

PROTECTION ELEMENTS

6 PROTECTION AND CONTROL ELEMENTS

This chapter describes the operation and settings of the different protection and control elements available in the relays of the ALP-4000 series. The chapter is divided in five main sections: current protection elements, differential protection elements, voltage protection elements, frequency protection elements and control elements.

6.1. CURRENT PROTECTION ELEMENTS

6.1.1. INSTANTANEOUS OVERCURRENT (50/50N)

The phase instantaneous overcurrent protection element (50) compares the measured operating quantity of a current input to the threshold. For the neutral instantaneous overcurrent protection element (50N), the threshold is compared to the zero sequence of the three-phase current input or to one of the single-phase inputs. Threshold is expressed in secondary values.

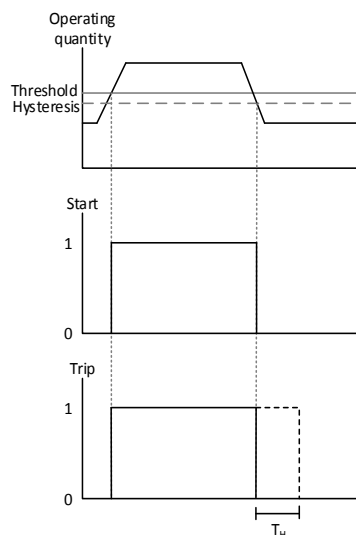


Figure 39 Timing diagram for the binary points of the instantaneous overcurrent protection elements (50/50N)

Figure 39 shows the timing diagram for the start and trip binary points. If the measured operating quantity of a phase is greater than the threshold, the trip and start binary points of this phase switch from 0 to 1. The start binary point switches back to 0 only when the operating quantity is below the hysteresis of the threshold. If the hold time (T_H) setting equals zero, the trip binary point switches back to 0 at the same time as the start binary point. Otherwise, there is a delay equivalent to T_H between the start binary point and the trip binary point falling to zero.

10 instances of the 50 protection element and 6 instances of the 50N protection element are configurable in the relay. Figure 40 shows the phase instantaneous overcurrent protection element logical diagram with the *Component* setting equal to *Three-phase*. Figure 41 shows the zero sequence instantaneous overcurrent protection element logical diagram with the *Component* setting equal to *Zero sequence*. For both elements, when the *Component* setting equals *Phase A/B/C*, the logical diagram corresponds to the one found on Figure 41. Table 19 lists the available settings for these protection elements.

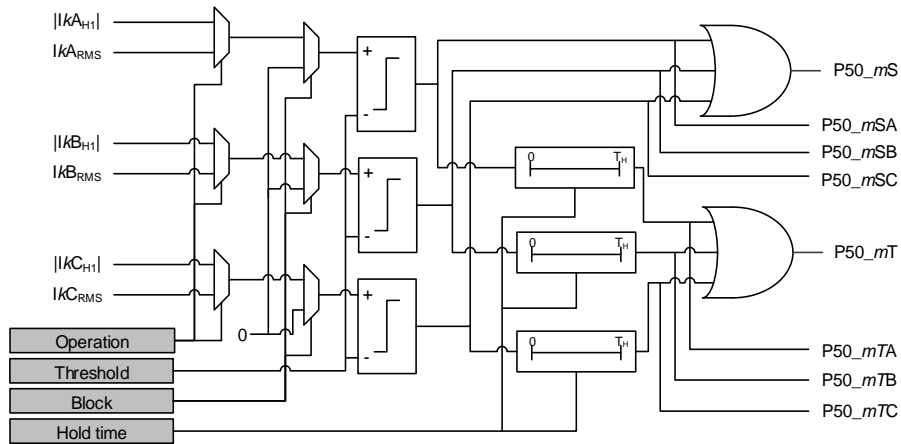


Figure 40 Phase instantaneous overcurrent protection element

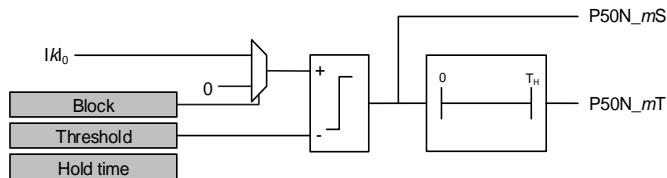


Figure 41 Neutral instantaneous overcurrent protection element

SETTING	RANGE	DESCRIPTION
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Block	Binary points	Binary point blocking the input
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Input	None; configured I/SI	Current or summed input used
Threshold	0.05-20 A (1A nominal) 0.25-100 A (5A nominal)	Start threshold, secondary
Hold time	0-100 s	Time between the start binary point falling to 0 and the trip binary point falling to 0
Operation	Total RMS; Fundamental RMS	Measured operating quantity evaluation method
Component (50)	Three-phase; Phase A; Phase B; Phase C	Measured operating quantity type
Component (50N)	Zero sequence; Phase A; Phase B; Phase C	Measured operating quantity type

Table 19 Instantaneous overcurrent protection elements settings (50/50N)

6.1.2. DEFINITE TIME OVERCURRENT (51 DT/51N DT)

The phase definite time overcurrent protection element (51 DT) compares the measured operating quantity of a Current input to the threshold. For the neutral definite time overcurrent protection element (51N DT), the threshold is compared to the zero sequence of the three-phase current input or to one of the single-phase inputs. Threshold is expressed in secondary values.

Figure 42 shows the timing diagram for the start and trip binary points. If the measured operating quantity of a phase is greater than the threshold, the start binary point of this phase switches to logic state 1. When it falls below the hysteresis of the threshold, the start binary point immediately switches back to logic state 0.

If the threshold is exceeded for a period of time shorter than the operating time setting, the behavior of the internal counter depends of the return type setting. When the return is instantaneous, the operating time internal counter is set to 0 as soon as the operating quantity falls below the hysteresis of the threshold. However, when the return is set to *Hold*, the internal counter value is memorized for a time period determined by the return time setting. Thus, if the operating quantity exceeds the threshold again during that time period, the internal counter does not start counting from zero. If the threshold is exceeded for a period of time longer than the operating time setting, the trip binary point switches to logic state 1. When the operating quantity falls below the hysteresis of the threshold, it is reset to zero after a period of time equal to the hold time setting.

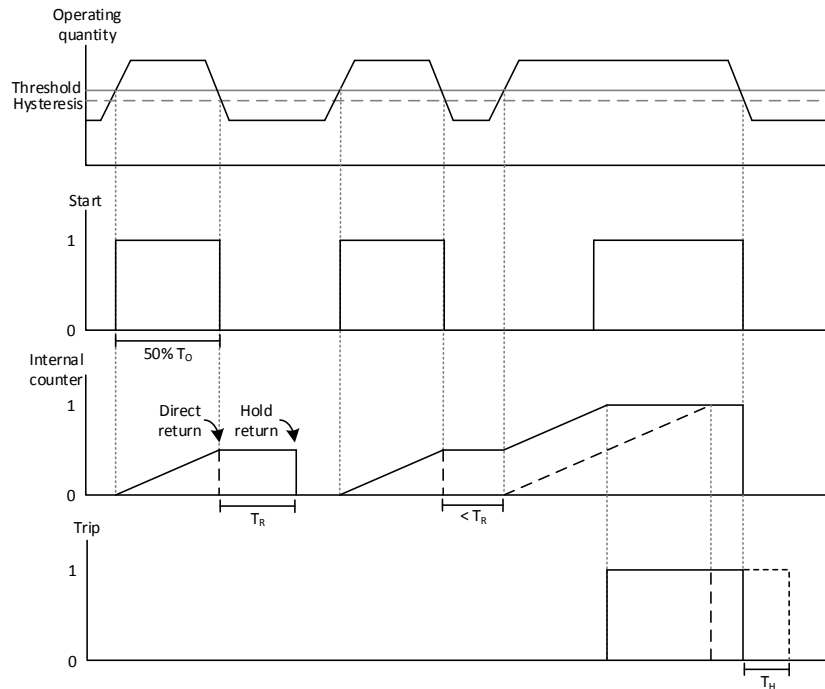


Figure 42 Timing diagram of the binary points of the definite time overcurrent protection elements (51 DT/51N DT)

10 instances of the 50 protection element and 6 instances of the 50N protection element are configurable in the relay. Figure 44 shows the phase definite time overcurrent protection element logical diagram with the *Component* setting equal to *Three-phase*. Figure 43 shows the zero sequence definite time overcurrent protection element logical diagram with the *Component* setting equal to *Zero sequence*. For both elements, when the *Component* setting equals *Phase A/B/C*, the logical diagram corresponds to the one found on Figure 43. Table 20 lists the available settings for these protection elements.

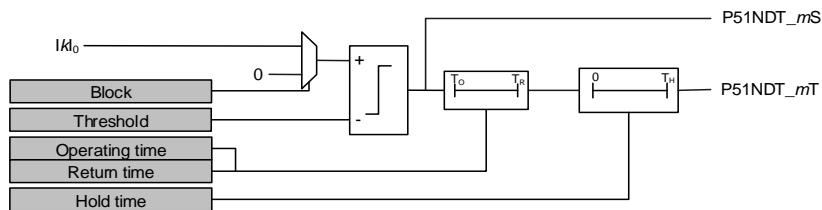


Figure 43 Zero sequence definite time overcurrent protection element

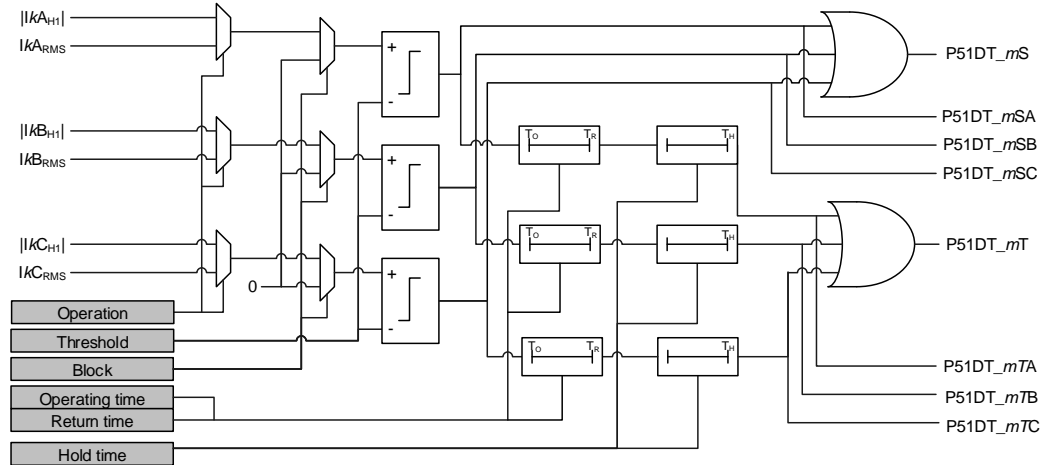


Figure 44 Phase definite time overcurrent protection element

SETTING	RANGE	DESCRIPTION
Block	Binary points	Binary point blocking the input
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Hold	Internal counter return type when start binary point falls to 0
Input	None; configured I/SI	Current or summed input used
Threshold	0.05-20 A (1A nominal) 0.25-100 A (5A nominal)	Start threshold, secondary
Hold time	0-100 s	Time between the start binary point falling to 0 and the trip binary point falling to 0
Operating time	0-100 s	Time between the start binary point rising to 1 and the trip binary point rising to 1
Return time	0-100 s	Trip binary point internal counter reset delay when start binary point falls to 0
Operation	Total RMS; Fundamental RMS	Measured operating quantity evaluation method
Component (50)	Three-phase; Phase A; Phase B; Phase C	Measured operating quantity type
Component (50N)	Zero sequence; Phase A; Phase B; Phase C	Measured operating quantity type

Table 20 Definite time overcurrent protection elements settings (51 DT/51N DT)

6.1.3. INVERSE TIME OVERCURRENT (51 IT/51N IT)

The phase inverse time overcurrent protection element (51 IT) compares the measured operating quantity of a Current input to the threshold. For the neutral inverse time overcurrent protection element (51N IT), the threshold is compared to the zero sequence of the three-phase current input or to one of the single-phase inputs. Threshold is expressed in secondary values.

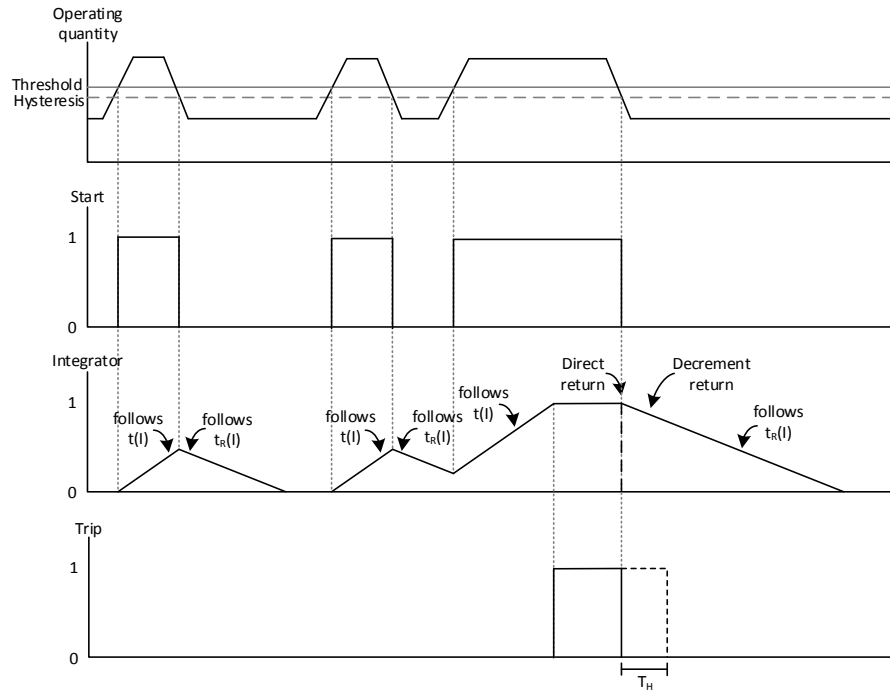


Figure 45 Timing diagram of the binary points of the inverse time overcurrent protection elements (51 IT/51N IT)

Figure 45 shows the timing diagram for the start and trip binary points. If the measured operating quantity of a phase is greater than the threshold, the start binary point of this phase switches to logic state 1. The trip binary point switches to logic state 1 only if the measured operating quantity is greater than the threshold for a period of time determined by the following equation:

$$t(I) = \text{Dial} \left[\frac{k}{\left(\frac{I}{\text{StrVal}} \right)^\alpha - 1} + c \right] \quad (1)$$

Where I is the operating quantity, in amperes,
 StrVal is the threshold, in amperes,
 Dial is the time multiplier, and
 k , α , and c are inverse curve parameters.

When the measured operating quantity falls below the hysteresis of the threshold, the start binary point immediately switches back to logic state 0. If the trip binary point equals logic state 1, it switches back to logic state 0 when the hold time elapses. If the operating time is not elapsed, the integrator value at the moment the measured operating quantity falls below the threshold decrements according to the return time determined by equation (2). If the operating time is elapsed, the behavior of the integrator depends on the return type setting. If the return type is set to *Direct*, the integrator value is immediately reset to 0. If the return type is set to *Decrement*, the integrator value decrements according to the return time determined by the following equation :

$$t_r(I) = \text{Dial} \left[\frac{t_r}{1 - \left(\frac{I}{\text{StrVal}}\right)^\beta} \right] \quad (2)$$

Where I is the operating quantity, in amperes,
 StrVal is the threshold, in amperes,
 Dial is the time multiplier, and
 t_r and β are inverse curve parameters.

It is important to note that in the protection relay, the ratio $\left(\frac{I}{\text{StrVal}}\right)$ is capped at a value of 30 for the operating and return times computations. The inverse time curve shapes available in the relay come from the IEC and IEEE standards. They are described on Table 21. Figures 46 to 57 show the curves for different dial values. Each curve has a zoomed in version for the small $\left(\frac{I}{\text{StrVal}}\right)$ ratios.

COURBE	k	α	c	t_r	β
IEC A (C1) - Inverse	0.14	0.02	0	13.5	2
IEC B (C2) – Very inverse	13.5	1	0	47.3	2
IEC C (C3) – Extremely inverse	80	2	0	80	2
IEC C4 – Inverse long time	120	1	0	120	1
IEEE Moderately inverse	0.0515	0.02	0.1140	4.85	2
IEEE Very inverse	19.61	2	0.491	21.6	2
IEEE Extremely inverse	28.2	2	0.1217	29.1	2

Table 21 Inverse time curve shapes available in the inverse time protection elements (51 IT/51N IT)

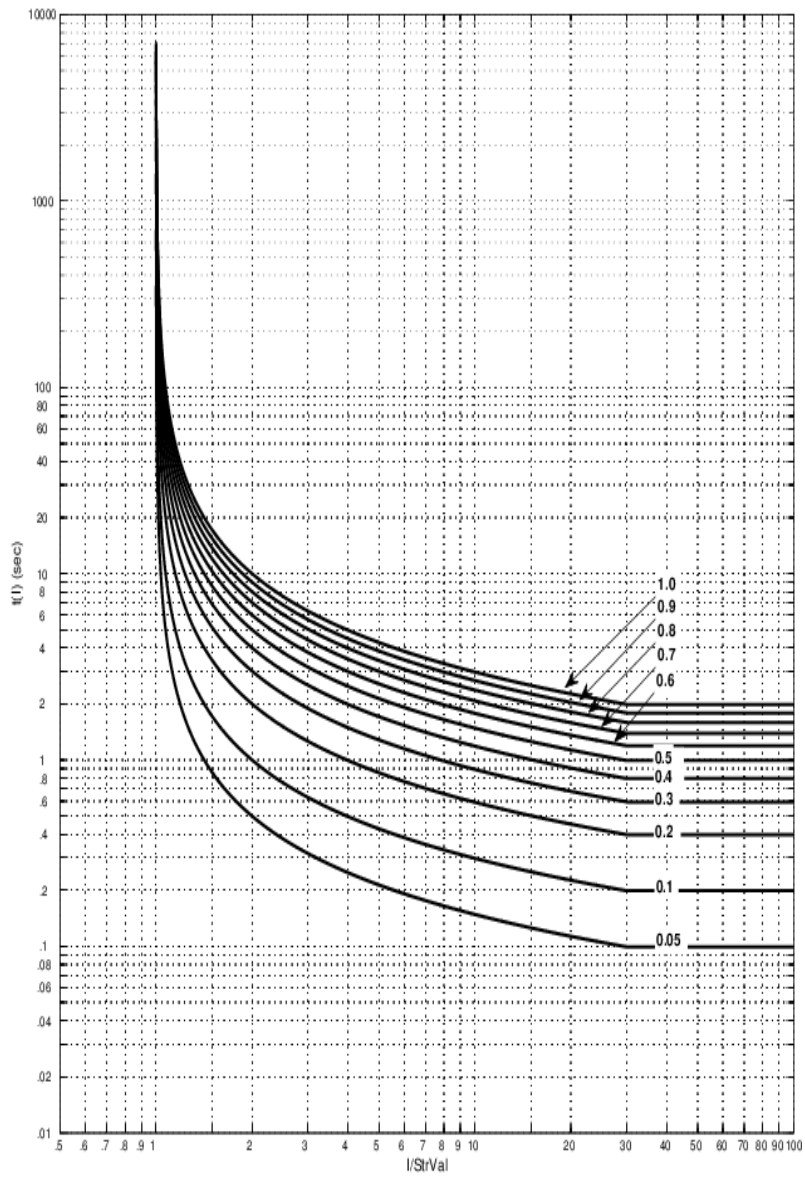


Figure 46 CEI A (C1) - Inverse

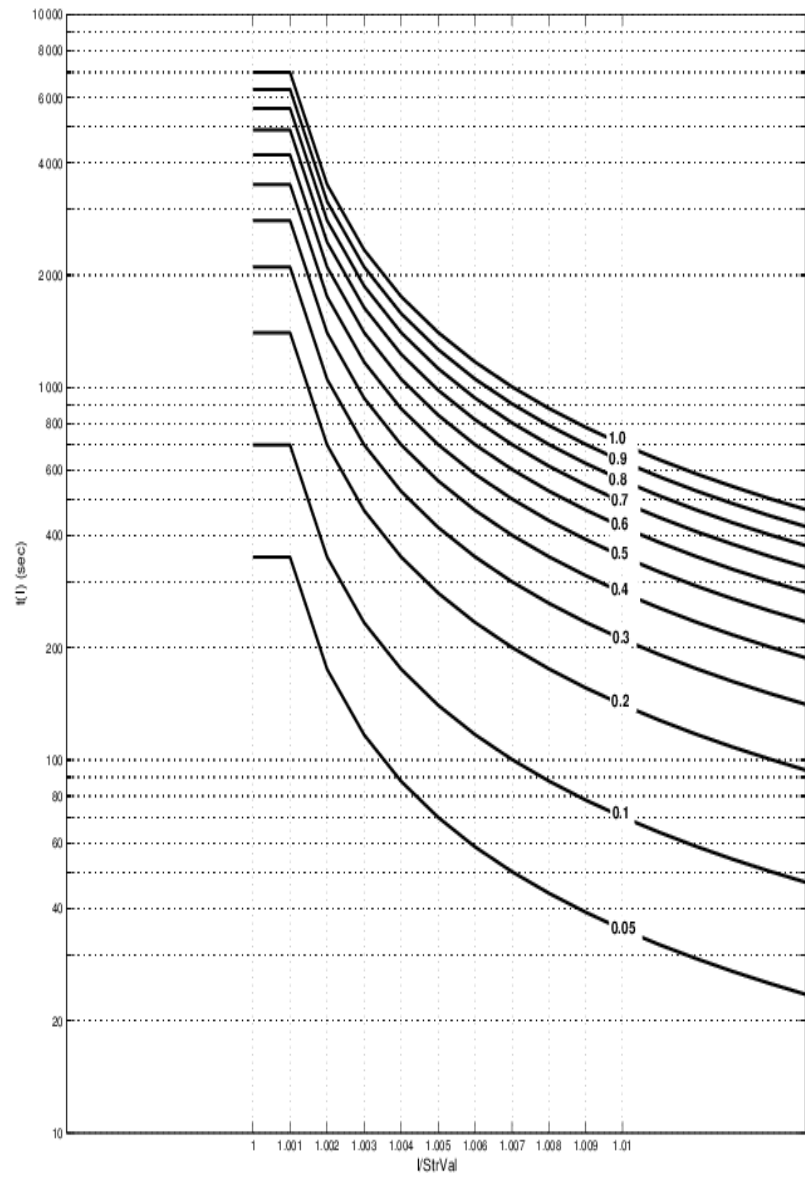


Figure 47 CEI A (C1) - Inverse - Zoom in

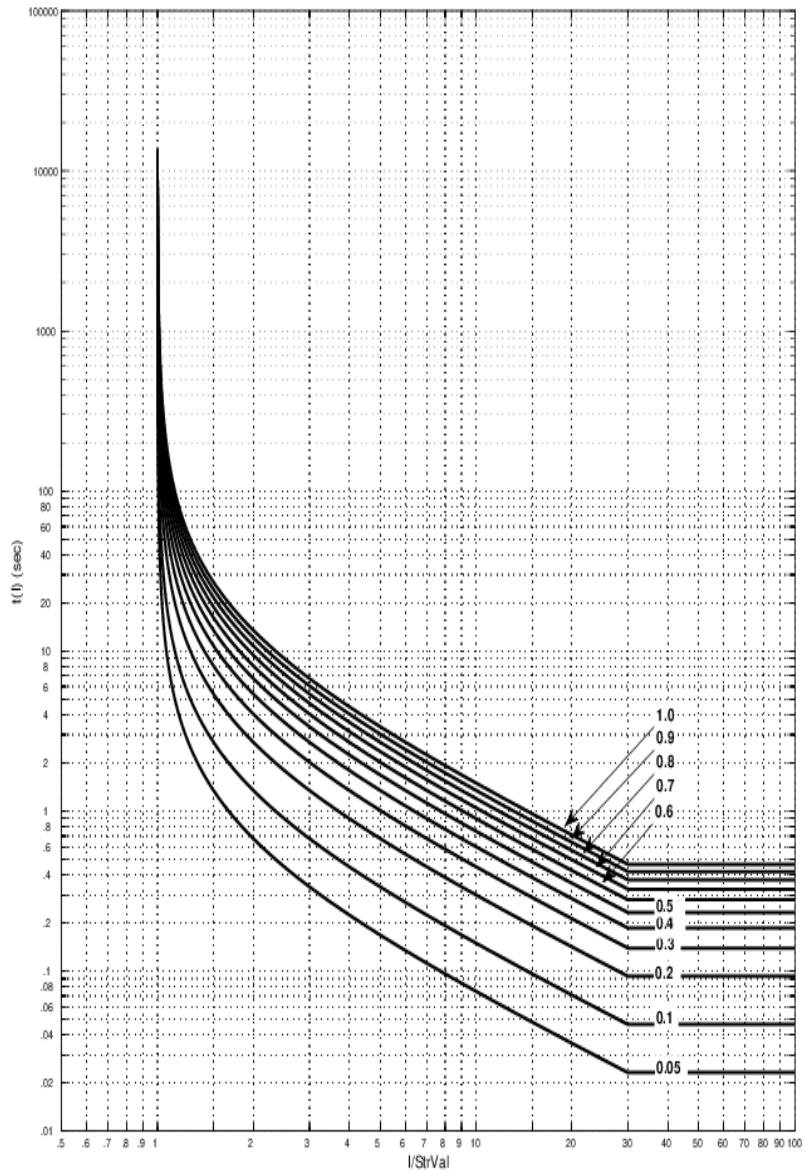


Figure 48 CEI B (C2) –Very inverse

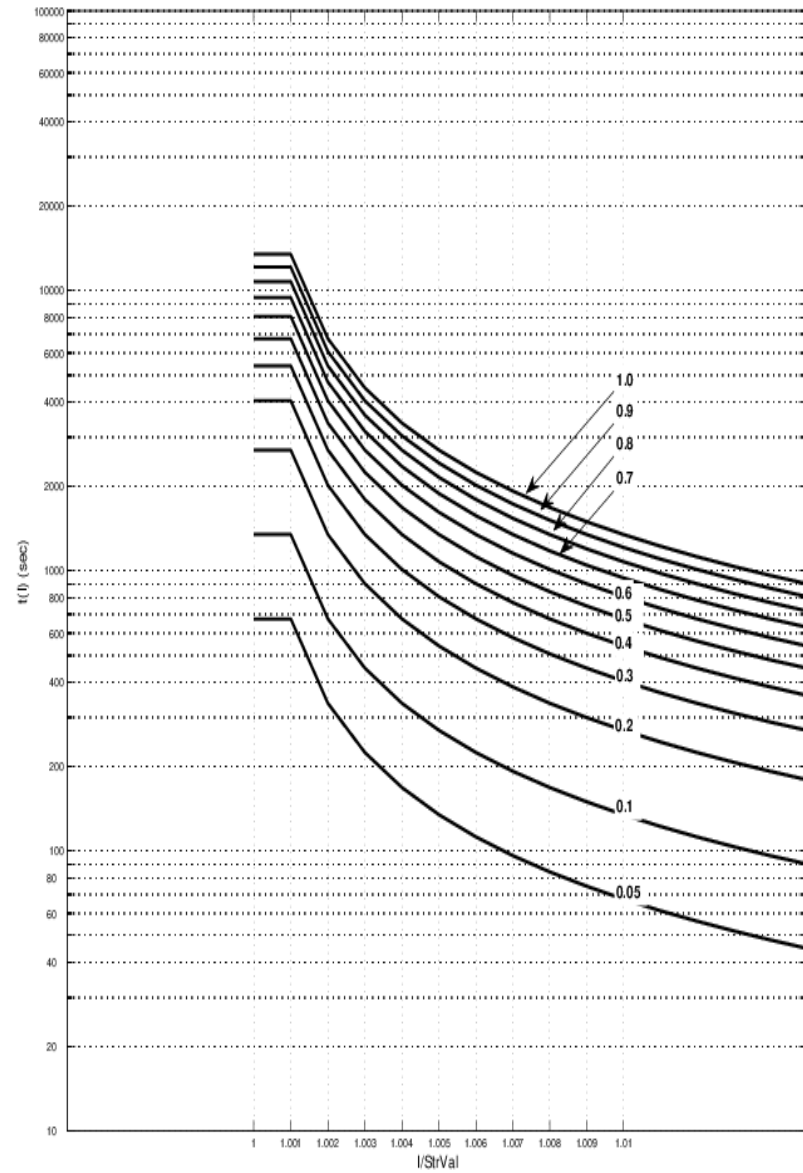


Figure 49 CEI B (C2) – Very inverse – Zoom in

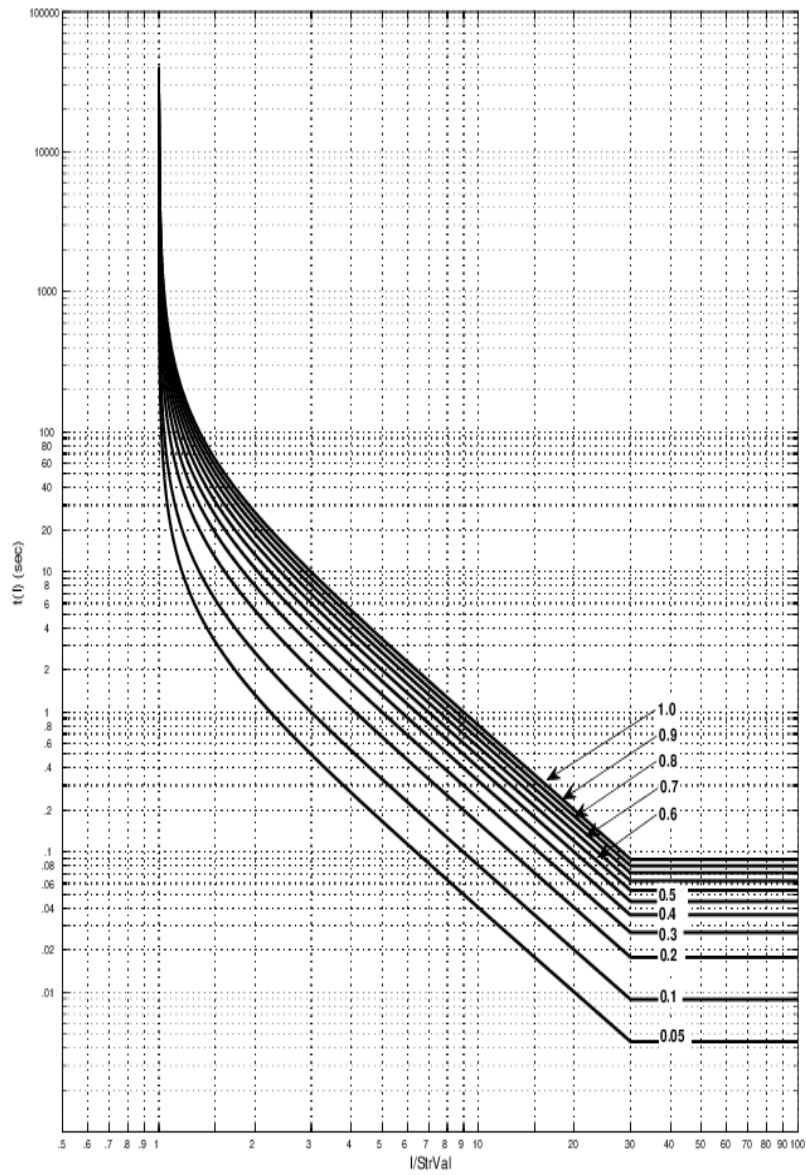


Figure 50 CEI C (C3) – Extremely inverse –

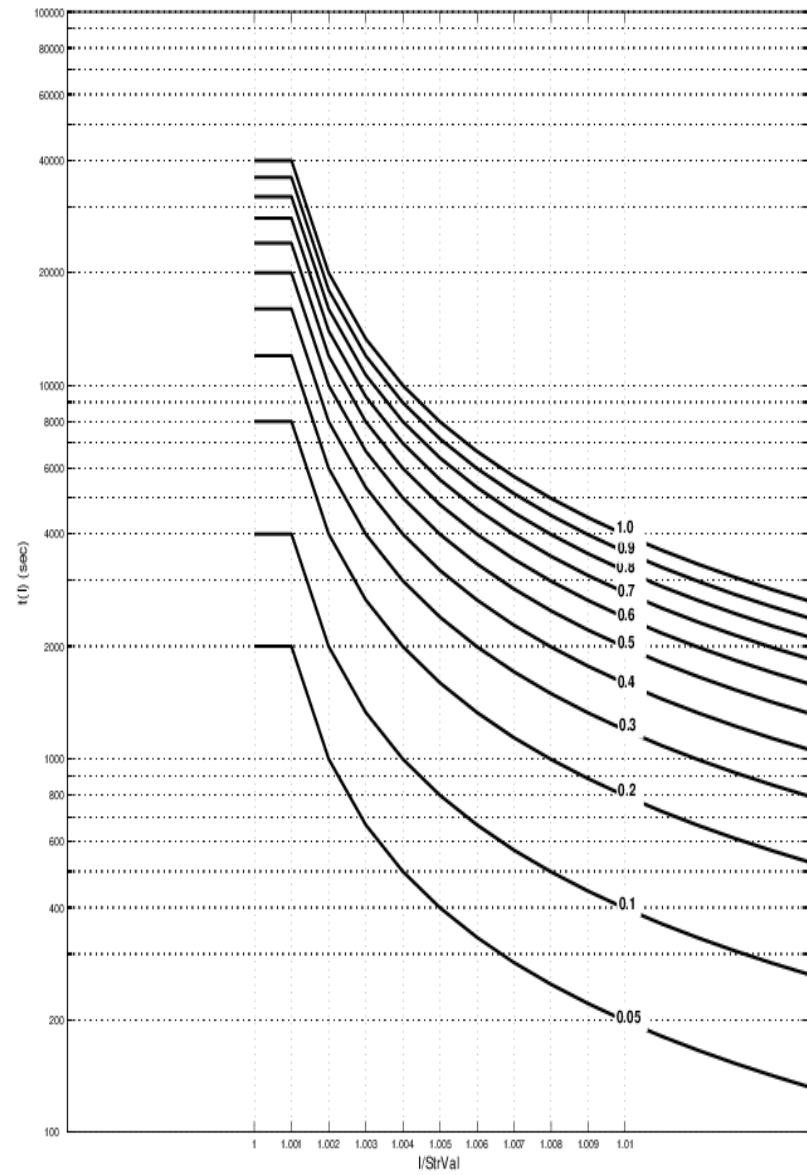


Figure 51 CEI C (C3) – Extremely inverse – Zoom in

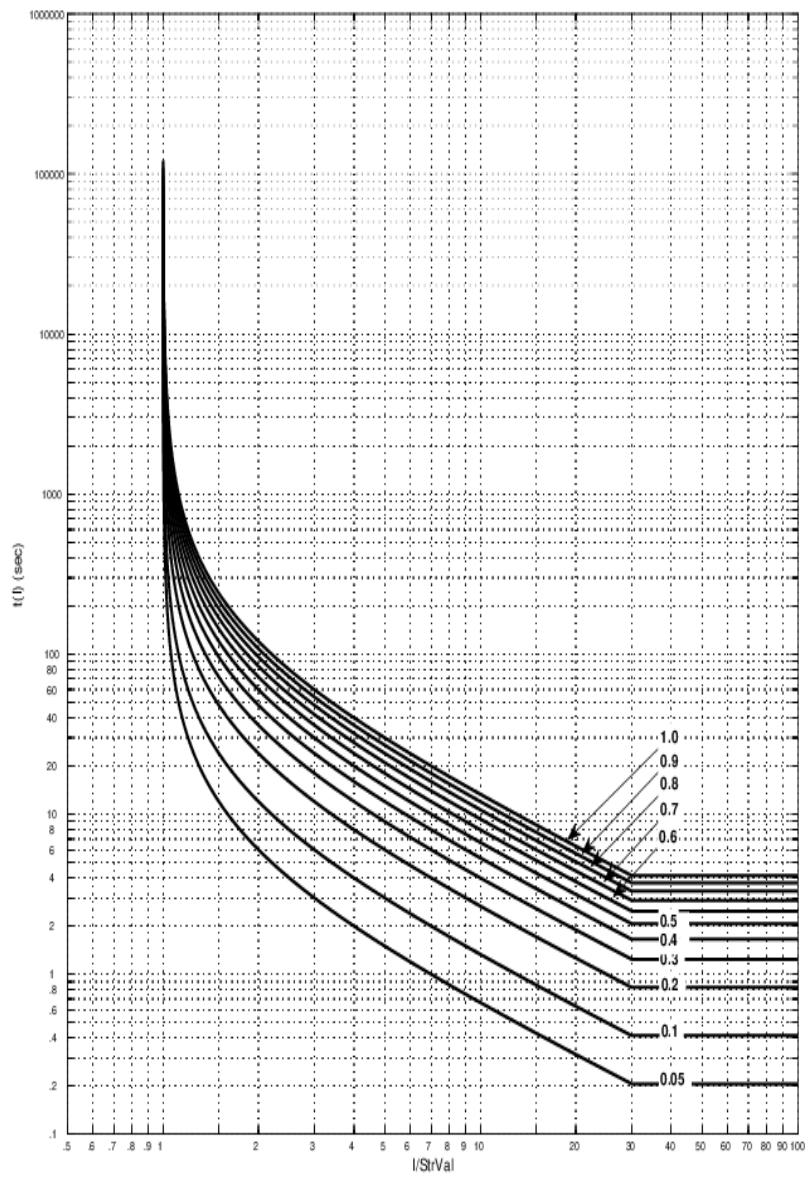


Figure 49 CEI C4 – Inverse long time

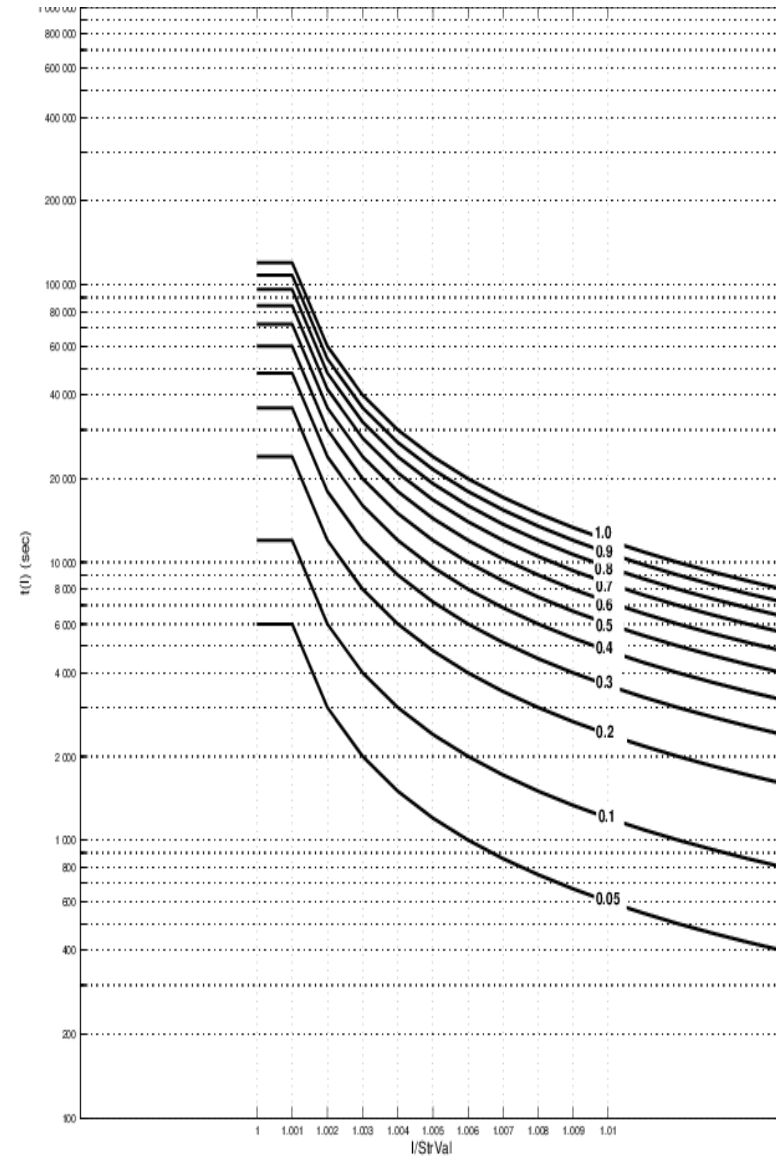


Figure 50 CEI C4 – Inverse long time – Zoom in

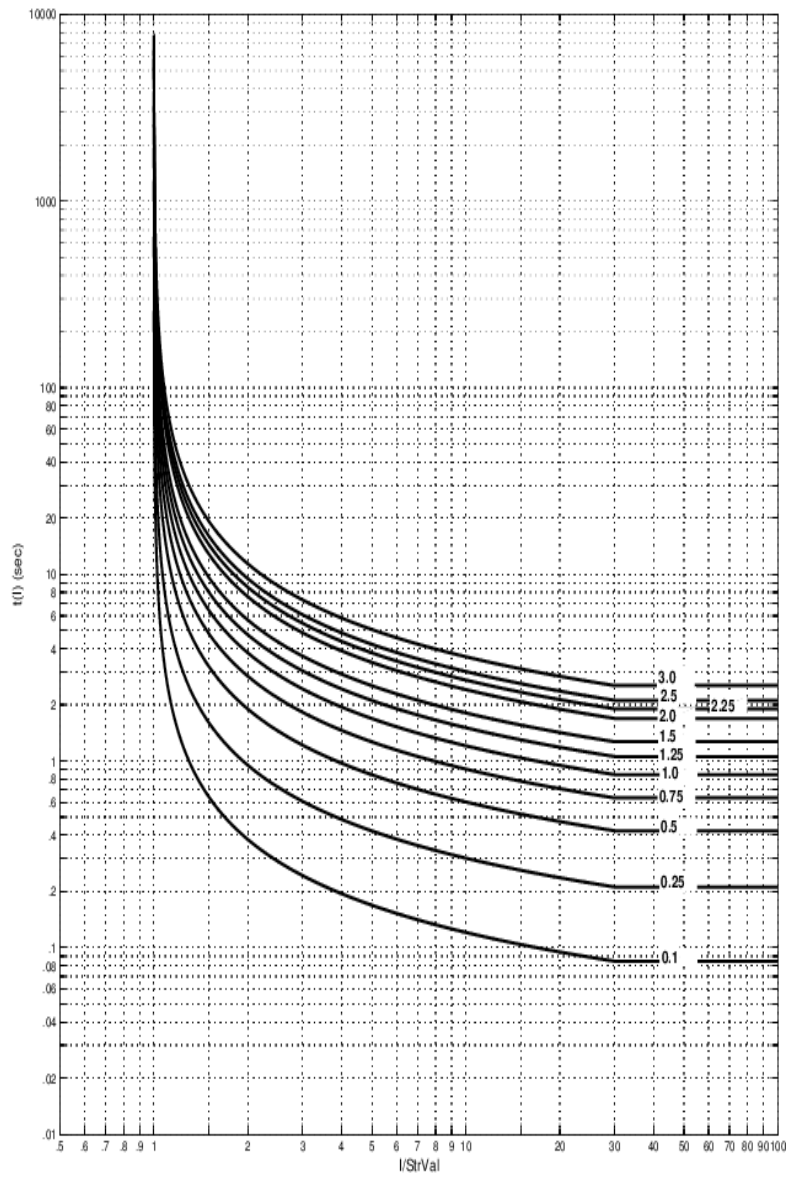


Figure 52 IEEE Moderately inverse

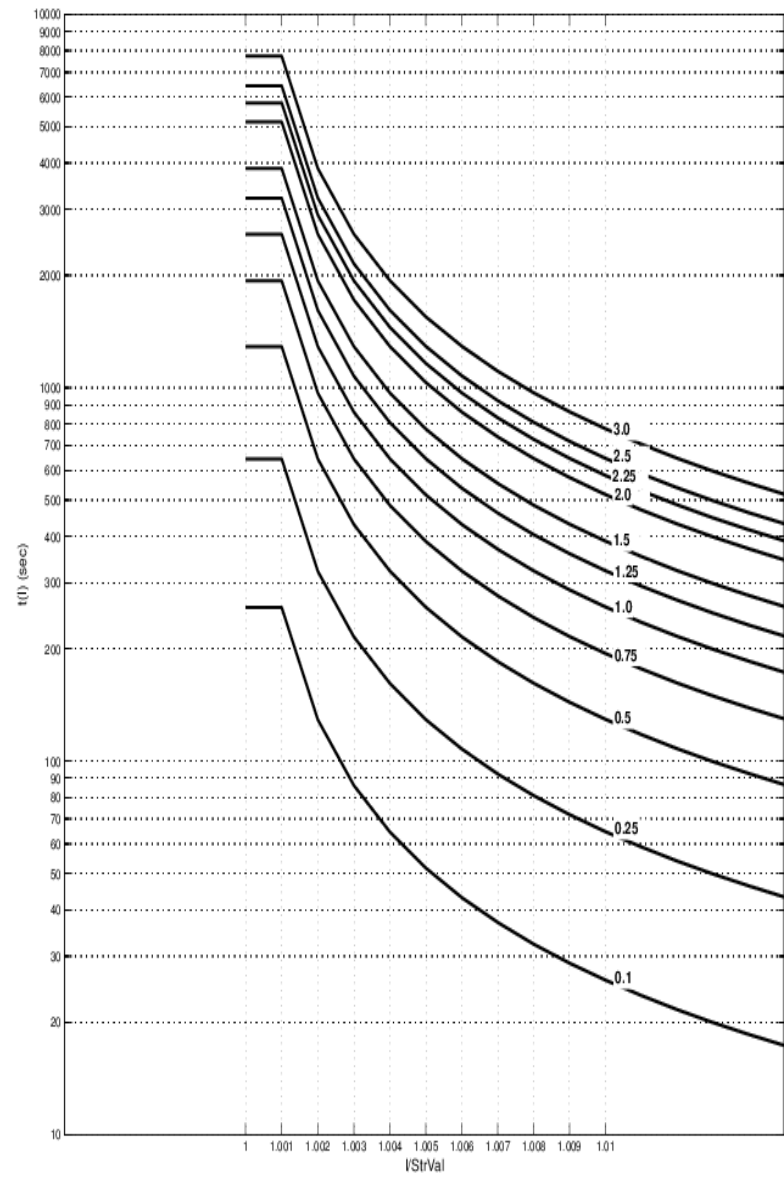


Figure 53 IEEE Moderately inverse – Zoom in

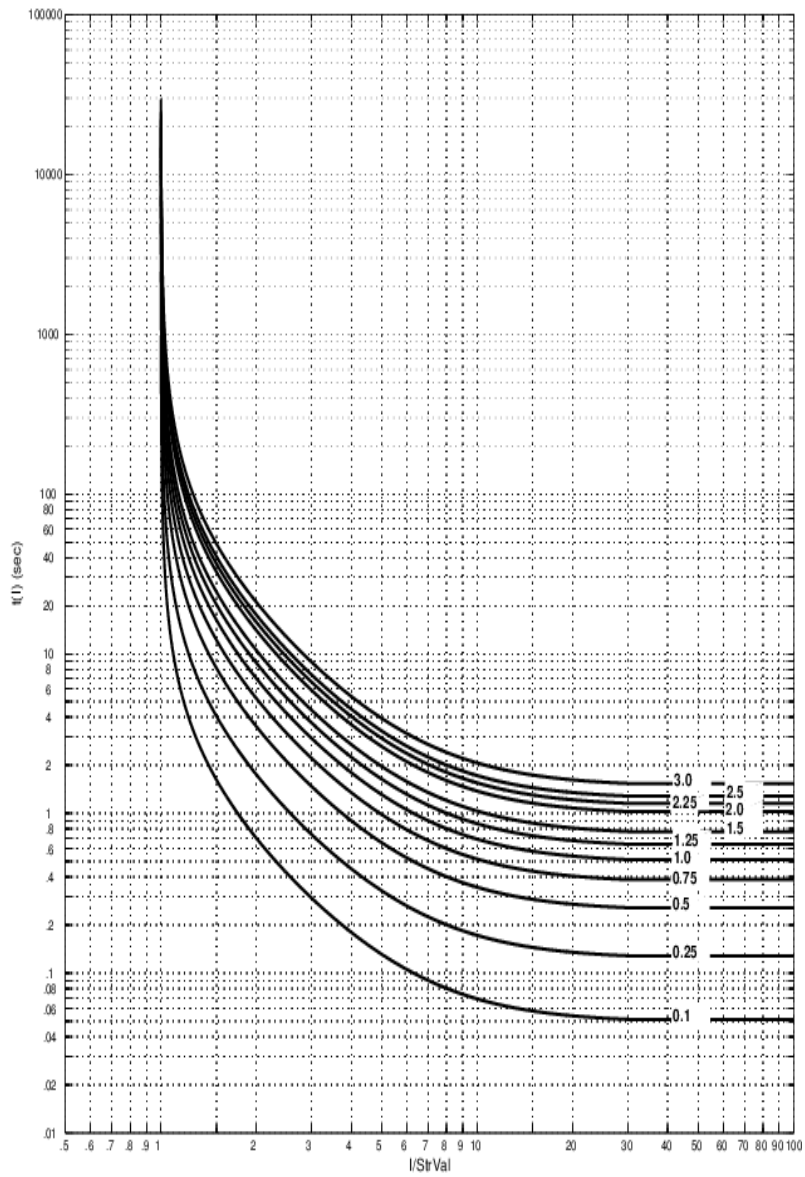


Figure 54 IEEE Very inverse

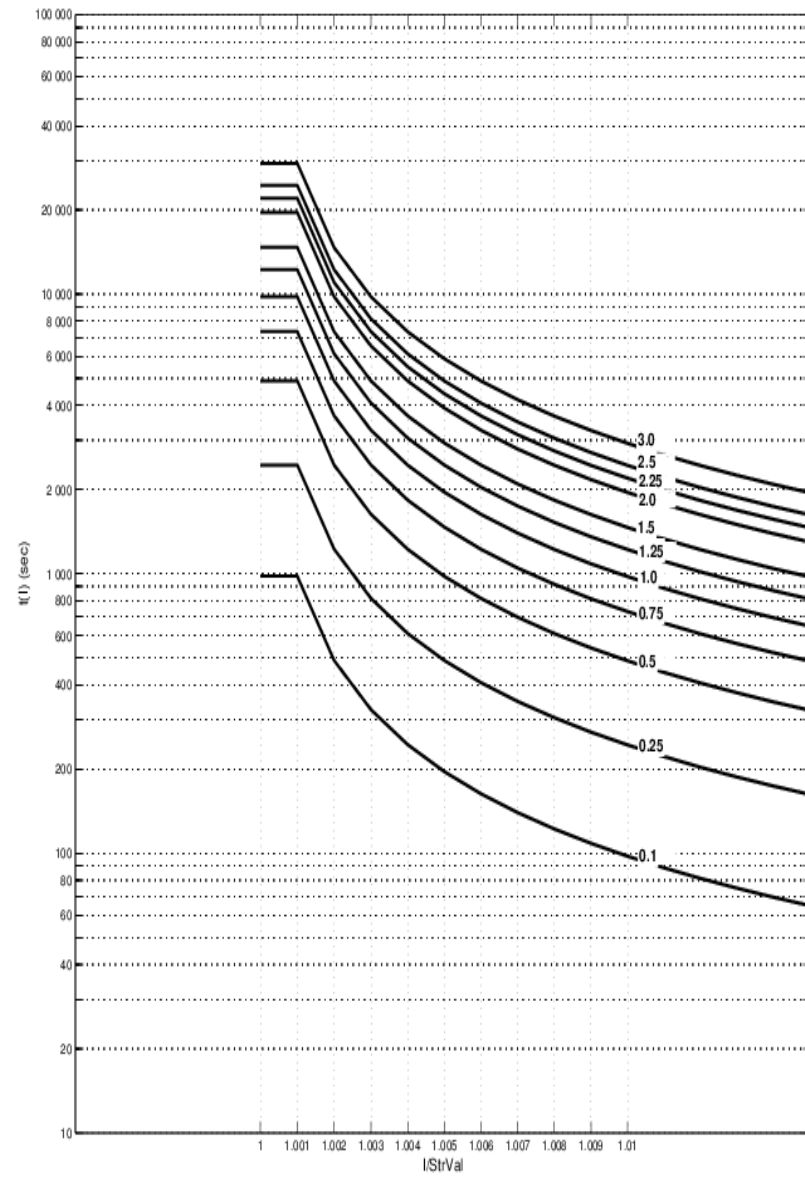


Figure 55 IEEE Very inverse -- Zoom in

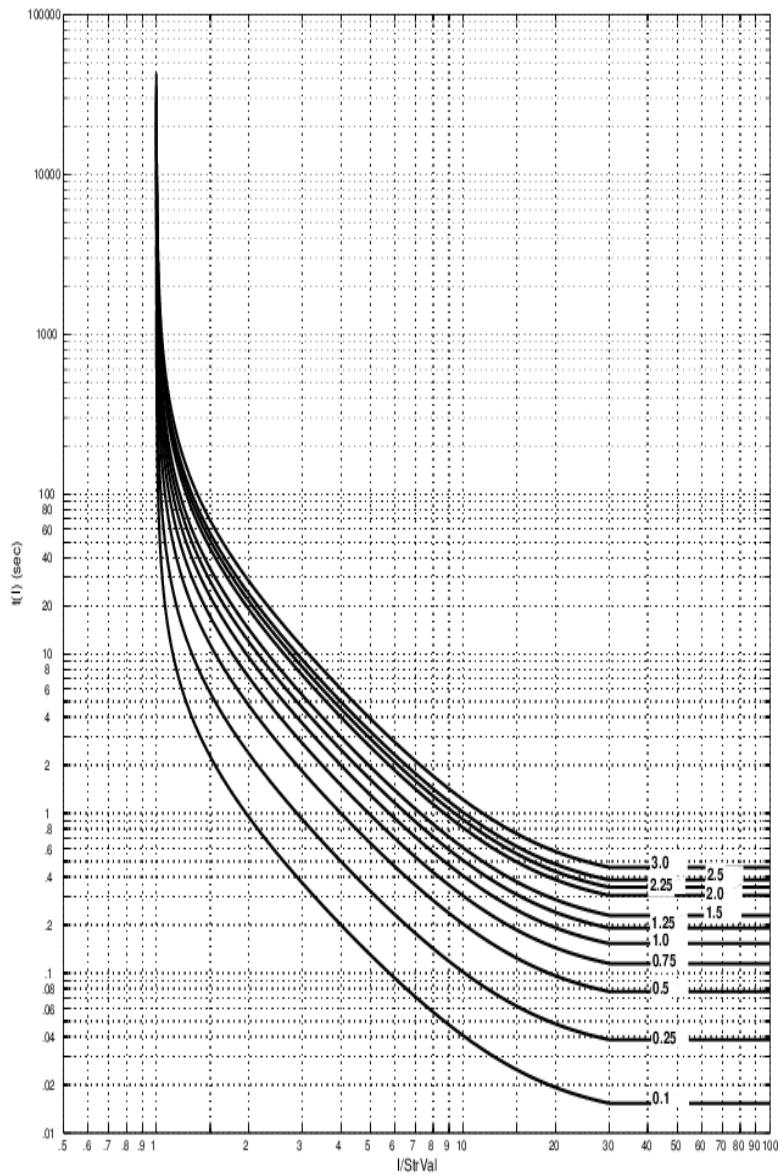


Figure 56 IEEE Extremely inverse

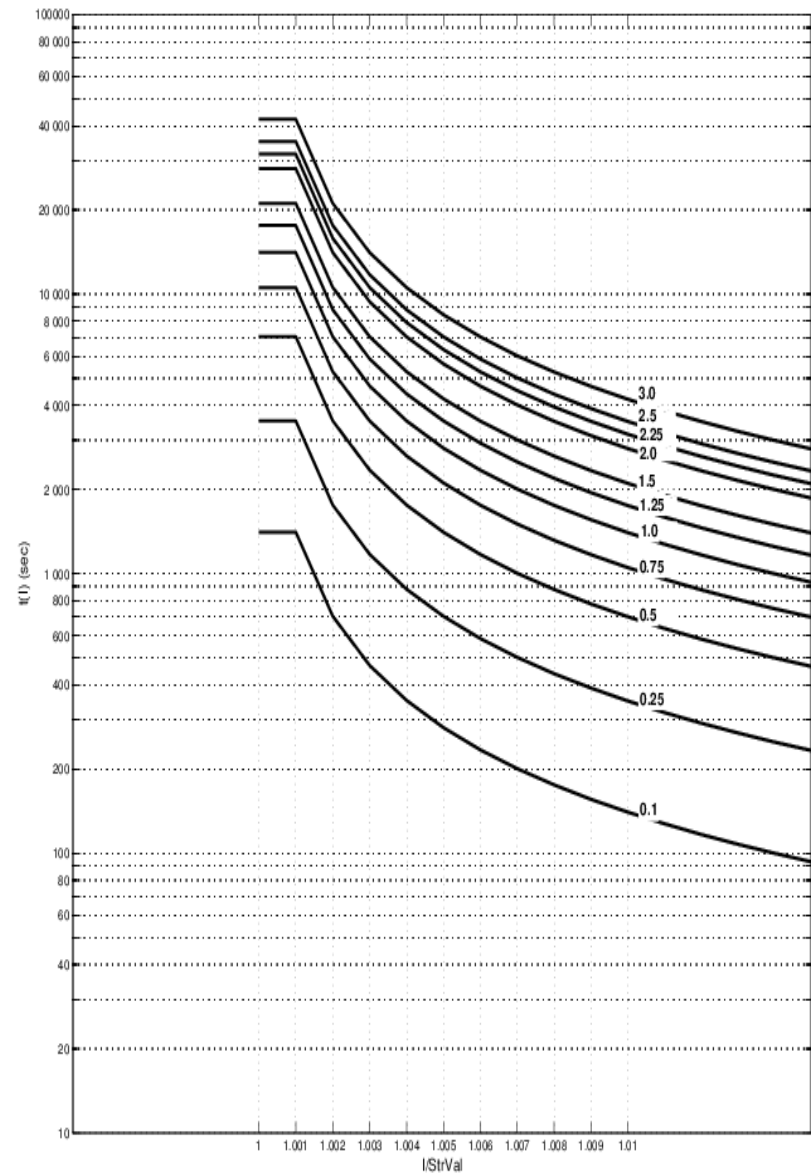


Figure 57 IEEE Extremely inverse – Zoom in

10 instances of the 50 protection element and 6 instances of the 50N protection element are configurable in the relay. Figure 59 shows the phase definite time overcurrent protection element logical diagram with the *Component* setting equal to *Three-phase*. Figure 58 shows the neutral definite time overcurrent protection element logical diagram with the *Component* setting equal to *Zero sequence*. For both elements, when the *Component* setting equals *Phase A/B/C*, the logical diagram corresponds to the one found on Figure 58. Table 22 lists the available settings for these protection elements.

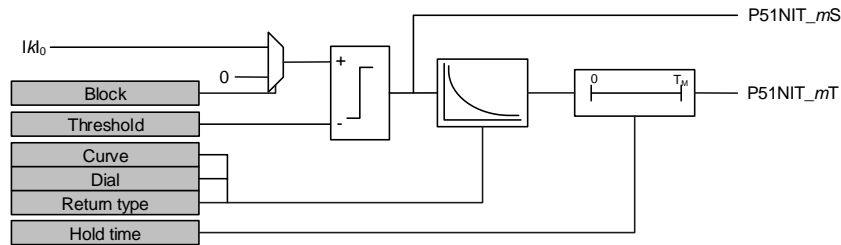


Figure 58 Neutral inverse time overcurrent protection element

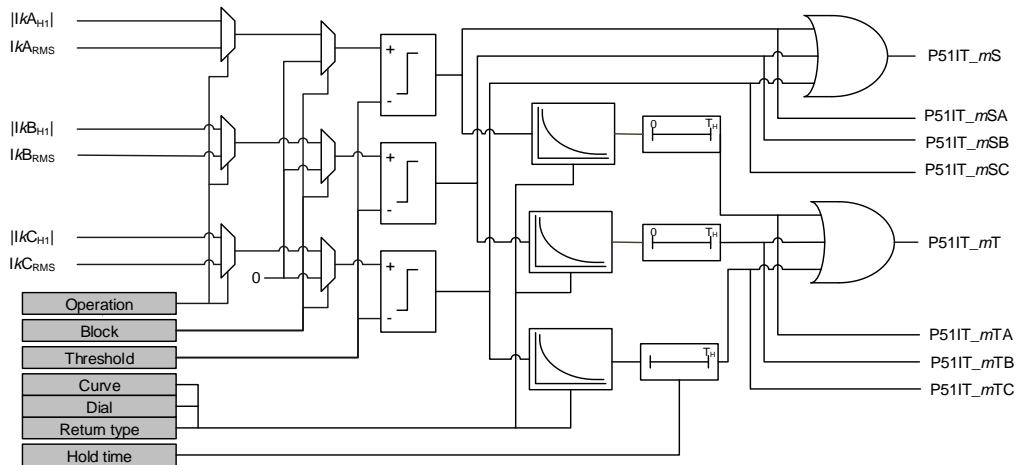


Figure 59 Phase inverse time overcurrent protection element

SETTING	RANGE	DESCRIPTION
Block	Binary points	Binary point blocking the input
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Decrement	Internal counter return type when start binary point falls to 0
Input	None; configured I/SI	Current or summed input used

Threshold	0.05-20 A (1A nominal) 0.25-100 A (5A nominal)	Start threshold, secondary
Hold time	0-100 s	Time between the start binary point falling to 0 and the trip binary point falling to 0
Operation	Total RMS; Fundamental RMS	Measured operating quantity evaluation method
Dial	0.05-1.10	Time multiplier factor used to compute the inverse trip time and the inverse return time
Component (50)	Three-phase; Phase A; Phase B; Phase C	Measured operating quantity type
Component (50N)	Zero sequence; Phase A; Phase B; Phase C	Measured operating quantity type
Curve	See Table 21 and Figures 46 to 57	Inverse time curve shape used to compute the inverse trip time and the inverse return time

Table 22 Inverse time overcurrent protection elements settings (51 IT/51N IT)

6.1.4. PHASE DIRECTIONAL OVERCURRENT PROTECTION ELEMENTS (67)

It is possible to configure a phase directional overcurrent element (67) by combining a phase directional element (DIR) with an overcurrent protection element (50/51 DT/51 IT).

First, it is important to note that the blocking settings of the protection elements are active high, i.e. the elements are blocked when the binary point associated with their *Block* setting is equal to logic state 1. Therefore, the correct direction binary point must be chosen to obtain the desired behaviour. Second, the same current input must be chosen for both the phase directional element and the overcurrent protection element.

Figure 60 shows an example of the configuration of a phase directional instantaneous overcurrent element that is blocked when current flows in the forward direction.

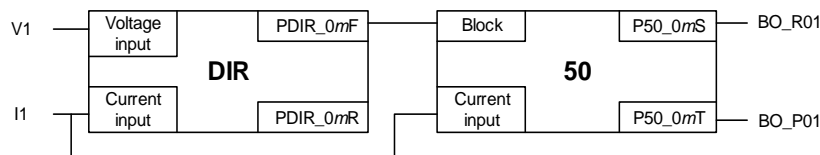


Figure 60 Example of the configuration of a phase directional overcurrent element (67)

6.2. DIFFERENTIAL PROTECTION ELEMENTS

6.2.1. TRANSFORMER (87U/R)

The transformer differential protection elements are used to detect faults that can happen in the protected transformer. The protection relay includes two transformer differential protection elements: with harmonics restraint (87R) and without harmonics restraint (87U). Traditionally, the unrestrained differential protection element protects the transformer against high current internal faults. The restrained differential protection element is more sensitive to low fault currents, while avoiding false trips caused by inrush currents and transformer overexcitation.

The transformer differential protection elements are based on the principle of conservation of electric charge. Theoretically, if the sum of the fundamentals of the currents entering the transformer is not equal to the sum of the fundamentals of the currents exiting it, there is a fault internal to the transformer. However, the transformer and current transformer configurations must be considered by compensating the filtered signals for amplitude and angle. These filtered and compensated signals are then used to compute the operation and restraint currents. Figure 61 shows the logic diagram for the differential protection elements when used with two current inputs.

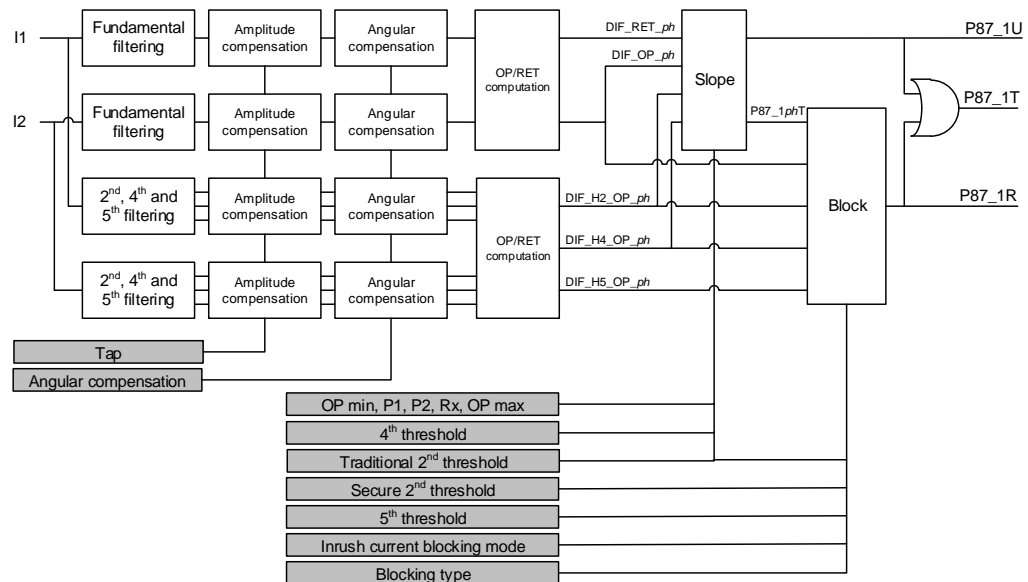


Figure 61 Restrained and unrestrained differential protection elements

In the protection relay, the restrained differential protection uses a percent differential with a dual slope and minimum threshold characteristic. The element processes each phase independently, thus producing three intermediary trip binary points.

6.2.1.1. MAGNITUDE CORRECTION

The protection relay measures the current from the secondary terminal of the current transformers. Since these CTs do not necessarily all have the same ratio, it is essential to bring all measured currents to an equal base. In the relay, the common reference for the magnitude correction is the apparent power of the transformer to protect. The relay computes a correction factor (equations (3) and (4)) for each current input using the information provided in the settings. It is also possible to directly input the correction factor in the settings. The choice between the two equations is done according to the CT connection type. Equation (3) is used for CTs connected in Wye, while equation (4) is used for Delta-connected CTs. The filtered current is multiplied by this correction factor to obtain a magnitude corrected current.

$$MCF = \frac{\sqrt{3} * LLV * CTR}{MVA} \quad (3)$$

$$MCF = \frac{LLV * CTR}{MVA} \quad (4)$$

Where MCF is the magnitude correction factor

MVA is the apparent power of the transformer

LLV is the line-to-line voltage associated with the current input,

CTR is the CT ratio associated with the current input.

6.2.1.2. PHASE CORRECTION

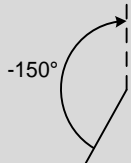
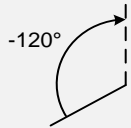
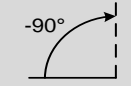
Currents entering a differential protection element are not necessarily in phase with each other because of phase shifting introduced by the windings of the transformer to protect or by the CTs. Therefore, it is necessary to correct the phase of the signals which are shifted from the reference input. This phase correction is a linear combination of the A, B and C phase of the signal, and can be represented by a matrix vector multiplication, as shown here :





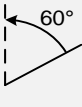
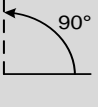
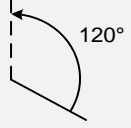
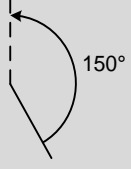
$$\begin{bmatrix} \text{Imc}_A \\ \text{Imc}_B \\ \text{Imc}_C \end{bmatrix} = \text{PCM} * \begin{bmatrix} \text{Impc}_A \\ \text{Impc}_B \\ \text{Impc}_C \end{bmatrix} \quad (5)$$

where $\text{Imc}_{A/B/C}$ is the magnitude corrected current phasor,
 $\text{Impc}_{A/B/C}$ is the magnitude and phase corrected current phasor,
 PCM is one of the phase correction matrices.

Table 23 lists the 12 possible phase shifts in the relay. You can see visual representation of the phase shift, the phase correction matrix and the corresponding linear combinations. It is important to note that all 12 linear combinations remove zero sequence from the signal while shifting its phase. The zero sequence must be removed for the cases where the transformer and CT windings both have a ground connection, thus allowing zero sequence current to flow. Presence of this current in a differential protection could cause false trips, so it is important to remove it.

The choice of the phase correction matrix is based on the angle of phase A of the transformer, but this angle can be modified by the CT connection $\pm 30^\circ$. This must be accounted for in the choice of the matrix. First, choose an arbitrary reference current input, and assign it a 0° phase correction matrix. The matrices of the other current inputs are chosen so that the input is in phase with the reference.

PHASE SHIFT	PHASE CORRECTION MATRIX	LINEAR COMBINATIONS
	$\begin{bmatrix} -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & 0 \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{\sqrt{3}}(-\text{Imc}_A + \text{Imc}_B)$ $\text{Impc}_B = \frac{1}{\sqrt{3}}(-\text{Imc}_B + \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{\sqrt{3}}(\text{Imc}_A + \text{Imc}_C)$
	$\begin{bmatrix} -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{3}(-\text{Imc}_A + 2 * \text{Imc}_B - \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{3}(-\text{Imc}_A - \text{Imc}_B + 2 * \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{3}(2 * \text{Imc}_A - \text{Imc}_B - \text{Imc}_C)$
	$\begin{bmatrix} 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ -\frac{1}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} & 0 \end{bmatrix}$	$\text{Impc}_A = \frac{1}{\sqrt{3}}(\text{Imc}_B - \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{\sqrt{3}}(-\text{Imc}_A + \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{\sqrt{3}}(\text{Imc}_A - \text{Imc}_B)$

	$\begin{bmatrix} \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \\ -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{3}(\text{Imc}_A + \text{Imc}_B - 2 * \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{3}(-2 * \text{Imc}_A + \text{Imc}_B + \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{3}(\text{Imc}_A - 2 * \text{Imc}_B + \text{Imc}_C)$
	$\begin{bmatrix} \frac{1}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \\ -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & 0 \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{\sqrt{3}}(\text{Imc}_A - \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{\sqrt{3}}(\text{Imc}_B - \text{Imc}_A)$ $\text{Impc}_C = \frac{1}{\sqrt{3}}(\text{Imc}_C - \text{Imc}_B)$
	$\begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{3}(2 * \text{Imc}_A - \text{Imc}_B - \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{3}(-\text{Imc}_A + 2 * \text{Imc}_B - \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{3}(-\text{Imc}_A - \text{Imc}_B + 2 * \text{Imc}_C)$
	$\begin{bmatrix} \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} & 0 \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \\ -\frac{1}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{\sqrt{3}}(\text{Imc}_A - \text{Imc}_B)$ $\text{Impc}_B = \frac{1}{\sqrt{3}}(\text{Imc}_B - \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{\sqrt{3}}(\text{Imc}_C - \text{Imc}_A)$
	$\begin{bmatrix} \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \\ -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{3}(\text{Imc}_A - 2 * \text{Imc}_B + \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{3}(\text{Imc}_A + \text{Imc}_B - 2 * \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{3}(-2 * \text{Imc}_A + \text{Imc}_B + \text{Imc}_C)$
	$\begin{bmatrix} 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{3}} & 0 & -\frac{1}{\sqrt{3}} \\ -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & 0 \end{bmatrix}$	$\text{Impc}_A = \frac{1}{\sqrt{3}}(-\text{Imc}_B + \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{\sqrt{3}}(\text{Imc}_A - \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{\sqrt{3}}(-\text{Imc}_A + \text{Imc}_B)$
	$\begin{bmatrix} -\frac{1}{3} & -\frac{1}{3} & \frac{2}{3} \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} & -\frac{1}{3} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{3}(-\text{Imc}_A - \text{Imc}_B + 2 * \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{3}(2 * \text{Imc}_A - \text{Imc}_B - \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{3}(-\text{Imc}_A + 2 * \text{Imc}_B - \text{Imc}_C)$
	$\begin{bmatrix} -\frac{1}{\sqrt{3}} & 0 & \frac{1}{\sqrt{3}} \\ \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} & 0 \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{\sqrt{3}}(-\text{Imc}_A + \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{\sqrt{3}}(\text{Imc}_A - \text{Imc}_B)$ $\text{Impc}_C = \frac{1}{\sqrt{3}}(\text{Imc}_B - \text{Imc}_C)$

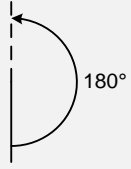
	$\begin{bmatrix} -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{bmatrix}$	$\text{Impc}_A = \frac{1}{3}(-2 * \text{Imc}_A + \text{Imc}_B + \text{Imc}_C)$ $\text{Impc}_B = \frac{1}{3}(\text{Imc}_A - 2 * \text{Imc}_B + \text{Imc}_C)$ $\text{Impc}_C = \frac{1}{3}(\text{Imc}_A + \text{Imc}_B - 2 * \text{Imc}_C)$
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Table 23 Phase correction matrices

6.2.1.3. HARMONIC RESTRAINT AND BLOCKING

To avoid false trips caused by inrush currents generated during transformer energization, the device offers three methods based on the even harmonics (2nd and 4th): restraint, traditional blocking and secure blocking. The restraint method raises the dual slope proportionally to the quantity of even harmonics detected in the inputs. The traditional blocking method is enabled when the quantity of one of the even harmonics is greater than its corresponding threshold (traditional 2nd threshold or 4th threshold).

The secure blocking method detects inrush currents in modern transformers which are characterized by weaker levels of 2nd harmonic in the inrush current. The relay exploits the fact that during an inrush current the fundamental and 2nd harmonic are in phase. If the traditional threshold is exceeded and the phase condition is fulfilled, the relay switches from the traditional threshold to the secure threshold. However, if the phase condition is no longer fulfilled, the relay switches from the secure threshold to the traditional threshold. If the traditional threshold is used, the relay blocks for at least three quarters of a cycle, whereas if the secure threshold is used, the relay blocks for at least 5 cycles. False trips caused by transformer overexcitation can be avoided with blocking based on the 5th harmonic. The relay produces intermediary blocking binary points for each phase (P87_1phBLK), as shown on Figure 62. For each phase, the P87_1phSEC binary point switches to 1 when the secure threshold is used and the relay blocks.

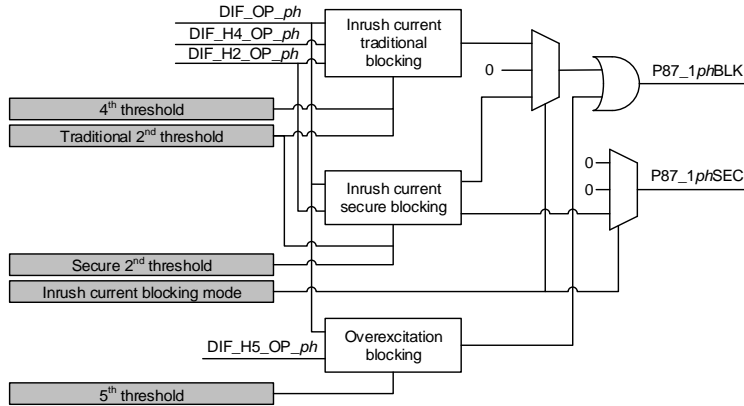


Figure 62 Blocking methods for the restrained differential protection element

The relay offers three blocking types: common blocking, 2 out of 3 blocking and per phase blocking. Figure 63 shows the logic diagram of each type. Common blocking is used to block the trip binary point as soon as a blocking binary point is detected on any phase. 2 out of 3 blocking is used to block the trip binary point as soon as a blocking binary point is detected on two out of the three phases. Per phase blocking first generates intermediary trip binary points for each phase before deciding on the overall trip binary point. When the secure blocking method is used, the relay limits the user to the per phase blocking type only to ensure a good balance between speed and security for the restrained differential protection element.

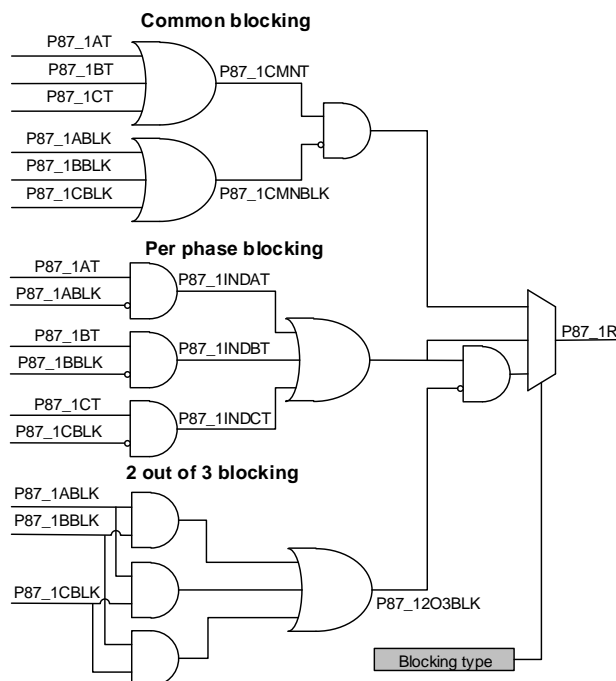


Figure 63 Blocking types for the restrained differential protection element

6.2.1.4. UNRESTRAINED DIFFERENTIAL ELEMENT

The unrestrained differential protection element has no restraint or harmonic blocking. It is a simple comparison between the operating current and a threshold usually set higher than the maximum expected inrush current.

6.2.1.5. DIFFERENTIAL PROTECTION SETTINGS

Table 24 lists the settings for the differential protection elements.

SETTING	RANGE	DESCRIPTION
Restrained differential protection element settings (87R)		
Operating current threshold	0.1 – 1 pu	Minimum operating current threshold
Differential slope 1	5 – 100%	Slope 1 value
Differential slope 2	0 – 100%	Slope 2 value
Knee point	1 – 4 pu	Knee point between the two slopes
Harmonic blocking mode	Traditional blocking; Secure blocking; Restraint	Choice between restraint or harmonic blocking (2 nd and 4 th harmonics)
Traditional 2nd threshold	5 – 100%	Traditional 2 nd harmonic blocking or restraint threshold
Secure 2nd threshold	5 – 100%	Secure 2 nd harmonic blocking threshold
4th threshold	5 – 100%	4 th harmonic or restraint blocking threshold
5th threshold	5 – 100%	5 th harmonic blocking threshold
Harmonic blocking type	Common; Per phase ; 2 out of 3	Choice between common, per phase or 2 out of 3 blocking types
CER restrained	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Unrestrained differential protection element settings (87U)		
Unrestrained threshold	5 – 20 pu	Unrestrained operating current threshold
CER unrestrained	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level

Table 24 Differential protection elements settings (87U/R)

6.3. VOLTAGE PROTECTION ELEMENTS

6.3.1. VOLTS PER HERTZ (24)

The Volts per Hertz protection element (24) detects transformer overexcitation by combining overvoltage detection with underfrequency detection. The ratio of normalized voltage over normalized frequency is compared to a threshold.

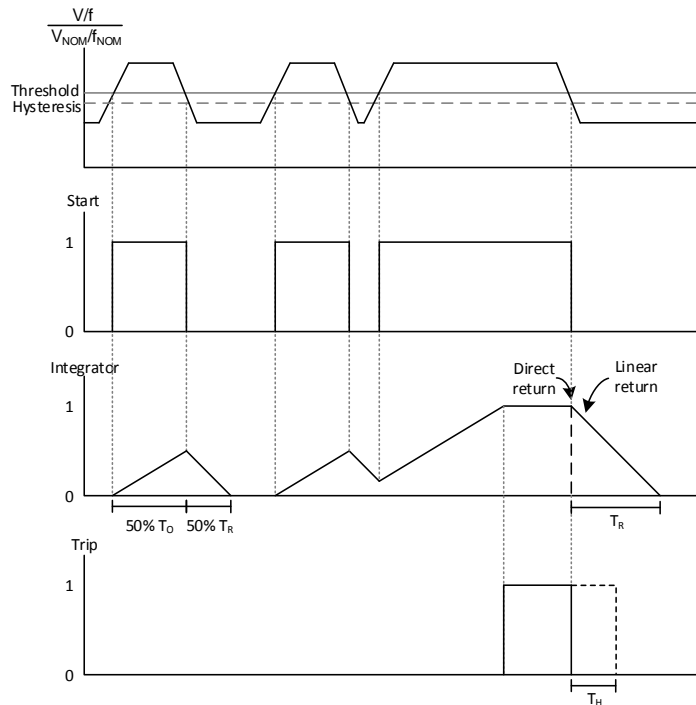


Figure 64 Timing diagram of the binary points of Volts per Hertz protection (24)

Figure 64 shows the timing diagram of the start and trip binary points. If the computed ratio is greater than the threshold, the start binary point switches to logic state 1. Each instance of the 24 protection element offers a choice of two modes for the calculation of the operating time delay, either *Definite time* or *Inverse time*. In *Definite time* mode, if the computed ratio remains above the threshold for a time delay equal or greater than the operating time setting (T_O), the trip binary point switches to logic state 1. In *Inverse time* mode, the trip binary point switches to logic state 1 if the ratio remains above the threshold for a time delay determined by the following equation:

$$t = \frac{\text{Dial}}{\left[\frac{\text{Ratio}}{\text{Threshold}} \right]^\alpha - 1} \quad (6)$$

Where Dial is the time multiplier setting, and α is an inverse curve parameter which can equal 1, 2 or 1/2.

In both modes, when the ratio falls back below the hysteresis of the threshold, the start binary point immediately switches back to logic state 0. If the operating time delay has elapsed, the trip binary point will switch back to logic state 0 when the hold time delay (T_H) elapses.

The Volts per Hertz protection element has two return types, either *Linear* or *Direct*, for the internal integrator which calculates the operating time delay. The return of the internal integrator is activated as soon as the ratio falls back below the threshold. In the *Linear* mode, if the operating time delay has elapsed, the internal integrator returns to zero in a time delay equal to the return time setting (T_R). If the operating time delay has not elapsed, the integrator returns to zero in a time delay proportional to the elapsed time since the start of the integration. For example, if the integrator is at 50% of its return value when the return is activated, the return time delay is equal to 50% of the T_R setting. In the *Direct* mode, if the operating time delay has elapsed, the internal integrator returns instantly to zero. If the operating time delay has not elapsed, the return of the internal integrator has the same behaviour as the *Linear* mode.

It is important to note that in the protection relay, the ratio is capped at a value of 30. There are 3 inverse time curve shapes available in the relay for the Volts per Hertz protection element. They are described in Table 25. Figures 65 to 70 show the curves for different dial values. Each curve has a zoomed in version for the small ratios.

CURVE	α
Curve 1	2
Curve 2	1
Curve 3	1/2

Table 25 Parameter α of the inverse time curves available in the Volts per Hertz protection element (24)

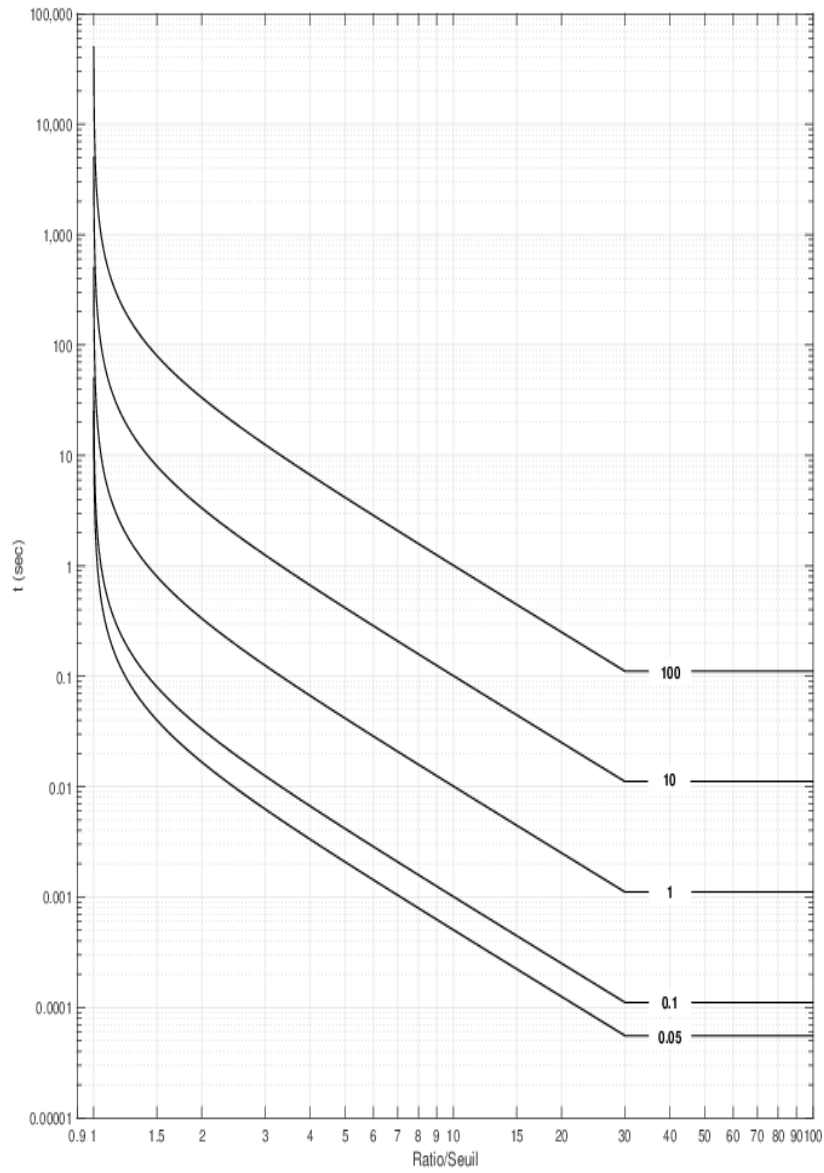


Figure 65 Curve 1

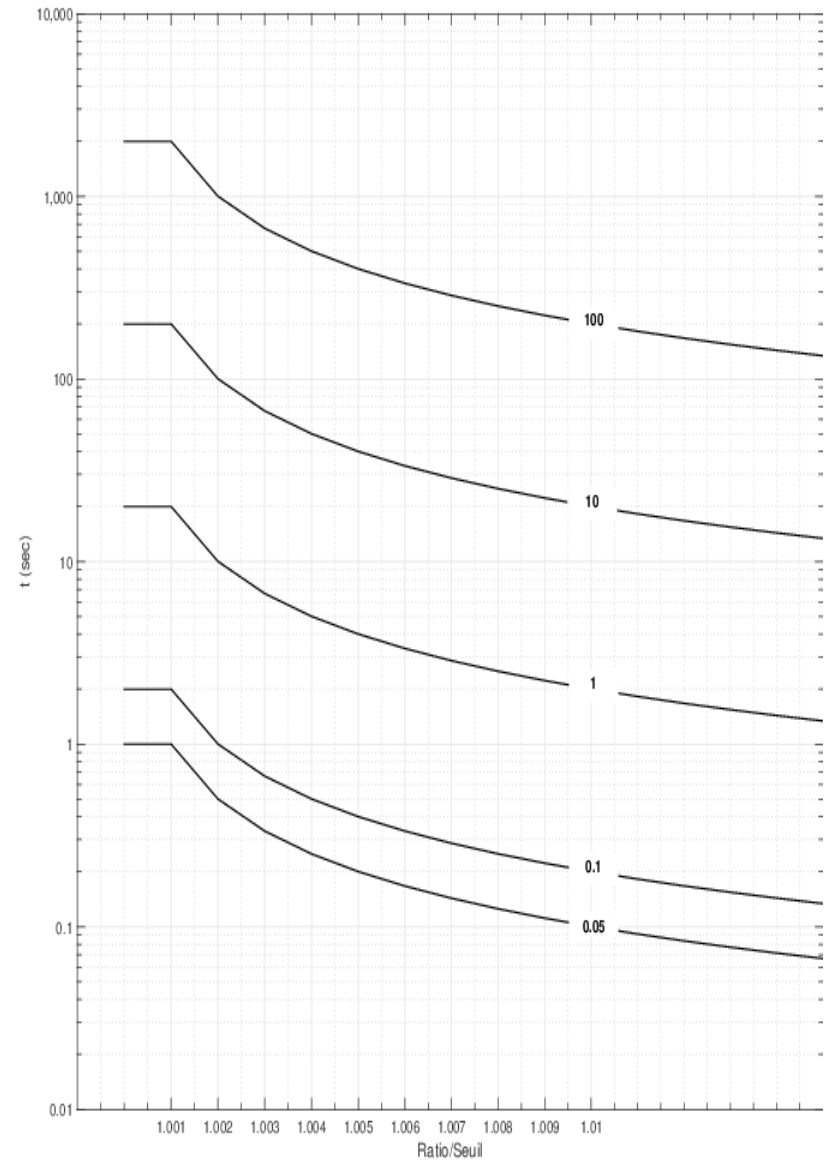


Figure 66 Curve 1 - Zoom in

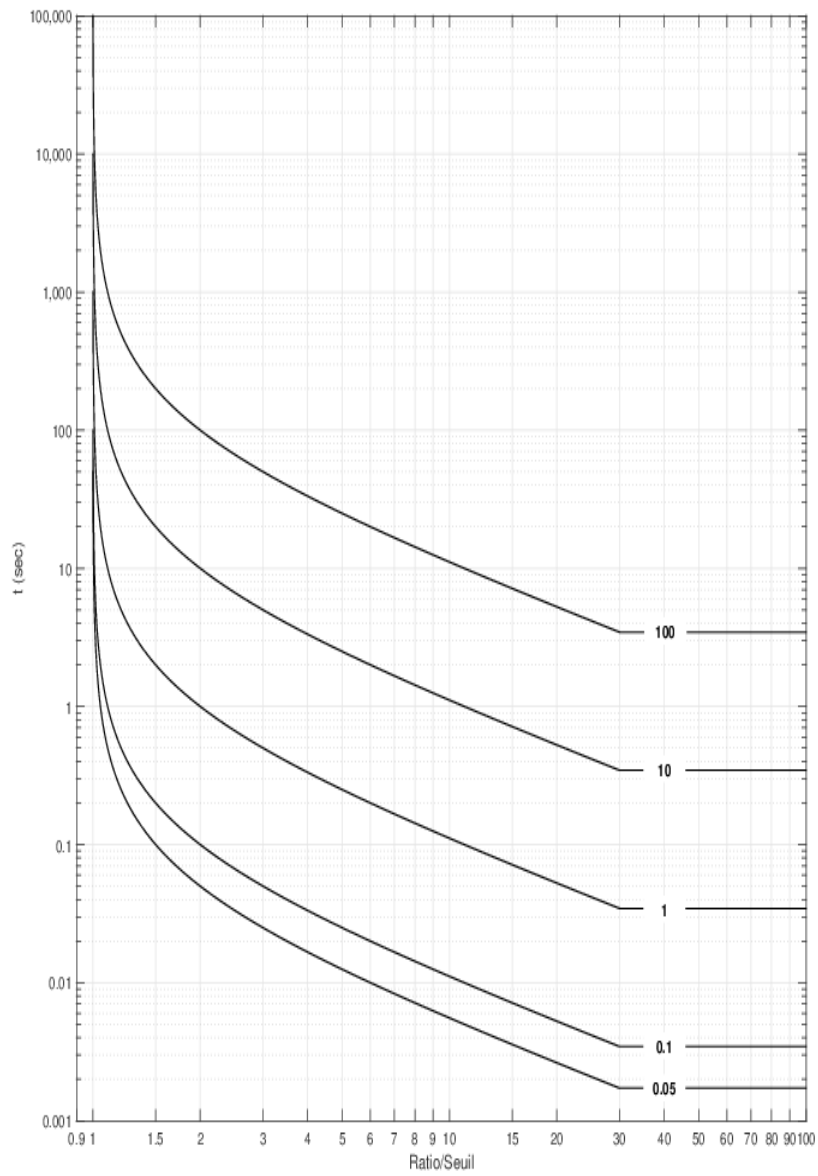


Figure 67 Curve 2

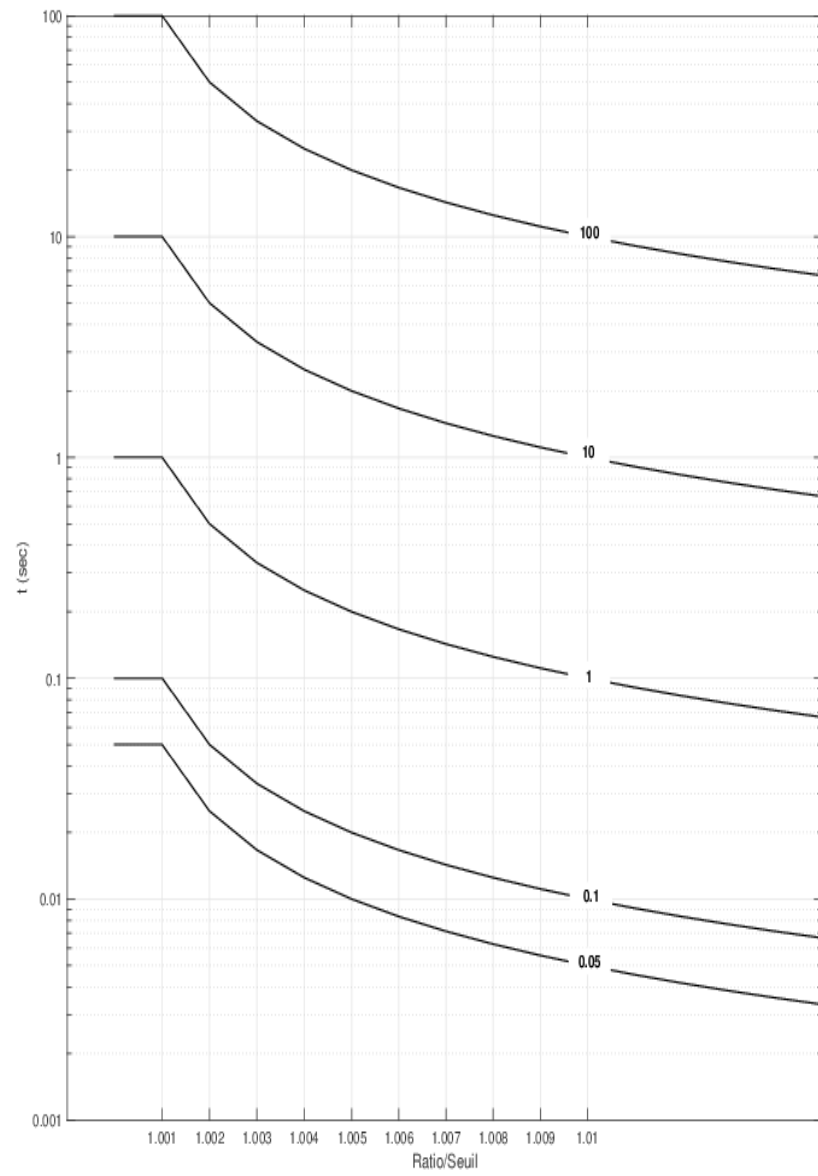


Figure 68 Curve 2 - Zoom in

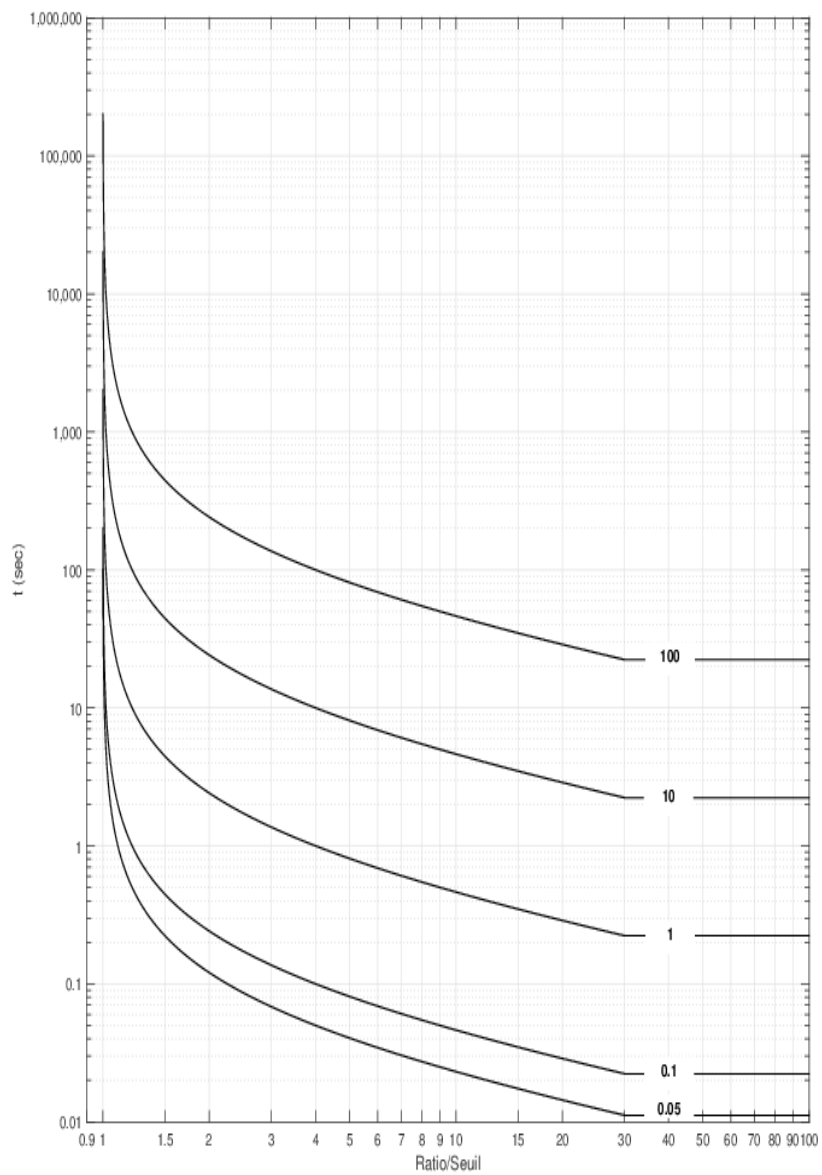


Figure 69 Curve 3

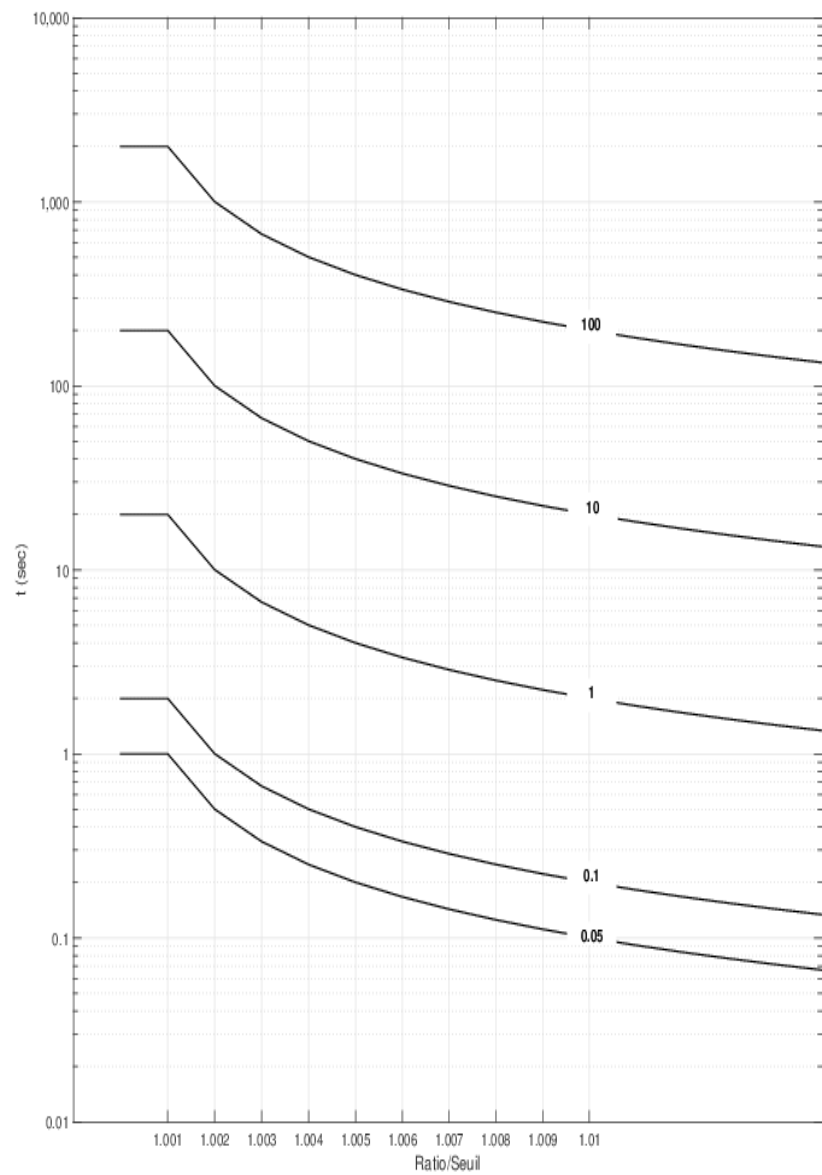


Figure 70 Curve 3 - Zoom in

3 instances of this protection element can be configured in the relay. Figure 71 shows the Volts per Hertz protection element logical diagram. Table 26 lists the available settings for this protection element.

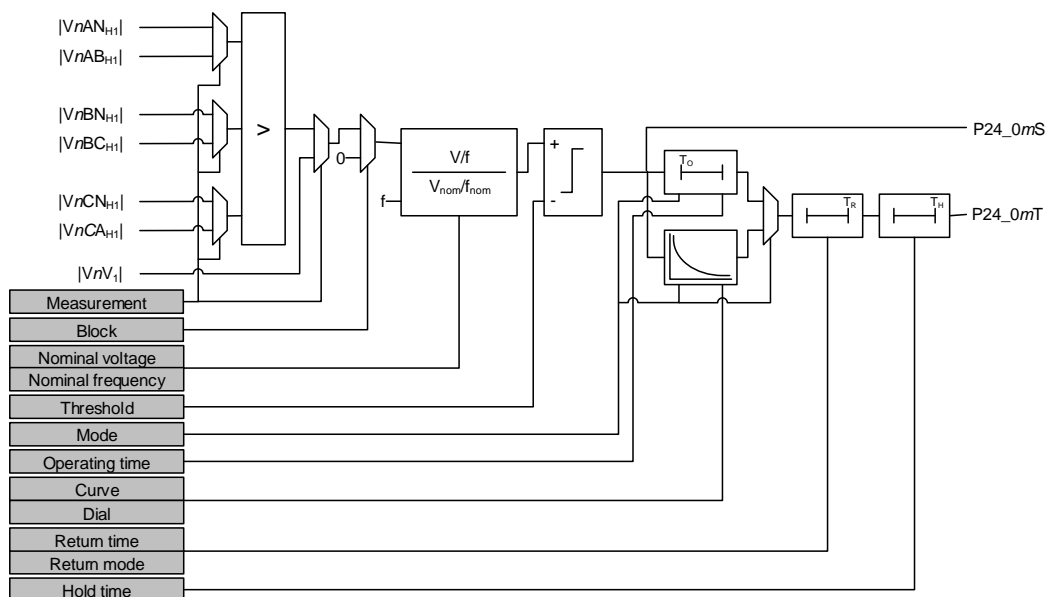


Figure 71 Volts per Hertz protection element

SETTING	RANGE	DESCRIPTION
Block	Binary points	Binary point blocking the input
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Input	None; configured V	Input used
Measurement	Phase-Ground; Phase-Phase; Positive sequence	Measurement type used in the comparison with the threshold
Threshold	0.8 – 3 pu	Start threshold
Mode	Definite time; Inverse time	Mode used for the instance
Operating time	0-900 s	Time between the start binary point rising to 1 and the trip binary point rising to 1; <i>Definite time</i> mode only
Curve	Curve 1; Curve 2; Curve 3	Choice of curve used for the calculation of the operating time delay; <i>Inverse time</i> mode only

Dial	0.05-100	Choice of dial used for the calculation of the operating time delay; <i>Inverse time</i> mode only
Return	Direct; Linear	Return mode of the internal integrator when the start binary point falls back to logic state 0
Return time	0-100 s	Time for the internal integrator to return to 0 when the start binary point falls back to logic state 0
Hold time	0-100 s	Time between the start binary point falling to 0 and the trip binary point falling to 0

Table 26 Volts per Hertz protection element

6.3.2. UNDERVOLTAGE (27)

The undervoltage protection element (27) compares the measured secondary operating quantity of a Voltage input to the threshold. Figure 72 shows the timing of the start and trip binary points. If the measured operating quantity falls below the threshold, the start binary point switches to logic state 1. If the measured operating quantity stays below the threshold for a period of time greater than the operating time setting, the trip binary point switches to logic state 1. It is also possible to set a minimum voltage threshold to block the element.

When the measured operating quantity rises above the hysteresis of the threshold, the start binary point immediately switches to logic state 0. If the operating time delay has elapsed, the trip binary point will switch back to logic state 0 when the hold time delay elapses.

At the moment the measured operating quantity rises above the threshold, if the operating time delay has not elapsed and the return type is set to *Decrement*, the operating time internal counter value is gradually decremented back to zero at a pace proportional to the operating time setting. Thus, if the measured operating quantity falls below the threshold during that period, the operating time internal counter does not start from zero. If the return type is set to *Direct*, the operating time internal counter value is reset to zero as soon as the operating quantity rises above the hysteresis of the threshold.

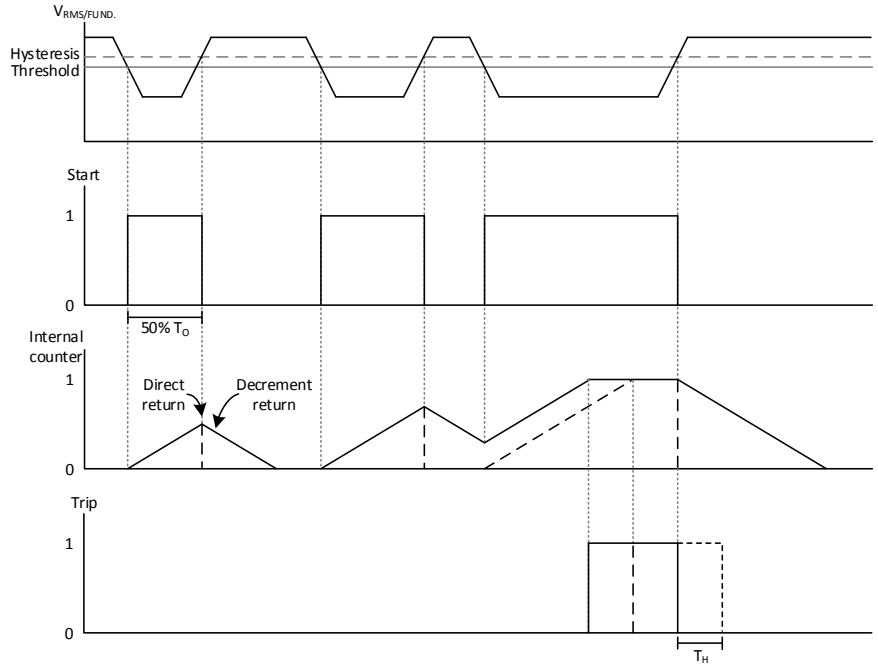


Figure 72 Timing diagram of the binary points of the undervoltage protection elements (27)

6 instances of the 27 protection element are configurable in the relay. Figure 73 shows the undervoltage protection element logical diagram. Table 27 lists the available settings for this protection element.

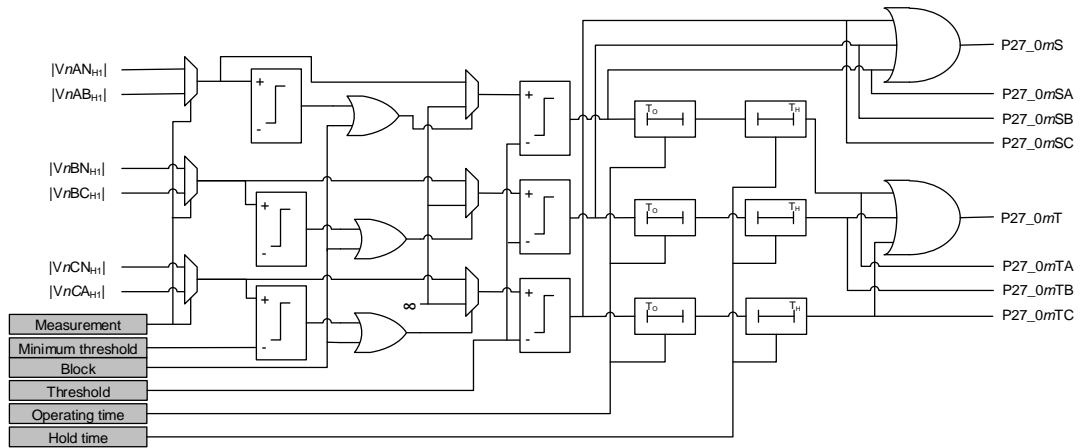


Figure 73 Undervoltage protection element

SETTING	RANGE	DESCRIPTION
Block	Binary points	Binary point blocking the input
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Decrement	Internal counter return type when start binary point falls to 0
Input	None; configured V	Input used
Threshold	20-300 V	Start threshold, secondary
Hold time	0-100 s	Time between the start binary point falling to 0 and the trip binary point falling to 0
Operating time	0-100 s	Time between the start binary point rising to 1 and the trip binary point rising to 1
Minimum	1-300 V	Minimum voltage threshold. If the measured value of any phase is below this threshold, the element is blocked
Measurement	Phase-Ground; Phase-Phase; Positive sequence	Measurement type used in the comparison with the threshold
Operation	Total RMS; Fundamental RMS	Measured operating quantity evaluation method (when <i>Measurement</i> is set to <i>Phase-Ground</i>)

Table 27 Undervoltage protection element settings (27)

6.3.3. OVERVOLTAGE (59)

The overvoltage protection element (59) compares the measured secondary operating quantity of a Voltage input to the threshold. Figure 74 shows the timing diagram of the start and trip binary points. If the measured operating quantity is greater than the threshold, the start binary point switches to logic state 1. If the measured operating quantity stays above the threshold for a period of time greater than the operating time setting, the trip binary point switches to logic state 1.

When the measured operating quantity falls below the hysteresis of the threshold, the start binary point immediately switches to logic state 0. If the operating time delay has elapsed, the trip binary point will switch back to logic state 0 when the hold time delay elapses. At the moment the measured operating quantity rises above the threshold, if the operating time delay has not elapsed and the return type is set to *Decrement*, the operating time internal counter value is gradually decremented back to zero at a pace

proportional to the operating time setting. Thus, if the measured operating quantity rises above the threshold during that period, the operating time internal counter does not start from zero. If the return type is set to *Direct*, the operating time internal counter value is reset to zero as soon as the operating quantity falls below the hysteresis of the threshold.

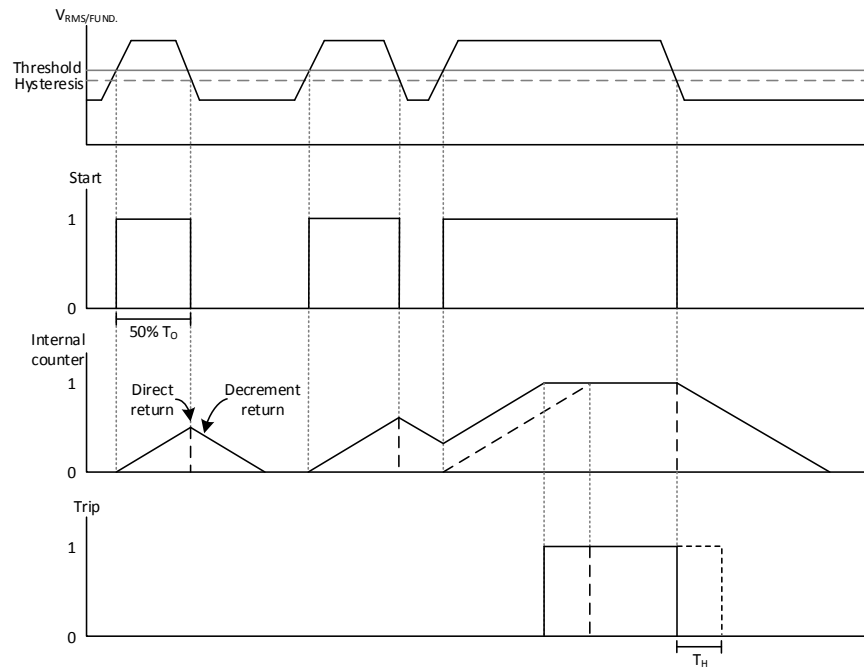


Figure 74 Timing diagram of the binary points of the overvoltage protection elements (59)

6 instances of the 59 protection element are configurable in the relay. Figure 75 shows the overvoltage protection element logical diagram. Table 28 lists the available settings for this protection element.

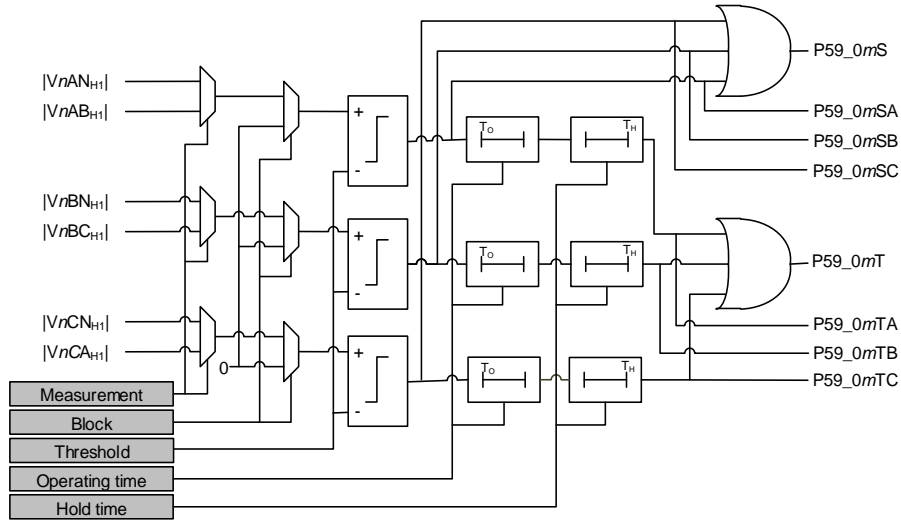


Figure 75 Overvoltage protection element

SETTING	RANGE	DESCRIPTION
Block	Binary points	Binary point blocking the input
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Decrement	Internal counter return type when start binary point falls to 0
Input	None; configured V	Input used
Threshold	20-300 V	Start threshold, secondary
Hold time	0-100 s	Minimum time between the start binary point falling to 0 and the trip binary point falling to 0
Operating time	0-100 s	Minimum time between the start binary point falling to 1 and the trip binary point falling to 1
Measurement	Phase-Ground; Phase-Phase; Positive sequence	Measurement type used in the comparison with the threshold
Operation	Total RMS; Fundamental RMS	Measured operating quantity evaluation method (when <i>Measurement</i> is set to <i>Phase-Ground</i>)

Table 28 Overvoltage protection element settings (59)

6.3.4. PEAK VOLTAGE DETECTOR (VPD)

The peak voltage detection element (VPD) compares the absolute raw phase-neutral secondary voltage to a threshold. If the number of samples where the voltage is higher than the threshold is equal or greater than the *Minimum/peak* setting, the peak is valid. If the number of valid peaks detected in a cycle is equal or greater than the *Peaks/cycle* setting, the cycle is active and the start binary point switches to logic state 1.

The *Mode* setting determines if and when the trip binary point switches to logic state 1. In the normal mode, there needs to be a consecutive number of active cycles equal or greater than the *Consecutive cycles* setting. When a cycle is inactive, the *return type* setting determines how the internal counter is reset. When the *return type* is set to *Direct*, the internal counter value is reset to zero when the first inactive cycle is encountered. When the *return type* setting is set to *Decrement*, the internal counter value is decremented by 1 for each inactive cycle encountered. The trip binary point will be reset to 0 after a time delay equal to the hold time setting following the first inactive cycle encountered after a trip. Figure 76 shows the timing diagram of the start and trip binary points for this mode.

In the sliding window mode, there needs to be at least “Required cycles” active cycles amongst “Window cycles” cycles. When this condition is no longer respected, the trip binary point will be reset to 0 after a time delay equal to the hold time setting.

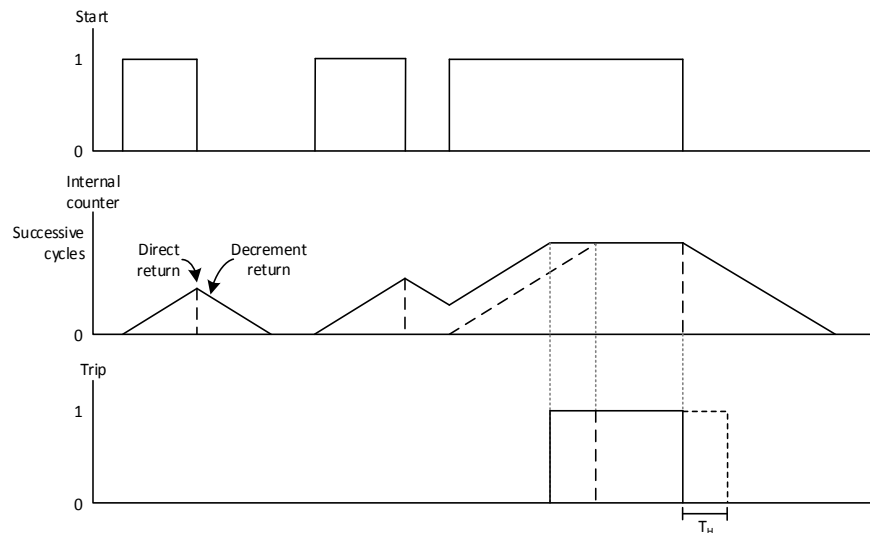


Figure 76 Timing diagram of the binary points of the peak voltage detector (VPD) for the normal mode

Figures 77 and 78 show one cycle of a raw 60 Hz waveform with voltage peaks that can be detected by the VPD protection element. The following settings are an example that would allow the VPD protection element to declare this cycle as active:

- Threshold : value represented by the dashed lines
- Minimum/peak : 2 samples
- Peaks/cycle : 2 peaks

With these settings, the peaks of zones A and B are active since they have 2 and 6 samples, respectively. The peaks of zone C are not active because they only have 1 sample each. Since this cycle has two active peaks, it is considered active by the algorithm and the start binary point switches to logic state 1.

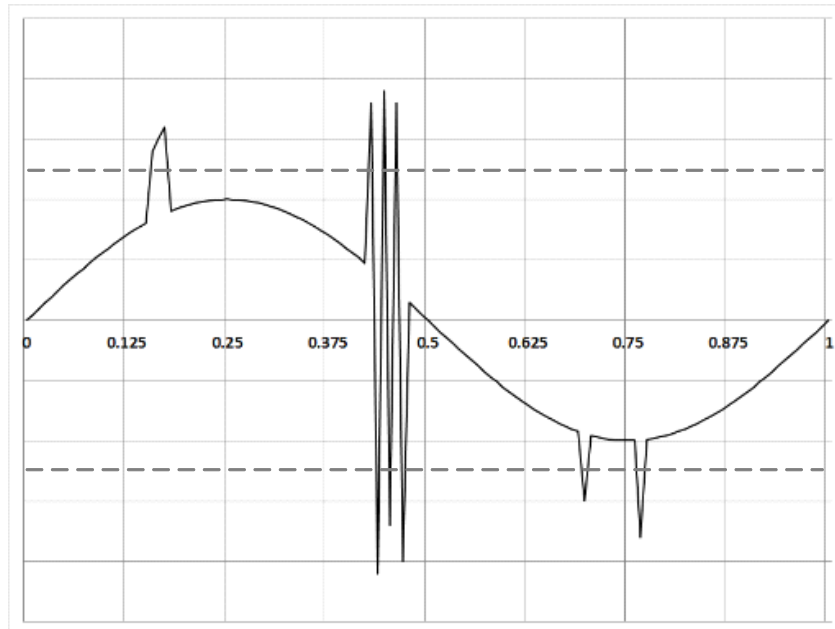


Figure 77 Waveform with voltage peaks

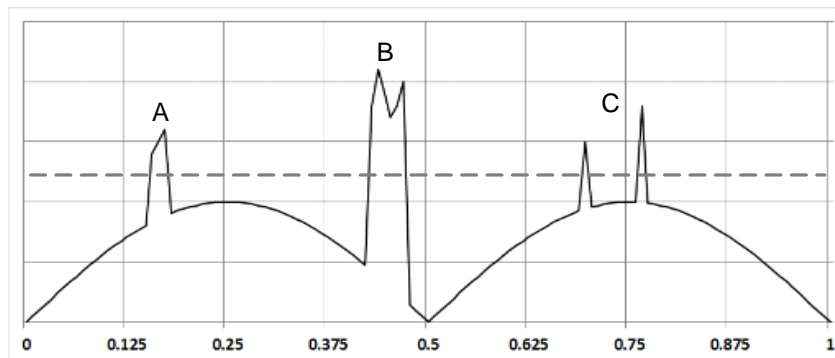


Figure 78 Waveform with voltage peaks – Absolute value

The VPD protection element is based on the fact that one cycle of a 60 Hz voltage has 128 raw samples. To respect this criteria at all times, frequency tracking must be deactivated. If it is not, the correct behaviour of the VPD protection element cannot be ensured.



IMPORTANT : Since the VPD protection element uses the raw phase-neutral secondary voltage, it is more sensitive to the disturbances that can affect the voltage read by the protection relay. It is therefore important to consider these factors when configuring the VPD protection element.

6 instances of the VPD protection element are configurable in the relay. Figure 79 shows the VPD protection element logical diagram. Table 29 lists the available settings for this protection element.

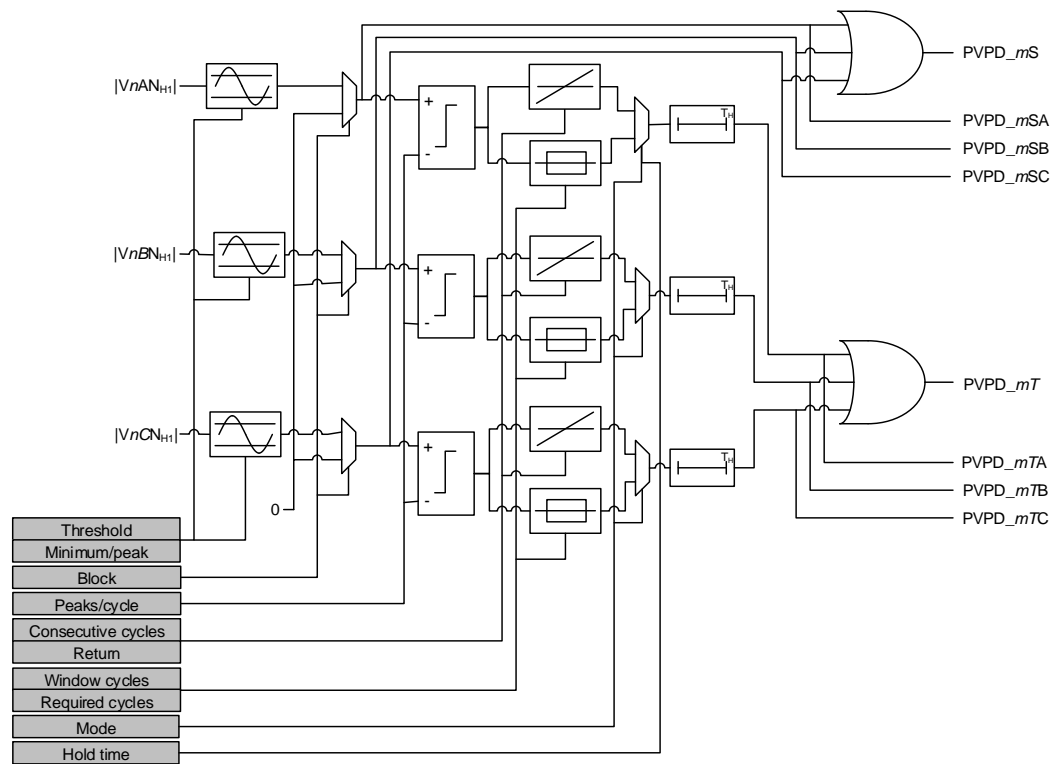


Figure 79 Voltage peak detector protection element

SETTING	RANGE	DESCRIPTION
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level

CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Hold	Normal mode : internal counter return type when a cycle is inactive
Input	None; configured V	Input used
Threshold	0.25-425 V	Start threshold, instantaneous secondary value
Hold time	0-100 s	Normal mode : after a trip, time delay between the first inactive cycle and the trip signal falling to 0 Sliding window mode : after a trip, time delay between the sliding window conditions being no longer respected and the trip signal falling to 0
Mode	Normal; Sliding window	Number of peaks detection mode
Minimum/peak	1 – 8	Minimum number of samples for an active peak
Peaks/cycle	1 – 8	Minimum number of active peaks for an active cycle
Consecutive cycles	1 – 16	Normal mode : number of consecutive active cycles needed for a trip
Window cycles	1 – 30	Sliding window mode : window width, in number of cycles
Required cycles	1 – 30	Sliding window mode : number of active cycles needed in a window for a trip

Table 29 Voltage peak detector protection element settings (VPD)

6.4. FREQUENCY PROTECTION ELEMENTS

6.4.1. UNDER/OVERFREQUENCY (81)

The under/overfrequency protection element (81) combines two types of protection elements in one. If the threshold set by the user is equal or greater than the nominal frequency, the enabled protection element is an overfrequency one; otherwise, it is an underfrequency protection element.

Figure 80 shows the timing diagram for the start and trip binary points of the overfrequency protection element. If the frequency rises above (overfrequency) or falls below (underfrequency) the threshold, the start binary point switches to logic state 1. If this condition is respected for a period of time greater than the operating time setting, the trip binary point switches to logic state 1.

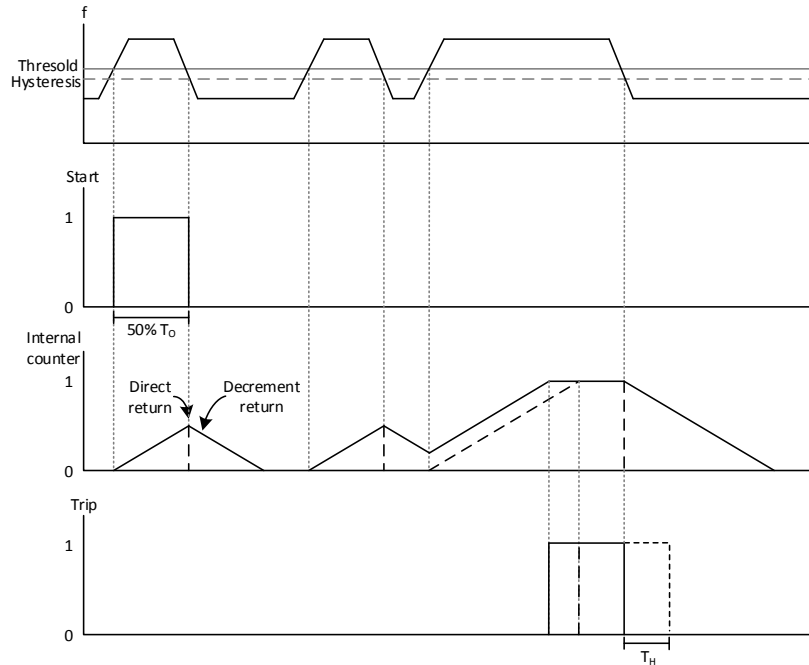


Figure 80 Timing diagram of the binary points of the overfrequency protection element (81)

When the frequency no longer respects the start condition, the start binary point immediately switches to logic state 0. If the operating time delay has elapsed, the trip binary point will switch back to logic state 0 when the hold time delay elapses. At the moment the frequency falls below “overfrequency” or rises above “underfrequency”, the hysteresis of the threshold, if the operating time delay has not elapsed and the return type is set to *Decrement*, the operating time internal counter value is gradually decremented back to zero at a pace proportional to the operating time setting. Thus, if the frequency respects the start condition again during that period, the operating time internal counter does not start from zero. When the return type is set to *Direct*, the internal counter value is reset to 0 as soon as the start condition is no longer respected.

It is important to note that the under/overfrequency protection element is disabled if the grid frequency is not computed by the relay (see section 7.2 for more details on frequency computation).

6 instances of the 81 protection element are configurable in the relay. Figure 81 shows the under/overfrequency protection element logical diagram. Table 30 lists the available settings for this protection element.

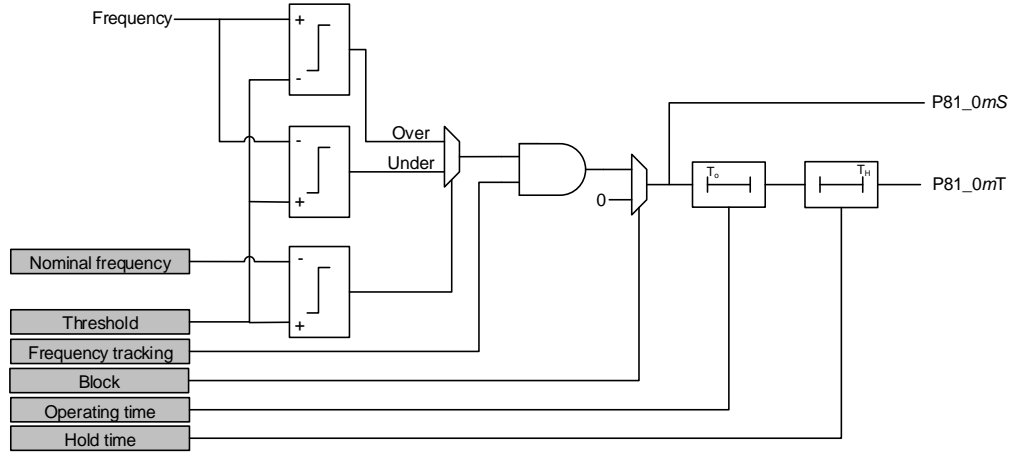


Figure 81 Under/overfrequency protection element

SETTING	RANGE	DESCRIPTION
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Decrement	Internal counter return type when start binary point falls to 0
Threshold	40-75 Hz	Start threshold
Hold time	0-100 s	Time between the start binary point falling to 0 and the trip binary point falling to 0
Operating time	0-100 s	Time between the start binary point rising to 1 and the trip binary point rising to 1

Table 30: Under/overfrequency protection element settings (81)

6.4.2. FREQUENCY RATE-OF-CHANGE (81R)

The frequency rate-of-change protection element (81R) compares the rate-of-change of the frequency to the threshold, which can be positive, negative or in absolute value. Figure 82 shows the timing diagram for the start and trip binary points in the case of a positive threshold. For positive thresholds, if the computed rate-of-change is greater than the threshold and the measured grid frequency is above or equal to the nominal frequency, the start binary point switches to logic state 1. For negative thresholds, if the computed rate-of-change is lower than the threshold and the measured grid frequency is below the nominal frequency, the start binary point switches to logic state 1. For absolute value thresholds, the start binary point switches to logic state 1 if the absolute value of the computed frequency rate-of-change is greater than the absolute value of the threshold. If

the start binary point stays at logic state 1 for a period of time greater than the operating time setting, the trip binary point switches to logic state 1.

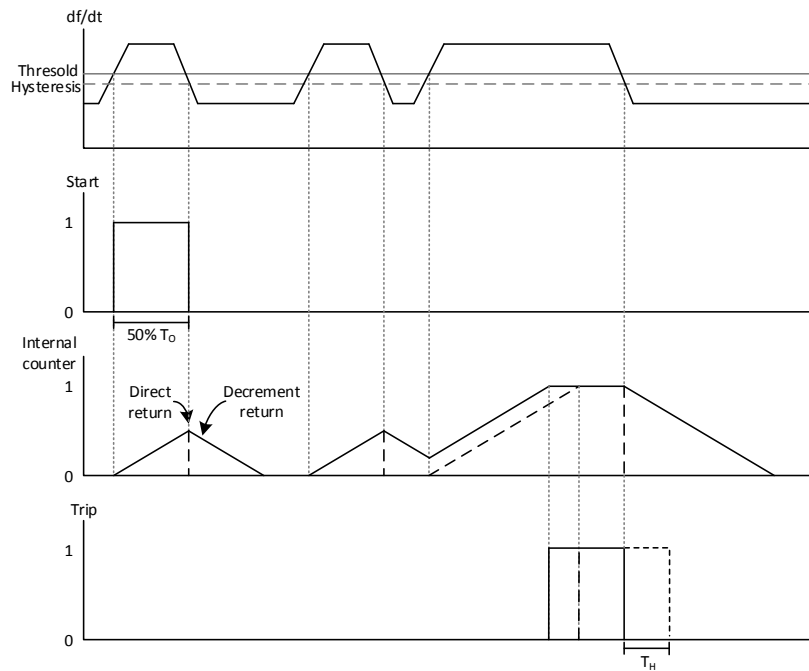


Figure 82 Timing diagram of the binary points of the frequency rate-of-change protection element (81R) for the positive threshold

When the frequency rate-of-change no longer respects the start condition, the start binary point is immediately reset to 0. If the operating time has elapsed, the trip binary point will fall back to 0 after a time delay equal to the hold time setting. When the return type is set to *Decrement* and the operating time has not elapsed, the value of the internal counter at the moment the start binary point falls to 0 will gradually be reset to zero at a pace proportional to the operating time. Thus, if the frequency rate-of-change respects the start condition again during that period of time, the internal counter does not start from zero. When the return type is set to *Direct*, the value of the internal counter is reset to zero as soon as the start condition is no longer respected.

It is important to note that the frequency rate-of-change protection element is disabled if the grid frequency is not computed (see section 7.2 for more details on frequency computation). 6 instances of the 81R protection element are configurable in the relay. Figure 83 Frequency rate-of-change protection element shows the under/overfrequency protection element logical diagram. Table 31 lists the available settings for this protection element.

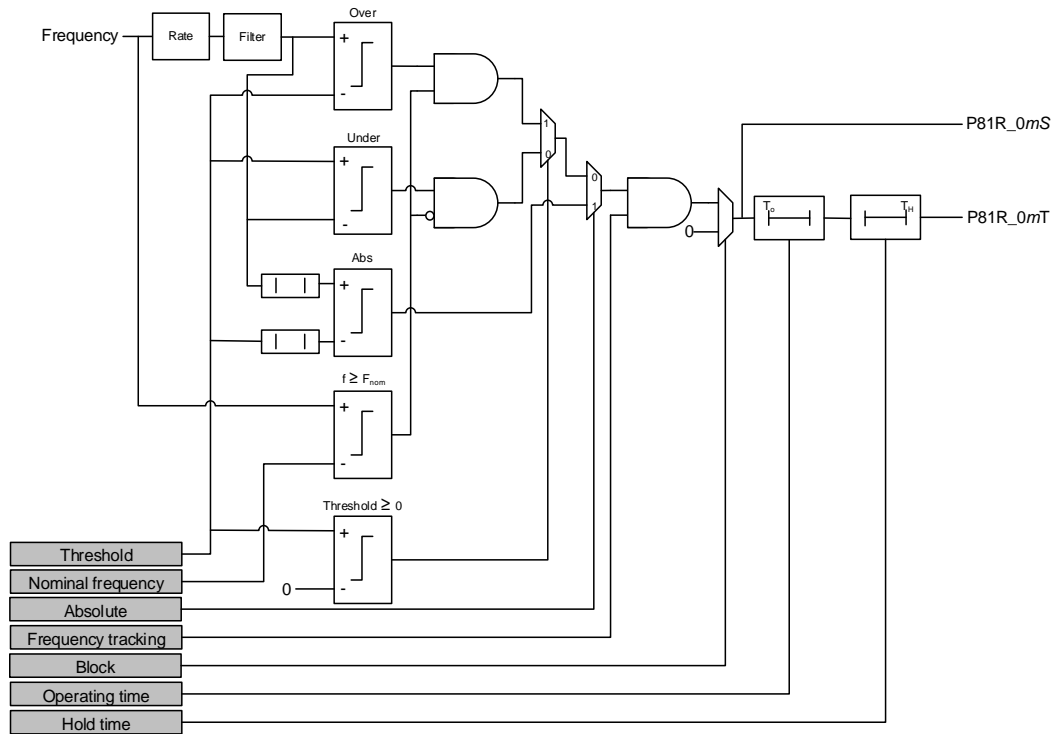


Figure 83 Frequency rate-of-change protection element

SETTING	RANGE	DESCRIPTION
CER start	None; Rising; Falling; Both	Event triggered by the start binary point, according to the chosen level
CER trip	None; Rising; Falling; Both	Event triggered by the trip binary point, according to the chosen level
Return	Direct ; Hold	Internal counter return type when start binary point falls to 0
Threshold	-10-10 Hz/s	Start threshold
Hold time	0-100 s	Minimum time between the start binary point falling to 0 and the trip binary point falling to 0
Operating time	0-100 s	Minimum time between the start binary point falling to 1 and the trip binary point falling to 1
Absolute slope	On ; Off (Relative)	Slope type
Minimum voltage	1-300 V	Minimum voltage threshold to enable the element

Table 31 Frequency rate-of-change protection element settings (81R)

6.5. CONTROL ELEMENTS

6.5.1. PHASE DIRECTIONAL ELEMENT (DIR)

The phase directional element determines the direction of each current phase and is used to control other protection elements via their blocking setting. Polarization of each phase directional element is done with the voltage positive sequence shifted in the leading direction by the element characteristic angle (ECA). For phases B and C, the polarizing quantity is shifted by 120° in the lagging or leading direction, respectively, as shown in figure 84. The direction of the current is determined by computing the angle between the current and the polarizing quantity. If this angle is between -90° and $+90^\circ$, the forward direction binary point (PDIR_0mA/B/CF) is set to logic state 1. Otherwise, the reverse direction binary point is set to logic state (PDIR_0mA/B/CR) 1.

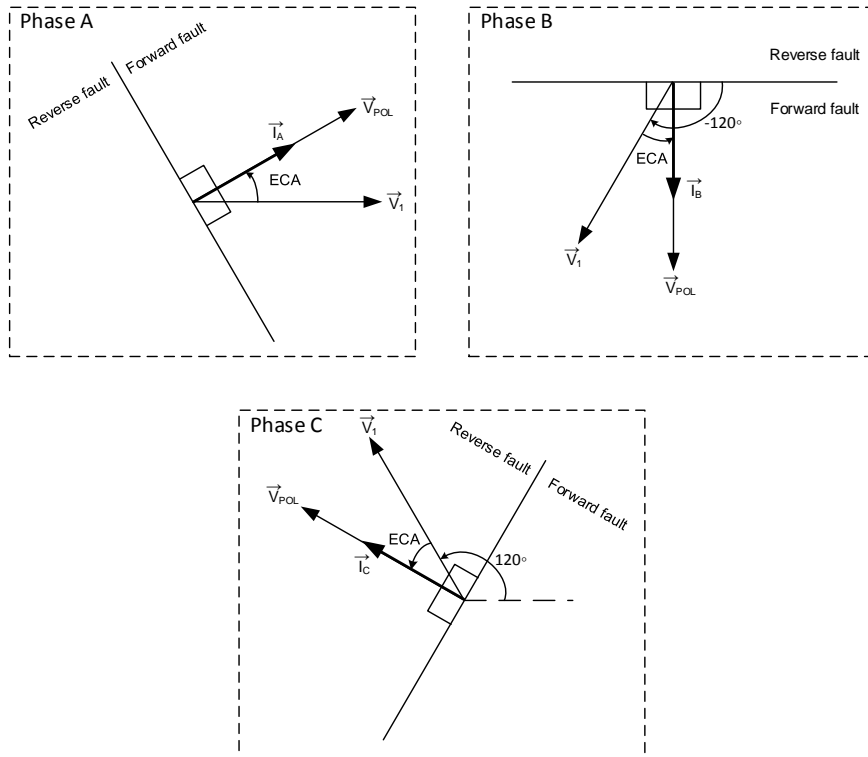


Figure 84 Phase directional elements polarization

A 1 second voltage memory is used to improve the security of the phase directional element. If the magnitude of the polarizing quantity is below the minimum voltage setting for at least a 60 Hz cycle, the phase directional element will use the memorised voltage as a polarizing quantity. This is valid for 1 second after the voltage drop. After this second, the phase directional element is blocked, forcing both direction binary points to logic state

0. The element is also blocked if the magnitude of the fundamental of the phase current is below 10% of the nominal current of the current input used. Figure 85 shows the phase directional element logical diagram. It is possible to configure 6 instances of the phase directional element. Table 32 shows the available settings for the phase directional element.

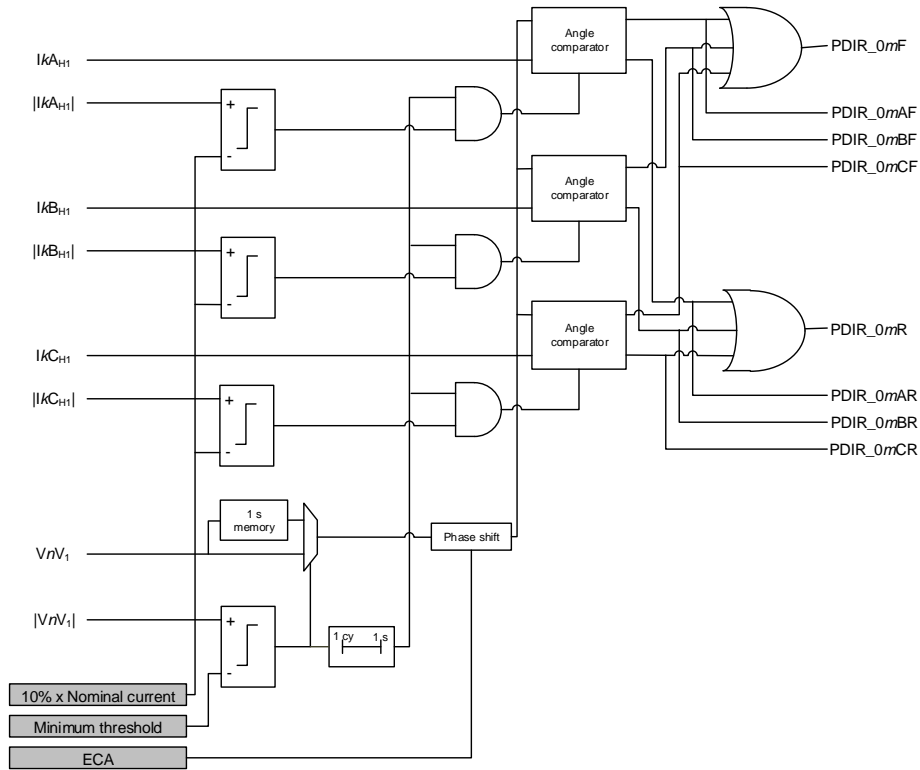


Figure 85 Phase directional element

SETTING	RANGE	DESCRIPTION
CER forward	None; Rising; Falling; Both	Event triggered by the forward direction binary point, according to the chosen level
CER reverse	None; Rising; Falling; Both	Event triggered by the reverse direction binary point, according to the chosen level
Voltage input	None; configured V	Voltage input used
Current input	None; configured I	Current input used
Minimum voltage	0 – 300 V	Minimum voltage threshold of the element, in secondary value. If the RMS value of the polarisation quantity is below this threshold, the memory is activated for 1 second.
ECA	0 – 359.999°	Element characteristic angle by which the voltage positive sequence is shifted in the leading direction to obtain the polarizing quantity

Table 32 Phase directional element settings

6.5.2. LOSS OF VOLTAGE DETECTION ELEMENT (LOV)

Certain applications need an alarm to be raised or a function to be blocked when a loss of voltage occurs. The loss of voltage detection element (LOV) fulfills those needs. If the fundamental magnitude of the voltage of a phase, measured in secondary values, drops below 90% within one cycle, but the fundamental magnitude of the current, measured in secondary values, is still at its nominal value, the detection binary point is set to 1. If the voltage doesn't come back to its nominal value within 15 cycles, the detection is latched until the voltage reaches its nominal value. The blocked binary point is set to 0 when a condition stops the element from detecting a voltage loss, such as an absence of or a variation in current, or being blocked by another binary point. When an absence of or a variation in current is detected, the blocked binary point is memorised for 15 cycles. Figure 86 shows the timing diagram of the detection and blocked binary points.

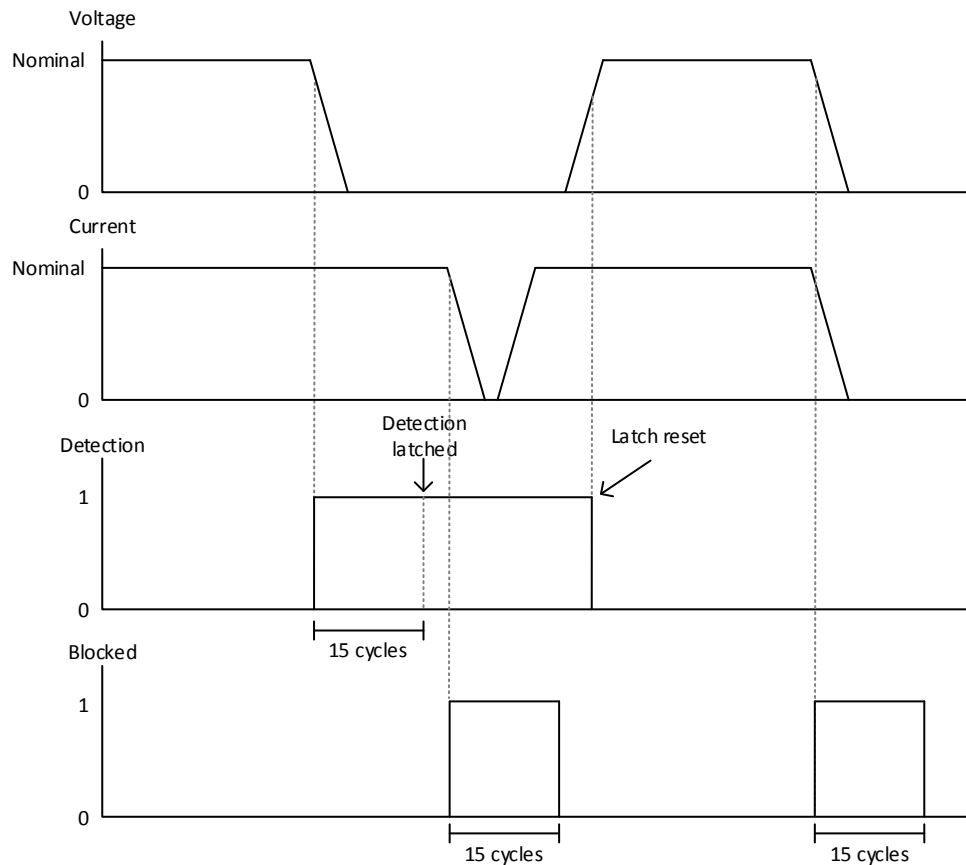


Figure 86 Timing diagram of the binary points of the loss of voltage detection element (LOV)

There is one loss of voltage detection element per three-phase voltage input of the protection relay. Figures 87 to 89 show the loss of voltage detection element logical diagram. Table 33 lists the available settings for this control element.

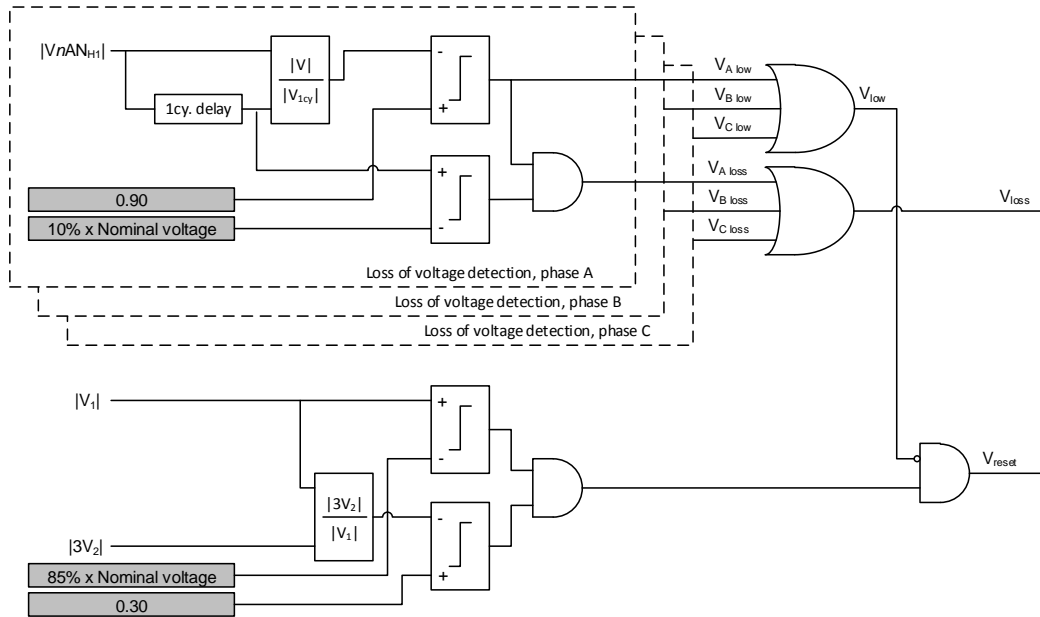


Figure 87 Loss of voltage detection element (LOV)

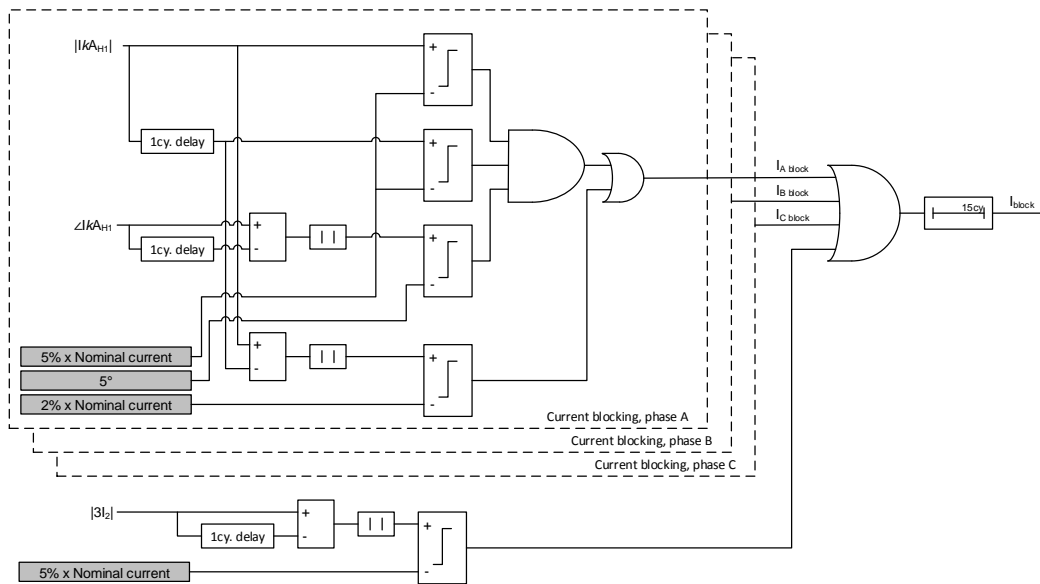


Figure 88 Current blocking for the loss of voltage detection element (LOV)

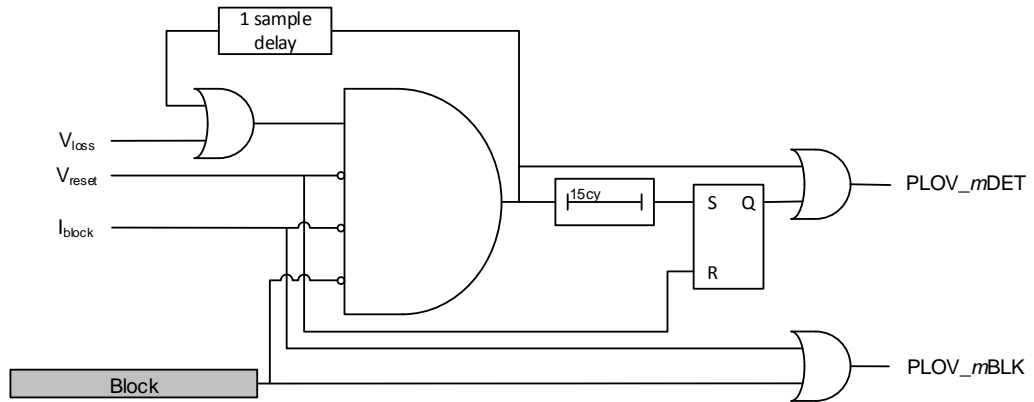


Figure 89 Output logic for the loss of voltage detection element (LOV)

SETTING	RANGE	DESCRIPTION
Block	Binary points	Binary point blocking the detection
CER detection	None; Rising; Falling; Both	Event triggered by the detection binary point, according to the chosen level
CER block	None; Rising; Falling; Both	Event triggered by the block binary point, according to the chosen level
Voltage input	Configured three-phase V (fixed)	Voltage input used
Current input	None; configured I	Current input used

Table 33 Loss of voltage detection element settings

7

METERING, SANITY CHECK AND
RECORDING

7 METERING, SANITY CHECK AND RECORDING

This chapter describes the metering, sanity check and recording functionalities available in the relays of the ALP-4000 series. The first section describes how the summed inputs work. The second section outlines the metering carried out by the relay. The third section details the sanity checks continuously performed by the relay. Finally, the last section describes the chronological events recorder of the relay.

7.1. SUMMED INPUTS

Some transformer protection schemes require the summing of two or more physical current inputs. The protection relay computes this sum itself in order to save on cabling and lower the burden of the current transformers in the substation.

It is possible to compute two different sums including each up to six physical current inputs. However, in one sum, the physical current inputs must be three-phase inputs and must have the same type of current transformers. The raw data of the physical current inputs is adjusted according to the input that has the highest current transformer ratio. The total secondary value for a summed current input is shown in equation (7) for a sum including the six physical current inputs. Only the current protection elements can use the summed inputs.

$$SI_x = \frac{RTC_1}{RTC_{MAX}} I_1 + \frac{RTC_2}{RTC_{MAX}} I_2 + \frac{RTC_3}{RTC_{MAX}} I_3 + \frac{RTC_4}{RTC_{MAX}} I_4 + \frac{RTC_5}{RTC_{MAX}} I_5 + \frac{RTC_6}{RTC_{MAX}} I_6 \quad (7)$$

7.2. METERING

The protection relay performs many real-time measurements from the raw currents and voltages sampled at a frequency of 7680 Hz (128 samples/cycle) for a grid frequency of 60 Hz. This raw data is filtered to produce the many operating quantities used in the relay. The filtered data is computed at a rate of 960 Hz (16 computations/cycle) and shown on

the *Metering* page of the web server. The data on the metering pages is refreshed once per second. Table 34 Metering done by the ALP-4000 lists the metering done in the relay.

PAGE	METERING	UNIT
Three-phase current Virtual three-phase current inputs #1 to #6	Frequency	Hz
	Phase A/B/C total RMS value	A (pri/sec ⁵)
	Phase A/B/C fundamental RMS value	A (pri/sec ⁵)
	Phase A/B/C fundamental angle value	degrees
	Phase A/B/C 2 nd harmonic RMS value	A (pri/sec ⁵)
	Phase A/B/C 4 th harmonic RMS value	A (pri/sec ⁵)
	Phase A/B/C 5 th harmonic RMS value	A (pri/sec ⁵)
	Positive sequence RMS value	A (pri/sec ⁵)
	Positive sequence angle value	degrees
	Negative sequence RMS value	A (pri/sec ⁵)
	Negative sequence angle value	degrees
	Zero sequence RMS value	A (pri/sec ⁵)
	Zero sequence angle value	degrees
	Three-phase voltage Virtual three-phase voltage inputs #1 and #2	Frequency
Phase A-N/B-N/C-N total RMS value		V (pri/sec ⁵)
Phase A-N/B-N/C-N fundamental RMS value		V (pri/sec ⁵)
Phase A-N/B-N/C-N fundamental angle value		degrees
Positive sequence RMS value		V (pri/sec ⁵)
Positive sequence angle value		degrees
Negative sequence RMS value		V (pri/sec ⁵)
Negative sequence angle value		degrees
Zero sequence RMS value		V (pri/sec ⁵)
Zero sequence angle value		degrees
Inputs/Outputs	Logic state of the inputs #1 to #16	--
	Logic state of the outputs #1 to #16	--

⁵ User can select display in primary or secondary value of the CT or PT

	Logic state of the high-speed power outputs #1 to #8	--
	Logic state of the alarm output	--
Differential current	Frequency	Hz
	Phase A/B/C operation current	P.U.
	Phase A/B/C restraint current	P.U.
	Phase A/B/C 2 nd harmonic operation current	P.U.
	Phase A/B/C 4 th harmonic operation current	P.U.
	Phase A/B/C 5 th harmonic operation current	P.U.

Table 34 Metering done by the ALP-4000 series

7.2.1. GRID FREQUENCY COMPUTATION AND TRACKING

Grid frequency is measured from a Clarke transform performed on the raw data of a current or voltage input, which can be selected on the *Frequency* page of the *ALP Config* software. Computation is done on raw data using a zero-crossing algorithm, which is filtered and validated to avoid abrupt frequency shifts. Frequency computation can range from 30 to 90 Hz.

Frequency computation is enabled only if the magnitude of a phasor calculated from the Clarke transform is greater than the minimum threshold set on the *Frequency* page of the *ALP Config* software. If the grid frequency cannot be accurately measured, the relay shows 0 Hz in the *Frequency* fields of the *Metering* pages of the web server and the local HMI.

To obtain accurate current and voltage measurements, the sampling frequency of the relay must adapt to the grid frequency in order to keep a raw data sampling rate of 128 samples/cycle. The relay can adapt its sampling frequency to grid frequencies within 40 to 75 Hz. If frequency tracking is not enabled on the *Frequency* page of the *ALP Config* software or the minimum magnitude condition is not respected, the relay assumes a 60 Hz grid frequency and sets the sampling rate accordingly. It is important to note that if frequency tracking is not enabled, the voltage and current measurements may not respect the specifications.

7.3. SANITY CHECK SYSTEM

The protection relay is equipped with a sanity check system of the system integrity. Many subsystems of the relay are monitored by this system in order to detect material faults that could be in the device. When in use, the protection relay has four system health states: normal, in problem, inhibited and locked. When the sanity check system detects one or more problems, the protection relay goes to state *In fault*; in this situation the alarm output remains deactivated and the protection elements are enabled and functional. However, it is possible for some secondary functionalities, e.g. the oscillographs, to be interrupted.

When a problem that could prevent the proper running of the protection elements is detected, but that this problem is temporary, the protection relay goes to state *Inhibited*. In this situation, the protection elements are disabled, the communication with the inputs and outputs boards is interrupted and the alarm output is activated, but the states of the outputs remain unchanged. When the problem disappears, the relay goes back to state *Normal*.

Finally, when a problem that could prevent the proper running of the protection elements is detected, and this problem is permanent, the protection relay goes to state *Locked*. When the relay is locked, the protection elements are disabled, the communication with the inputs and outputs boards is interrupted and the alarm output is activated, but the states of the outputs remain unchanged. Only a human intervention can bring back the relay to its normal state. If such is the case, please contact the manufacturer's support team. Table 35 summarizes the system health states.

STATE	PROBLEM	LED STATE	PROTECTION ELEMENTS	OUTPUT STATE	ALARM OUTPUT STATE	NOTE
Normal	-	Green	Enabled	-	Inactive	-
In fault	Problem detected	Amber	Enabled	-	Inactive	Secondary functionalities potentially interrupted
Inhibited	Temporary problem detected	Red	Disabled	Unchanged	Active	Return to normal mode upon problem disappearance
Locked	Permanent problem detected	Red	Disabled	Unchanged	Active	Human intervention needed to return to normal state

Table 35 System health states

The user has three ways to learn about the system health state. Firstly, complete information about the system health is available on the *Maintenance* page of the web server. By clicking the *Global* link on the left of the page, the web server displays the system health in a table, along with other pertinent information on the relay. If a problem is detected, a link named *Details* will appear next to the system health status. By clicking this link, additional information about the problem is displayed. Also on the *Maintenance* page, the *System Health* link displays a table filled with all the elements monitored by the continuous diagnostic system and their respective state.

Secondly, partial information about the system health can be found on the local HMI. The system health LED shows the overall state of the sanity check. When the LED is green, the relay is in state *Normal*. When the LED is amber, the relay is in state *In fault*. When the LED is red, the relay is in state *Inhibited* or *Locked*. Also, a summary of the information shown on the *Maintenance* page can be displayed on the local HMI situated on the front panel of the relay. This summary is available in the *Maintenance* menu, under *System Health*.

Thirdly, system health is available via the DNP3 communication protocol. One binary point indicates the relay has an active alarm, another indicates that it is in state *Inhibited*, while a third indicates the relay is in state *Locked*.

When the relay is in state *Locked*, and all of the problems have been solved, it is possible to unlock it. When this operation is possible, a link named *Unlocking* is displayed on the *Maintenance* page of the web server. Unlocking the relay is also possible via the local HMI in the *Maintenance* menu, under *System Health* and then *Unlocking*.

7.4. CHRONOLOGICAL EVENTS RECORDER

The report of the chronological events recorder (CER) can be accessed on the *Events* page of the web server. This report can contain up to 1000 events divided in five categories : *Protection*, *Security*, *Settings*, *Maintenance*, *Process* and *Others*. If the CER is full, older events are replaced with newer ones. Table 36 describes the event categories.

CATEGORY	DESCRIPTION
Protection	Enabled CER settings in the configuration file
Security	Web server and local HMI security, e.g. opening a session, modifying a password
Settings	Ethernet connection, COMTRADE format and web server inactivity delay
Maintenance	Sanity check
Process	Sanity check
Others	All other events

Table 36 Event categories description

For each event, the CER displays its identification number, its creation date and time, its category, its description and links to the details and oscillograms pages, if applicable. For *Protection* events, the details page displays a subset of the metering and the relay settings at the moment of the event. For other categories, the details page displays more information about the event.

8

SETTINGS AND PROGRAMMING

8 SETTINGS AND PROGRAMMING

8.1. ALP CONFIG SOFTWARE

The *ALP Config* software allows the user to configure most settings in the relay. Figure 90 shows the graphical user interface of *ALP Config*. The tree menu on the left pane of the GUI lists all the available setting pages. When tree item is selected, a page displaying all available settings for this item is shown on the right pane of the GUI. The software automatically verifies the data entered by the user and displays a message if an error occurs. An additional verification is done when the file is saved. The saved file is based on the SCL format and has an *.icd* extension.

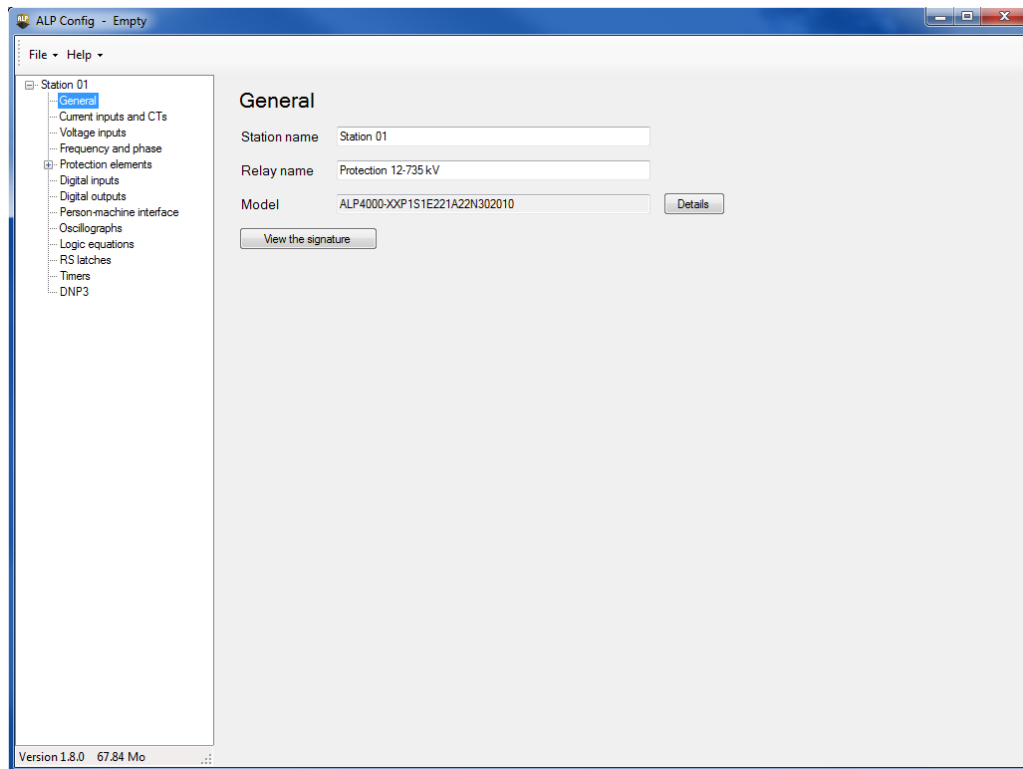


Figure 90 *ALP Config* software

8.2. PRINTING THE SETTINGS

The *ALP Config* software gives the user the option to print the settings with the *Print* function available in the *File* menu. The configuration is shown as an HTML file in a print preview dialog. It is also possible to save the HTML file on disk with the *Export configuration* function available in the *File* menu.

8.3. RELAY MODEL

When a new configuration file is created, the software requires the model number of the relay on which the file will be transferred. According to the options selected by the user, the software produces the appropriate model number. Please note that once the model number is set, there is no way to change it. The correct options must therefore be chosen. For more information on the grid frequency computation and tracking, please see section 7.2.1.

8.4. IDENTIFICATION

The first item in the tree, *General*, allows the user to set the station name and relay name. This information is shown on the local HMI and on the web server. This setting page also allows the user to view the model number details and the file signature.

8.5. CURRENT INPUTS

The *Current inputs* page allows the user to set the characteristics of each CT linked to the physical current inputs. It also lets the user choose which physical current inputs are included in the summed inputs. To be summed together, the physical current inputs must have the same type of current transformer, but can have different nominal currents (1A or 5A). Only the enabled current and summed inputs can be used by the protection elements. Disabling an input used by a protection element triggers a warning message. Table 37 lists all the available settings on the *Current inputs* page.

SETTING	RANGE	DESCRIPTION
---------	-------	-------------

CT connection	Wye; Delta	Connection type of the CT connected to the current input
CT ratio	1 – 50 000	Ratio of the CT connected to the current input
Summed inputs	I1 to I6	Physical current inputs included in the sum

Table 37 Current inputs settings

8.6. TRANSFORMER

The *Transformer* page allows the user to configure all settings related to the transformer to protect, such as its power rating, the line-to-line voltage of the lines linked to the physical current inputs, and the amplitude and angular correction factors. These settings are shown in table 38

SETTING	RANGE	DESCRIPTION
Power rating	1 – 5000 MVA	Power rating of the transformer to protect
Line-to-line voltage	1 – 1 000 kV	Line-to-line voltage of the line connected to the current input
Tap computation	Automatic Manuel	Automatic: computation based on the line-to-line voltage, ratio and power rating settings Manual : tap value entered by the user
Tap	0.7-74.0	Amplitude compensation factor for the current input
Angular compensation	-150° - 180°	Angular compensation for the current input

Table 38 Transformer settings

8.7. VOLTAGE INPUTS

The *Voltage inputs* page allows the user to enable the voltage inputs and set the characteristics of the PTs connected to them. Only the enabled voltage inputs can be used by the protection elements. Disabling a voltage input used by a protection element triggers a warning message.

8.8. DELTA CONNECTION USAGE

The *Voltage inputs* and *Current inputs* pages described in sections 8.5 and 8.7 allow the user to specify if transformers connected to an input are using Wye or Delta connections.

For protection functions, this setting only has an effect when calculations use a common base, like for the transformer differential protection element (see section 6.2.1.1). For other protections that operate mainly on secondary values, this setting has no impact.

These settings also have an impact on measurements displayed in the local HMI, the remote HMI and the chronological event recorder. When an input uses a delta connection, the transformer ratio used to convert secondary values in primary values is divided by $\sqrt{3}$. Moreover, primary angle values are compensated, depending on both the connection used on the measured input and the connection used on the angular reference input according to this table:

ANGULAR REF. CONNECTION	MEASURED INPUT CONNECTION	APPLIED COMPENSATION
Wye	Wye	0°
Wye	Delta	-30°
Delta	Wye	+30°
Delta	Delta	0°

Tableau 1 Applied compensation for the display of primary values

As for oscillograms, these contain only secondary values but also include a transformer ratio for each channel. When an input is delta connected, this ratio is divided by $\sqrt{3}$. However, the COMTRADE format does not allow the application of an offset to transform a secondary angle into a primary angle. Users must be careful of this detail when viewing an oscillogram in a software that supports primary value display.

8.9. FREQUENCY AND ANGLE

The *Frequency and angle* page allows the user to configure the settings used in the frequency computation and tracking, as well as set the angular reference used in all angle measurements. Disabling the frequency computation when frequency protection elements are enabled triggers a warning message.

8.10. PROTECTION AND CONTROL ELEMENTS

The pages under the *Protection elements* and *Control elements* tree items allow the user to configure all settings related to a protection or control element available in the relay. To learn more about the settings of a specific protection or control element, please refer to chapter 6 .

8.11. OUTPUTS

The *Outputs* page allows the user to associate each of the 16 outputs and 8 high-speed power outputs with a binary point as well as set an event trigger with the *CER* setting.

8.12. INPUTS

The *Inputs* page allows the user to set a debouncing filter for each input (see section 3.2.3), as well as set an event trigger with the *CER* setting.

8.13. HUMAN-MACHINE INTERFACE

The *Human-machine interface* page allows the user to configure the programmable LEDs, buttons LEDs and the trip LED. For each LED, it is possible to associate a binary point with the color red and another with the color green. When one of the binary points is at logic state 1, the LED will light red or green, accordingly. If both binary points are at logic state 1, the LED will light amber. Also, an event trigger can be set for each button with the *CER* setting.

8.14. OSCILLOGRAPHS

The relay allows the user to set 10 oscillographs producing oscillograms in the COMTRADE file format. To enable an oscillograph, one must set the trigger binary point and other settings, as described in Table 39. The maximum recording length of an oscillogram is 5 seconds. If the oscillogram storage space is full, older recordings are overwritten. The oscillograms can be accessed via the chronological events recorder (CER). Each recording of an oscillogram automatically produces an event in the *Protection* category. In addition to the *Details* link, a link named *Oscillo* is displayed in the corresponding column of the report. This link allows the user to download the COMTRADE files. Data is recorded in secondary values; however, oscillograms contain transformer ratios for each channel for use with software that support translation to primary values. Since raw and filtered data are not sampled at the same rate (7680 Hz vs 960 Hz), two separate oscillograms are produced for each trigger for a total of 6 downloadable files (header, configuration and data files for each trigger). It is also possible to download all files simultaneously via a zip archive. Once downloaded, it is possible to view the oscillograms with any COMTRADE viewer software.

SETTING	RANGE
Binary point	All binary points of the relay
Detection level	Positive/Rising; Negative/Falling; Both
Before (ms)	0 – 5000 ms ⁶
After (ms)	0 – 5000 ms ⁶

Table 39 Oscillograph settings

8.15. LOGIC EQUATIONS

The *Logic equations* page allows the user to set control logic equations for the relay. Therefore, it is possible to tailor the behavior of the protection elements to the specific practices and needs of the user.

The logic equations can contain a maximum of 300 logic elements. These logic elements consist of the binary points, the logic operators and the logic equations themselves. Four

⁶ The sum of *Before* and *After* cannot be more than 5 seconds.

logic operators are supported: AND, OR, NOT and XOR. The operator precedence is, from the highest to the lowest priority: NOT, XOR, AND and OR. However, evaluation of elements between parentheses has priority over the operator evaluation.

Programming a logic equation is done by entering it under the column *Logic Equation* on the *Logic equations* page. By default, the logic equations are named as *LOGIC_xy*, where *xy* is a number from 1 to 50, but it is possible to personalize their name by entering it in the appropriate column. The new name will then be used in the list of binary points available in the *ALP Config* software. It is possible to trigger an event by setting the *CER* setting in the corresponding column.

When entering a logic equation, the user must respect the following constraints :

1. The name of a logic equation must have a maximum of 16 alphanumeric characters; including the underscore,
2. The name must not include blank spaces,
3. The name must always begin with a letter;
4. The logic equation must never be empty;
5. The logic equation must not have more than 255 characters;
6. The logic equation must only include existing binary points
7. The order in which the logic equations are entered determines their processing order.

8.16. RS LATCHES

The *RS latches* page allows the user to set a latch which maintains a logic state related to its binary point settings. To program the latches, a binary point must be set for the set (S) signal and another for the reset (R) signal. Both signals cannot be associated with the same binary point. A switching level (high or low) must also be set for both signals. Signal R has priority over signal S. The latch outputs are assigned to binary points named *LATCH_xy*, where *xy* is a number between 01 and 15. Figure 91 shows the latch behavior for all possible combinations of the R and S trigger levels.

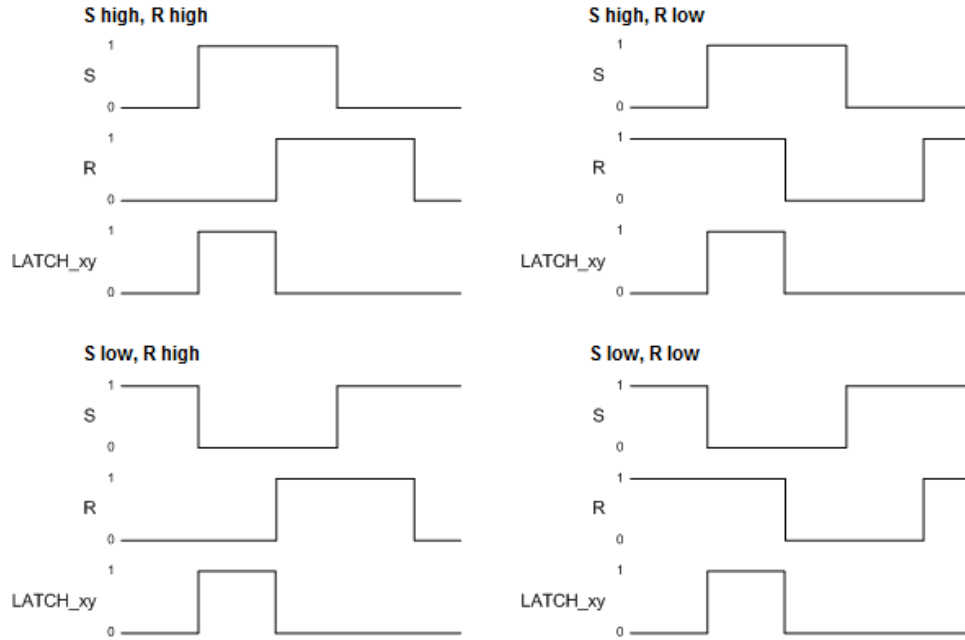


Figure 91 RS latch behavior

8.17. TIMERS

The *Timers* page allows the user to set a timer which delays or maintains the logic state of its binary point setting. To program the timers, a trigger binary point and a trigger type must be set. Four trigger types are available : *High level*, *Low Level*, *Rising edge* and *Falling edge*. Two time settings are available: pickup time and dropout time. Both have a range of 0 to 100s. The timer outputs are assigned to binary points named *TIMER_{xy}*, where xy is a number between 01 and 15. Figure 92 shows the timer behavior for each trigger type. For the *Rising edge* and *Falling edge* types, if the binary point is triggered again before the timer returns to zero, these additional triggers will be ignored.

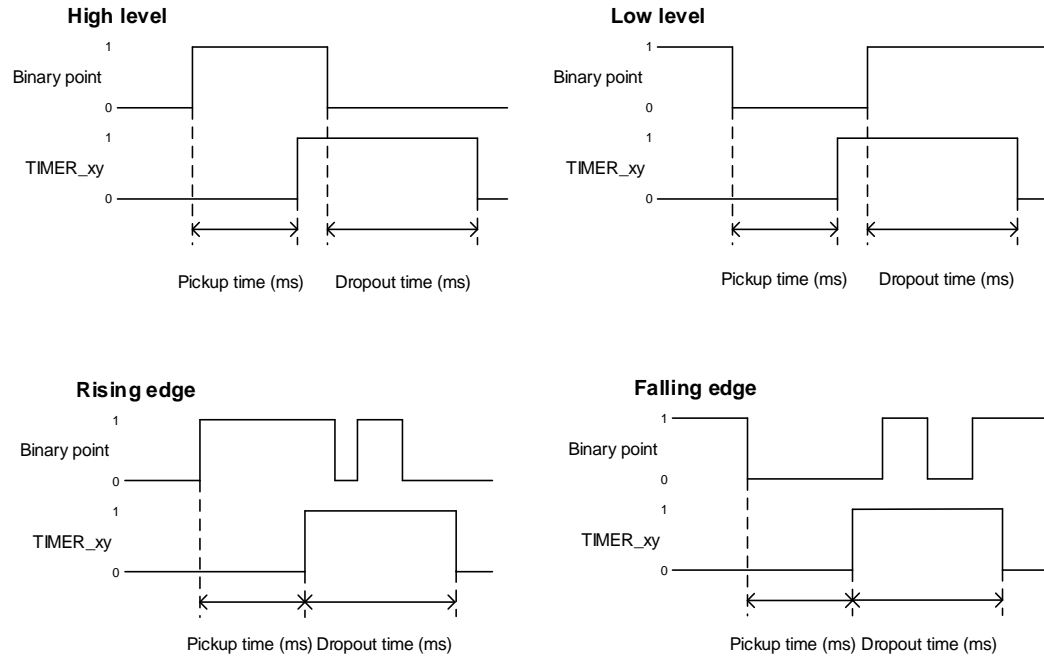


Figure 92 Timer behavior

8.18. DNP3

The *DNP3* page allows the user to set the two instances of the DNP3 communication protocol used in the relay. For more information on the DNP3 communication protocol, please refer to section 11.1.

On the page, tabs *Instance 1* and *Instance 2* allow the configuration of settings specific to each instance of the protocol. The only constraint is that the TCP port be different for each instance. Tabs *Event Queue*, *Default Variations*, *Binary Inputs*, *Binary Outputs* and *Analog Inputs* apply to all instances of the protocol. The following constraints apply to tabs *Binary Inputs*, *Binary Outputs* and *Analog Inputs*:

1. The Name and Description fields are read-only
2. In each tab, the index must be unique
3. To be reported in an event class, a point must be included in class 0

9

WEB SERVER

9 WEB SERVER

The relays of the ALP-4000 series include a web server which uses HTTPS and serves as the main HMI. The server has 6 primary pages used for different purposes: *Home*, *Metering*, *Events*, *Settings*, *Maintenance* and *Security*.

9.1. ACCESS LEVEL

The functionalities a user can access depend on his access level. Table 40 lists all the access levels and their privileges.

PAGE	ADMINISTRATION	SETTINGS	MONITORING
Home	X	X	X
Metering	X	X	X
Events	X	X	X
Settings	X	X	Viewing only
Maintenance	X	Viewing only	Viewing only
Security	X		

Table 40 Web server access level privileges

9.2. DESCRIPTION OF THE PRIMARY PAGES

The *Metering* and *Events* pages are described in sections 7.2 and 7.4, respectively. The *Settings* page allows the user to transfer a new configuration file to the relay, as well as view and download the active configuration currently in the relay.

The *Maintenance* page contains links to pages offering various functionalities and information. The *Global* link displays general information about the relay, such as its

system health status, time sync status, software and hardware versions, and date and time programmed in the relay. The *System health* link displays the state of the Ethernet ports and of the continuous diagnostic system, which is described in section 7.3. The *Time Sync* link displays the state of IRIG-B synchronization and allows an *Administration* user to modify the date and time of the relay if the IRIG-B connection is disabled or inexistant. The *Version* link displays information about the software and hardware versions of the components of the relay. The *COMTRADE* link allows the user to set the COMTRADE format of the files produced by the relay. The *Commissioning* link allows the *Administration* and *Settings* users to force the state of the outputs to verify their wiring. The *Update* link allows the *Administration* user to update the firmware of the relay.



WARNING: While using the *Commissioning* tool, the relay should not be in use. It is also recommended to use an empty configuration file. Failure to respect these recommendations may result in severe damage to your station.

The *Security* page allows the *Administration* user to change the password for all access levels as well as change the session timeout which is used to disconnect inactive users from the local HMI and web server.

10 LOCAL HMI

10 LOCAL HMI

The local human-machine interface of the relays of the ALP-4000 series is situated on its front panel. It consists of programmable and fixed LEDs and buttons, as well a graphical LCD screen.

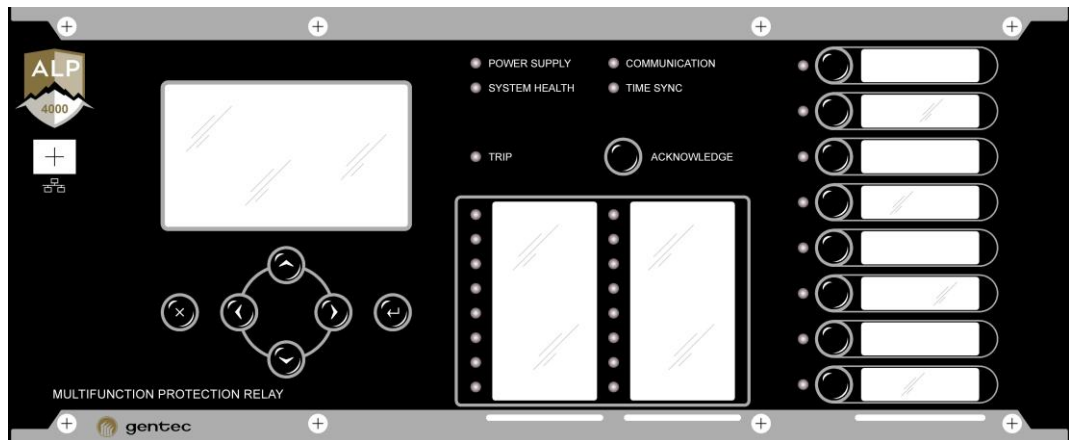


Figure 93 ALP-4000 front panel

10.1. FIXED LEDS AND BUTTONS

The local HMI of the protection relay has five fixed LEDs and seven fixed buttons. One of these buttons is used to acknowledge the latched LEDs (*Trip*, *System Health* and the set programmable LEDs). The remaining six fixed buttons are used to navigate through the menus shown on the LCD screen. The fixed LEDs can have three colors: green, red and amber. Table 41 describes what each color means for each fixed LED. Each LED and button has a corresponding binary point in the relay. It is therefore possible for each LED and button to drive a LED, a output or serve as an operand in a logic equation.

LED	GREEN	RED	AMBER	OFF
Power supply	Normal	In problem	Relay starting	---
Communication	At least one port is linked to a network	---	---	No port is linked to a network
System health	No problems	Relay locked	Active warning	Relay starting
Time sync	Connected IRIG-B source	Unconnected IRIG-B source	---	Relay starting
Trip	---	Trip since last acknowledgement; stays red until acknowledged.	---	No trip since last acknowledgement

Table 41 Fixed LEDs description

The active warnings when the System health LED is amber are for the following potential errors:

- Communication with the digital boards
- Communication with the analog boards
- Monitoring of the digital and high-speed power outputs
- Internal circuitry

10.2. PROGRAMMABLE LEDES AND BUTTONS

The local HMI of the protection relay has eight programmable buttons and their LEDs, as well as sixteen programmable LEDs. The LEDs can have three colors: green, red and amber. Programming of the LEDs and buttons is done via the ALP Config software (see section 8.13 for more details). Each LED and button has a corresponding binary point in the relay. It is therefore possible for each LED and button to drive a LED, a output or serve as an operand in a logic equation.

10.3. LCD SCREEN

The LCD screen of the protection relay can display measurements and system health information, and be used to configure the Ethernet ports settings. The measurements displayed are the total primary RMS values for each phase of each enabled three-phase analog input. To navigate through the pages, use the fixed buttons available below the screen: up, down, left, right, escape and enter. The Ethernet configuration steps are described in section 4.6.1. The system health information displayed on the local HMI is described in section 7.3.

11

COMMUNICATIONS

11 COMMUNICATIONS

11.1. DNP3

DNP3 is an open specification communication protocol allowing its users to monitor and control a system process remotely. In the first half of the 90s, it was developed by private interests and was afterwards turned into an open specification, to be used free of royalties. The protocol was designed as a solution to a lack of interoperability between manufacturers. Before DNP3, multiple proprietary protocols were used and interoperability between manufacturers was virtually nonexistent.

Since then, the DNP3 specification has become the IEEE 1815 standard. Its use is widespread in North America, in Australia and in the United Kingdom, mainly by power utilities, but also in water and sanitary utilities. Its use has shown, and still shows, that it is a reliable and efficient protocol.

It is assumed that the user reading the following sections has basic knowledge about the operation of DNP3. To get acquainted with the protocol, it is preferable to read the introduction (clause 0) of the IEEE 1815-2012 standard which gives an excellent overview of the history and of the operating principles found in the DNP3 protocol.

The next sections will present the implementation details of DNP3 for the relay.

11.1.1. GENERAL INFORMATION

DNP3 communicates using any enabled Ethernet port of the relay using the TCP/IP protocol. Two independent instances of the DNP3 protocol can be configured. Each instance has to be configured with a different TCP port. Only one master may connect to each instance at a time.

It is possible to set the communication configuration parameters for each instance independently. However, event queue configuration, default variations and data point lists are the same for all instances.

11.1.2. DNP3 POINTS

The protection relay uses three types of DNP3 objects: Binary Inputs, Binary Outputs and Analog Inputs. Each of these object types can be reported using a static object group, giving the current value of a point, and/or an event object group, giving significant changes. It is possible to configure the DNP3 variation used by default for each of these object groups.

The configuration software also allows, for each available data point in the device, the setting of its index, whether it is included in class 0 response, and whether its events are reported in class1/2/3.

When a Binary Input or Output is configured to be reported in an event class, all its value changes will be added to event queues. For Analog Inputs, two mechanisms can limit the number of events that will be reported. First, it is possible to configure a deadband to define the amplitude of value change that is significant enough to trigger an event. Second, Analog Inputs also have a refresh delay of 100 milliseconds at a minimum. If more than 50 Analog Inputs are configured to be reported in class 1, 2 or 3, this refresh delay increases to 1 second.

11.1.3. DNP3 COMMAND

The Binary Outputs of the protection relay can be controlled using DNP3. Each output is latched; at all times; an output has a 0 or 1 state. Receiving a *Latch ON* or *Pulse - Close* control sets the output to 1 and receiving a *Latch OFF* or *Pulse – Trip* resets it to 0. *Pulse* controls are not supported.

Three types of outputs are available on the protection relay. The two first types allow control of the Outputs and the High-speed power outputs. These 16 and 8 points, respectively, allow remote assertion of one of the real outputs of the relay. Functionally, the logic level of a DNP3 Binary Output is combined with the binary point set to the corresponding real output using an OR gate.

The third type allows control of binary registers. These registers are virtual data points that can be used as binary points elsewhere in the device settings. For example, they can be used in logic equations, to block a protection element, to trigger an oscillograph, etc...

11.1.4. INTEROPERABILITY LEVEL

The DNP3 implementation used in the relay fulfills all requirements for interoperability subset level 2 described in the IEEE 1815-2012 standard.

The implementation also includes features that go beyond this level. If the master station used conforms strictly to level 2, special care must be taken when specifying the relay DNP3 settings to avoid using the features that are not required for level 2. Among others, when the master is limited to level 2, it is not recommended to configure Binary Outputs in an event class. Moreover, it is possible that level 2 masters do not support Analog Input Event variations 3, 4, 5 and 7 (floating point variations and timestamps).

For the same reasons, when connecting a DNP3 level 3 master to the protection relay, the master must be configured to limit its request to the supported features, as described in the interoperability table included in the relay DNP3 Device Profile.

11.1.5. DNP3 DEVICE PROFILE

In order to provide a way to check for interoperability between DNP3 devices, the DNP Users Group provides a standard DNP3 Device Profile that is used to give information about supported features, available settings and limits for each device.

The relay DNP3 Device Profile can be obtained in two ways. First, a default device profile is distributed with this manual. It contains all the information about supported features and the device default settings.

Second, it is possible to export a DNP3 Device Profile from a device configuration using the *ALP Config* software. In this case, the profile contains not only the supported features, but also the device DNP3 settings, as specified by the user.

11.1.6. SETTINGS

Tables 42 to 51 explain the settings and their value range for the DNP3 implementation used in the relay.

SETTING	RANGE	DESCRIPTION
Enable	Enabled – Disabled	Indicates whether this DNP3 instance is enabled or disabled.
TCP listening port	0 – 65535	Local TCP port on which the DNP3 instance will be listening for an incoming connection.
Local UDP port	0 – 65535	Local UDP port on which the DNP3 instance will be listening for broadcast requests. A 0 value indicates that the UDP port is disabled.
Accepts source addresses	0 – 255 or *	IP addresses from which TCP connection requests or UDP packets will be accepted. An asterisk indicates that all values will be accepted.
TCP keep-alive timer	1 second – 596 hours	Indicates the period at which Link Status Requests will be sent when the link is idle. If no response is received, the link will be closed.

Table 42 DNP3 Instance settings – IP Parameters

SETTING	RANGE	DESCRIPTION
Data link address	0 – 65519	DNP3 local link address for this instance.
RX timeout – Complete frame	0 – 2147483647	Reception timeout for a complete DNP3 frame starting from detection of a frame start, in milliseconds. If the frame is not completely received within this timeout, the received bytes will be ignored.
Link layer confirmations	Never, Sometimes or Always	Indicates whether this DNP3 instance has to request link layer confirmations from the master. <i>Sometimes</i> means that link layer confirmations are required only for application fragments spanning more than one link layer frame. NOTE: The <i>DNP Users Group</i> strongly discourages the use of link layer confirmations. This setting should always be configured to <i>Never</i> .
Link layer confirmation timeout	0 – 2147483647	Reception timeout for link layer confirmation starting from when a frame is sent, in milliseconds. This setting is used when link layer confirmations are enabled and for the TCP keep-alive timer.
Maximum data link retries	0 – 255	Maximum retries for a link layer frame following a link layer confirmation timeout. After a timeout on the last retry, the concerned TCP connection is closed.

Table 43 DNP3 Instance settings – Data Link Layer

SETTING	RANGE	DESCRIPTION
Application confirmation timeout	0 – 2147483647	Reception timeout for an application layer confirmation starting from when a fragment is sent, in milliseconds. This timeout applies when an application confirmation is requested either for a response to a request or for an unsolicited response.
Select timeout	0 – 600	Reception timeout for an operate request starting from the reception of a valid select request, in seconds. If the operate request is received after this timeout expires, the control will be refused.
Application confirmations – multi-fragments responses	Enabled – Disabled	Indicates if application confirmations are required for fragments other than the last in a multi-fragment response. If this setting is enabled, the protocol will wait for a confirmation to be received before sending a new fragment. If this setting is disabled, the protocol will request a confirmation only when required by the standard (e.g. if the fragment contains events).

Table 44 DNP3 instance settings – Application Layer

SETTING	RANGE	DESCRIPTION
Enable	Enabled – Disabled	Indicates if this DNP3 instance has to support unsolicited responses. If enabled, the instance will send a null response upon startup (e.g. when a new configuration file is sent to the device). Before sending unsolicited responses containing events, a request to enable unsolicited responses must be received from the master.
Master data link address	0 – 65519	DNP3 Link Layer address where unsolicited responses will be sent.
Unsolicited retries	0 – 65535	Maximum retries for an unsolicited response after application confirmation timeout.
Retry delay	0 – 2147483647	Delay between an unsolicited response application confirmation timeout and its retry, in milliseconds.

Table 45 DNP3 Instance settings – Unsolicited Responses

SETTING	RANGE	DESCRIPTION
Number of class 1 events	1 – 255	Indicates how many class 1 events must be added to the Event queues to trigger an unsolicited response. NOTE: An unsolicited response could be sent with less events upon expiry of the hold time – class 1.
Number of class 2 events	1 – 255	Indicates how many class 2 events must be added to the Event queues to trigger an unsolicited response.

Number of class 3 events	1 – 255	NOTE: An unsolicited response could be sent with less events upon expiry of the hold time – class 2. Indicates how many class 3 events must be added to the Event queues to trigger an unsolicited response.
Hold time after class 1 event	0 – 2147483647	NOTE: An unsolicited response could be sent with less events upon expiry of the hold time – class 3. Maximum delay between queuing of a class 1 event and the trigger of an unsolicited response.
Hold time after class 2 event	0 – 2147483647	NOTE: An unsolicited response could be sent before the hold time is expired if the event queues contain more than the number of class 1 events setting. Maximum delay between queuing of a class 2 event and the trigger of an unsolicited response.
Hold time after class 3 event	0 – 2147483647	NOTE: An unsolicited response could be sent before the hold time is expired if the event queues contain more than the number of class 2 events setting. Maximum delay between queuing of a class 3 event and the trigger of an unsolicited response.

Table 46 DNP3 Instance settings – Unsolicited Responses Trigger Conditions

SETTING	RANGE	DESCRIPTION
Queue size	1 – 65535	Indicates the maximum event queue size for each type of object that can be buffered in each of the DNP3 instances.
Event reporting mode	All events – Only most recent	Indicates the behavior of the event queue. When <i>All events</i> are selected, multiple value or flag changes can be stored in the queue, each with a timestamp. When <i>Only most recent</i> is selected, a given data point will only be present once in the queue; only the most recent event will be kept.

Table 47 DNP3 Event Queue settings

SETTING	RANGE	DESCRIPTION
Default Variation	Variable according to the object group	Indicates for each object group the preferred variation to be included in a response if the master does not explicitly specify a variation.

Table 48 DNP3 Default Variations settings

SETTING	RANGE	DESCRIPTION
Index	0 – 65534	Indicates the DNP3 index of the Binary Input.
Name	–	Read-only field containing the name of the Binary Input in the protection relay.
Description	–	Read-only field providing a functional description for the Binary Input.
Included in class 0	Enabled – Disabled	Indicates if the current value of the Binary Input must be included in response to a class 0 request received from a master. Even if the point is not included in class 0, it will still be possible to retrieve it using a read request for group 1.
Event class	Not reported Class 1 Class 2 Class 3	Indicates in which class the events occurring for a Binary Input will be reported (i.e. a change of value and/or flags).

Table 49 DNP3 Binary Inputs settings

SETTING	RANGE	DESCRIPTION
Index	0 – 65534	Indicates the DNP3 index of the Binary Output used for monitoring and control.
Name	–	Read-only field containing the name of the Binary Output in the protection relay.
Description	–	Read-only field providing a functional description for the Binary Output.
Included in class 0	Enabled – Disabled	Indicates if the current value of the Binary Output must be included in response to a class 0 request received from a master. Even if the point is not included in class 0, it will still be possible to retrieve it using a read request for group 1.
Event class	Not reported Class 1 Class 2 Class 3	Indicates in which class the events occurring for a Binary Output will be reported (i.e. a change of value and/or flags).
Command allowed	Enabled – Disabled	Indicates if DNP3 control requests will be accepted (enabled) or refused (disabled) for the Binary Output.

Table 50 DNP3 Binary Outputs settings

SETTING	RANGE	DESCRIPTION
Index	0 – 65534	Indicates the DNP3 index of the Analog Input.
Name	–	Read-only field containing the name of the Analog Input in the protection relay.
Description	–	Read-only field providing a functional description for the Analog Input.
Included in class 0	Enabled – Disabled	Indicates if the current value of the Analog Input must be included in response to a class 0 request received from a master. Even if the point is not included in class

		0, it will still be possible to retrieve it using a read request for group 1.
Event class	Not reported Class 1 Class 2 Class 3	Indicates in which class the events occurring for an Analog Input will be reported (i.e. a change of value and/or flags).
Deadband	Positive floating point number	Indicates what constitutes a significant value change in order to generate an event. Deadband is set as a floating point value and is applied on the corresponding floating point value of the point as it is published by DNP3 floating point variations. When the variation used is of integer type, the integer value is first converted to a floating point value using the scale and offset specified in the DNP3 Device Profile for the Analog Input, before applying the deadband.

Table 51 DNP3 Analog Inputs settings

12

BINARY POINTS

12

BINARY POINTS

BINARY POINT	RANGE	DESCRIPTION
SYSTEM RELATED		
ALARM_REL	--	Alarm
ALARM_REL_ST	--	Alarm relay status
DIAG_MAINTEMP	--	Main board temperature error
DIAG_EXT_FLSH	--	External flash memory error
DIAG_PPS	--	Pulse per second synchronization error
INHIBIT_ST	--	Inhibit status
LOCK_ST	--	Locked status
MAIN_SUPPLY_ST	--	Main power supply voltage low
REL_OFF	--	Full deactivation of outputs
REL_OFF_ST	--	Status of full deactivation of outputs
TEST_LED	--	LED test
WARN_ALL_SUP	--	Warning for all power supplies
WARN_SUP5_0	--	Warning 5.0V power supply
WARN_SUP3_3	--	Warning 3.3V power supply
WARN_SUP2_5	--	Warning 2.5V power supply
WARN_SUP1_8	--	Warning 1.8V power supply
WARN_SUP1_2	--	Warning 1.2V power supply
WARN_SUP1_0	--	Warning 1.0V power supply
WARNING	--	General warning
INPUTS, OUTPUTS AND HIGH-SPEED POWER OUTPUTS		
BI_xy	01 to 32	Inputs 01 to 16 (17 to 32 are for future expansion)
BO_Pxy	01 to 32	High-speed power outputs 01 to 08 (09 to 32 are for future expansion)
BO_Rxy	01 to 32	Outputs 01 to 16 (17 to 32 are for future expansion)
BR_xy	01 to 40	Binary registers 01 to 40 command (DNP3)
OBO_Pxy	01 to 32	High-speed power outputs 01 to 08 (09 to 32 are for future expansion) command (DNP3)
OBO_Rxy	01 to 32	Outputs 01 to 32 (17 to 32 are for future expansion) command (DNP3)

BUTTONS

BTN_x	1 to 8	Programmable buttons
BTN_ACK		Acknowledge button
BTN_D		Down button
BTN_ENT		Enter button
BTN_ESC		Escape button
BTN_L		Left button
BTN_R		Right button
BTN_U		Up button

LATCHES, LOGIC EQUATIONS AND TIMERS

LATCH_xy	01 to 15	RS latches outputs
LOGIC_xy	01 to 50	Logic equations outputs, if the default name was kept
Custom name	--	Logic equations outputs, if custom names were used
TIMER_xy	01 to 15	Timers outputs

LEDS

LED_xy_G	01 to 16	Programmable LEDs - Green
LED_xy_R	01 to 16	Programmable LEDs - Red
LED_BTNx_G	1 to 8	Programmable button LEDs - Green
LED_BTNx_R	1 to 8	Programmable button LEDs - Red
LED_COMM_c	G, R	Communication LED – Green or Red
LED_PWR_c	G, R	Power supply LED – Green or Red
LED_SYNC_c	G, R	Time sync LED – Green or Red
LED_SYS_c	G, R	System health LED – Green or Red
LED_TRIP_c	G, R	Trip LED – Green or Red

PROTECTION ELEMENTS

P24_xy_S	xy: 01 to 03	24 element Start binary point of instance xy
P25_xy_T	xy: 01 to 03	24 element Trip binary point of instance xy
P27_xy_pS	xy: 01 to 06 p: A,B,C	27 element Start binary point for phase p of instance xy
P27_xy_pT	xy: 01 to 06 p: A,B,C	27 element Trip binary point for phase p of instance xy
P27_xyS	01 to 06	27 element Start binary point for instance xy: OR of the three P27_xy_pS binary points of instance

		<i>xy</i>
P27_xyT	01 to 06	27 element Trip binary point for instance <i>xy</i> : OR of the three P27_xy_pT binary points of instance <i>xy</i>
P50_xy_pS	<i>xy</i> : 01 to 10 <i>p</i> : A,B,C	50 element Start binary point for phase <i>p</i> of instance <i>xy</i>
P50_xy_pT	<i>xy</i> : 01 to 0 <i>p</i> : A,B,C	50 element Trip binary point for phase <i>p</i> of instance <i>xy</i>
P50_xyS	01 to 10	50 element Start binary point for instance <i>xy</i> : OR of the three P50_xy_pS binary points of instance <i>xy</i>
P50_xyT	01 to 10	50 element Trip binary point for instance <i>xy</i> : OR of the three P50_xy_pT binary points of instance <i>xy</i>
P50N_xyS	01 to 06	50N element Start binary point for instance <i>xy</i>
P50N_xyT	01 to 06	50N element Trip binary point for instance <i>xy</i> :
P51_DT_xy_pS	<i>xy</i> : 01 to 10 <i>p</i> : A,B,C	51_DT element Start binary point for phase <i>p</i> of instance <i>xy</i>
P51_DT_xy_pT	<i>xy</i> : 01 to 0 <i>p</i> : A,B,C	51_DT element Trip binary point for phase <i>p</i> of instance <i>xy</i>
P51_DT_xyS	01 to 10	51_DT element Start binary point for instance <i>xy</i> : OR of the three P51_DT_xy_pS binary points of instance <i>xy</i>
P51_DT_xyT	01 to 10	51_DT element Trip binary point for instance <i>xy</i> : OR of the three P51_DT_xy_pT binary points of instance <i>xy</i>
P51_IT_xy_pS	<i>xy</i> : 01 to 10 <i>p</i> : A,B,C	51_IT element Start binary point for phase <i>p</i> of instance <i>xy</i>
P51_IT_xy_pT	<i>xy</i> : 01 to 0 <i>p</i> : A,B,C	51_IT element Trip binary point for phase <i>p</i> of instance <i>xy</i>
P51_IT_xyS	01 to 10	51_IT element Start binary point for instance <i>xy</i> : OR of the three P51_IT_xy_pS binary points of instance <i>xy</i>
P51_IT_xyT	01 to 10	51_IT element Trip binary point for instance <i>xy</i> : OR of the three P51_IT_xy_pT binary points of instance <i>xy</i>
P51N_DT_xyS	01 to 06	51N_DT element Start binary point for instance <i>xy</i>
P51N_DT_xyT	01 to 06	51N_DT element Trip binary point for instance <i>xy</i> :
P51N_IT_xyS	01 to 06	51N_DT element Start binary point for instance <i>xy</i>
P51N_IT_xyT	01 to 06	51N_DT element Trip binary point for instance <i>xy</i> :
P59_xy_pS	<i>xy</i> : 01 to 06 <i>p</i> : A,B,C	59 element Start binary point for phase <i>p</i> of instance <i>xy</i>
P59_xy_pT	<i>xy</i> : 01 to 06 <i>p</i> : A,B,C	59 element Trip binary point for phase <i>p</i> of instance <i>xy</i>
P59_xyS	01 to 06	59 element Start binary point for instance <i>xy</i> : OR of the three P59_xy_pS binary points of instance <i>xy</i>
P59_xyT	01 to 06	59 element Trip binary point for instance <i>xy</i> : OR of the three P59_xy_pT binary points of instance <i>xy</i>

P81_xyS	01 to 06	81 element Start binary point for instance <i>xy</i>
P81_xyT	01 to 06	81 element Trip binary point for instance <i>xy</i> .
P81R_xyS	01 to 06	81R element Start binary point for instance <i>xy</i>
P81R_xyT	01 to 06	81R element Trip binary point for instance <i>xy</i> .
P87_12O3BLK	--	Block binary point for the <i>2-out-3</i> blocking type
P87_1pBLK	<i>p</i> : A,B,C	Result of the blocking or restraint computations for phase <i>p</i>
P87_1pSEC	<i>p</i> : A,B,C	Intermediary secure blocking binary point for phase <i>p</i>
P87_1pT	<i>p</i> : A,B,C	Intermediary Trip binary point for phase <i>p</i>
P87_1CMNBLK	--	Block binary point for the <i>Common</i> blocking type
P87_1CMNT	--	Intermediary Trip binary point for phase <i>p</i> for the <i>Common</i> blocking type
P87_1INDp	<i>p</i> : A,B,C	Intermediary Trip binary point for phase <i>p</i> for the <i>Per Phase</i> blocking type
P87_1R	--	87R element Trip binary point
P87_1T	--	87 element Trip binary point: OR of binary points P87_1R and P87_1U
P87_1U	--	87U element Trip binary point
PDIR_xy_pF	<i>xy</i> : 01 to 06 <i>p</i> : A,B,C	Phase directional element Forward direction binary point for phase <i>p</i> of instance <i>xy</i>
PDIR_xy_pR	<i>xy</i> : 01 to 06 <i>p</i> : A,B,C	Phase directional element Reverse direction binary point for phase <i>p</i> of instance <i>xy</i>
PDIR_xyF	01 to 06	Phase directional element Forward direction binary point for instance <i>xy</i> : OR of the three PDIR_xy_pF binary points of instance <i>xy</i>
PDIR_xyR	01 to 06	Phase directional element Reverse direction binary point for instance <i>xy</i> : OR of the three PDIR_xy_pR binary points of instance <i>xy</i>
PLOV_xyDET	<i>xy</i> : 01 to 02	Loss of voltage detection element Detection binary point for instance <i>xy</i>
PLOV_xyBLK	<i>xy</i> : 01 to 02	Loss of voltage detection element Blocked binary point for instance <i>xy</i>
PVPD_xy_pS	<i>xy</i> : 01 to 06 <i>p</i> : A,B,C	VPD element Start binary point for phase <i>p</i> of instance <i>xy</i>
PVPD_xy_pT	<i>xy</i> : 01 to 06 <i>p</i> : A,B,C	VPD element Trip binary point for phase <i>p</i> of instance <i>xy</i>
PVPD_xyS	01 to 06	VPD element Start binary point for instance <i>xy</i> : OR of the three PVPD_xy_pS binary points of instance <i>xy</i>
PVPD_xyT	01 to 06	VPD element Trip binary point for instance <i>xy</i> : OR of the three PVPD_xy_pT binary points of instance <i>xy</i>
TRIP	--	OR of the Trip binary points of all configured protection elements

Table 52 List of binary points used in the ALP-4000 series

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ANALOG DATA

13 ANALOG DATA

ANALOG DATA	RANGE	DESCRIPTION
CURRENT INPUTS		
I_x_H1_MAG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> fundamental phasor magnitude for current input <i>x</i>
I_x_H1_ANG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> fundamental phasor angle for current input <i>x</i>
I_x_RMS_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> total RMS value for current input <i>x</i>
I_x_POS_MAG	x: 1 to 6	Positive sequence magnitude for current input <i>x</i>
I_x_POS_ANG	x: 1 to 6	Positive sequence angle for current input <i>x</i>
I_x_NEG_MAG	x: 1 to 6	Negative sequence magnitude for current input <i>x</i>
I_x_NEG_ANG	x: 1 to 6	Negative sequence angle for current input <i>x</i>
I_x_ZERO_MAG	x: 1 to 6	Zero sequence magnitude for current input <i>x</i>
I_x_ZERO_ANG	x: 1 to 6	Zero sequence angle for current input <i>x</i>
I_x_H2_MAG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> 2 nd harmonic phasor magnitude for current input <i>x</i>
I_x_H2_ANG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> 2 nd harmonic phasor angle for current input <i>x</i>
I_x_H4_MAG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> 4 th harmonic phasor magnitude for current input <i>x</i>
I_x_H4_ANG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> 4 th harmonic phasor angle for current input <i>x</i>
I_x_H5_MAG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> 5 th harmonic phasor magnitude for current input <i>x</i>
I_x_H5_ANG_p	x: 1 to 6 p: A,B,C	Phase <i>p</i> 5 th harmonic phasor angle for current input <i>x</i>
SUMMED INPUTS		
S_{ix}_H1_MAG_p	x: 1 to 4 p: A,B, C	Phase <i>p</i> fundamental phasor magnitude for summed input <i>x</i>
S_{ix}_H1_ANG_p	x: 1 to 4 p: A,B, C	Phase <i>p</i> fundamental phasor angle for summed input <i>x</i>
S_{ix}_RMS_p	x: 1 to 4 p: A,B, C	Phase <i>p</i> total RMS value for summed input <i>x</i>
S_{ix}_POS_MAG	x: 1 to 4	Positive sequence magnitude for summed input <i>x</i>
S_{ix}_POS_ANG	x: 1 to 4	Positive sequence angle for summed input <i>x</i>
S_{ix}_NEG_MAG	x: 1 to 4	Negative sequence magnitude for summed input <i>x</i>
S_{ix}_NEG_ANG	x: 1 to 4	Negative sequence angle for summed input <i>x</i>
S_{ix}_ZERO_MAG	x: 1 to 4	Zero sequence magnitude for summed input <i>x</i>
S_{ix}_ZERO_ANG	x: 1 to 4	Zero sequence angle for summed input <i>x</i>

VOLTAGE INPUTS		
VI_H1_MAG_px	x: 1 to 2 p: A,B,C	Phase <i>p</i> fundamental phasor magnitude for voltage input <i>x</i>
VI_H1_ANG_px	x: 1 to 2 p: A,B,C	Phase <i>p</i> fundamental phasor angle for voltage input <i>x</i>
VI_RMS_px	x: 1 to 2 p: A,B,C	Phase <i>p</i> total RMS value for voltage input <i>x</i>
VI_POS_MAG_x	x: 1 to 2	Positive sequence magnitude for voltage input <i>x</i>
VI_POS_ANG_x	x: 1 to 2	Positive sequence angle for voltage input <i>x</i>
VI_NEG_MAG_x	x: 1 to 2	Negative sequence magnitude for voltage input <i>x</i>
VI_NEG_ANG_x	x: 1 to 2	Negative sequence angle for voltage input <i>x</i>
VI_ZERO_MAG_x	x: 1 to 2	Zero sequence magnitude for voltage input <i>x</i>
VI_ZERO_ANG_x	x: 1 to 2	Zero sequence angle for voltage input <i>x</i>
DIFFERENTIAL PROTECTION ELEMENTS		
DIF_OP_p	p: A,B,C	Phase <i>p</i> operation current for the differential protection elements
DIF_REST_p	p: A,B,C	Phase <i>p</i> restraint current for the differential protection elements
DIF_H2_OP_p	p: A,B,C	Phase <i>p</i> 2 nd harmonic current for the differential protection elements
DIF_H4_OP_p	p: A,B,C	Phase <i>p</i> 4 th harmonic current for the differential protection elements
DIF_H5_OP_p	p: A,B,C	Phase <i>p</i> 5 th harmonic current for the differential protection elements
FREQUENCY		
FREQ	--	Measured frequency
SAMPLING_FREQ	--	Sampling frequency
SYSTEM RELATED		
TEMPERATURE	--	Internal temperature
SUP_5_0	--	5.0V power supply
SUP_3_3	--	3.3V power supply
SUP_2_5	--	2.5V power supply
SUP_1_8	--	1.8V power supply
SUP_1_2	--	1.2V power supply
SUP_1_0	--	1.0V power supply
MAIN_SUP_UNIT	--	Main power supply unit
MAIN_SUP_VOLT	--	Main power supply
IRIGB_STATE	--	IRIG-B synchronization state

WARN_IOCE	--	Input/output communication warning
WARN_ACSE	--	Analog communication warning
WARN_ICE	--	Internal communication error
WARN_INTEGRITY	--	System integrity warning
DIAG_NVSRAM	--	nvSRAM memory error
LOCK	--	Relay locked
ADC_COMM_RTY	--	Analog boards communication retry
IO_COMM_RTY	--	Digital boards communication retry
INHIBIT_ST	--	Relay inhibited
DIAG_RTC_SPI	--	External SPI clock error

Table 53 List of the analog data used in the ALP-4000 series

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14.4. GETTEXT

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"Source code" for a work means the preferred form of the work for making modifications to it. For a library, complete source code means all the source code for all modules it contains, plus any associated interface definition files, plus the scripts used to control compilation and installation of the library.

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- The modified work must itself be a software library.
- You must cause the files modified to carry prominent notices stating that you changed the files and the date of any change.
- You must cause the whole of the work to be licensed at no charge to all third parties under the terms of this License.
- If a facility in the modified Library refers to a function or a table of data to be supplied by an application program that uses the facility, other than as an argument passed when the facility is invoked, then you must make a good faith effort to ensure that, in the event an application does not supply such function or table, the facility still operates, and performs whatever part of its purpose remains meaningful.

(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must be optional: if the application does not supply it, the square

root function must still compute square roots.)

These requirements apply to the modified work as a whole. If identifiable sections of that work are not derived from the Library, and can be reasonably considered independent and separate works in themselves, then this License, and its terms, do not apply to those sections when you distribute them as separate works. But when you distribute the same sections as part of a whole which is a work based on the Library, the distribution of the whole must be on the terms of this License, whose permissions for other licensees extend to the entire whole, and thus to each and every part regardless of who wrote it.

Thus, it is not the intent of this section to claim rights or contest your rights to work written entirely by you; rather, the intent is to exercise the right to control the distribution of derivative or collective works based on the Library.

In addition, mere aggregation of another work not based on the Library with the Library (or with a work based on the Library) on a volume of a storage or distribution medium does not bring the other work under the scope of this License.

3. You may opt to apply the terms of the ordinary GNU General Public License instead of this License to a given copy of the Library. To do this, you must alter all the notices that refer to this License, so that they refer to the ordinary GNU General Public License, version 2, instead of to this License. (If a newer version than version 2 of the ordinary GNU General Public License has appeared, then you can specify that version instead if you wish.) Do not make any other change in these notices.

Once this change is made in a given copy, it is irreversible for that copy, so the ordinary GNU General Public License applies to all subsequent copies and derivative works made from that copy.

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4. You may copy and distribute the Library (or a portion or derivative of it, under Section 2) in object code or executable form under the terms of Sections 1 and 2 above provided that you accompany it with the complete corresponding machine-readable source code, which must be distributed under the terms of Sections 1 and 2 above on a medium customarily used for software interchange.

If distribution of object code is made by offering access to copy from a designated place, then offering equivalent access to copy the source code from the same place satisfies the requirement to distribute the source code, even though third parties are not compelled to copy the source along with the object code.

5. A program that contains no derivative of any portion of the Library, but is designed to work with the Library by being compiled or linked with it, is called a "work that uses the Library". Such a work, in isolation, is not a derivative work of the Library, and therefore falls outside the scope of this License.

However, linking a "work that uses the Library" with the Library creates an executable that is a derivative of the Library (because it contains portions of the Library), rather than a "work that uses the Library". The executable is therefore covered by this License. Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file that is part of the Library, the object code for the work may be a derivative work of the Library even though the source code is not. Whether this is true is especially significant if the work can be linked without the Library, or if the work is itself a library. The threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data structure layouts and accessors, and small macros and small inline functions (ten lines or less in length), then the use of the object

file is unrestricted, regardless of whether it is legally a derivative work. (Executables containing this object code plus portions of the Library will still fall under Section 6.)

Otherwise, if the work is a derivative of the Library, you may distribute the object code for the work under the terms of Section 6. Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

6. As an exception to the Sections above, you may also combine or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

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b) Use a suitable shared library mechanism for linking with the Library. A suitable mechanism is one that (1) uses at run time a copy of the library already present on the user's computer system, rather than copying library functions into the executable, and (2) will operate properly with a modified version of the library, if the user installs one, as long as the modified version is interface-compatible with the version that the work was made with.

c) Accompany the work with a written offer, valid for at least three years, to give the same user the materials specified in Subsection 6a, above, for a charge no more than the cost of performing this distribution.

d) If distribution of the work is made by offering access to copy from a designated place, offer equivalent access to copy the above specified materials from the same place.

e) Verify that the user has already received a copy of these materials or that you have already sent this user a copy.

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e) Provide Installation Information, but only if you would otherwise be required to provide such information under section 6 of the GNU GPL, and only to the extent that such information is necessary to install and execute a modified version of the Combined Work produced by recombining or relinking the Application with a modified version of the Linked Version. (If you use option 4d0, the Installation Information must accompany the Minimal Corresponding Source and Corresponding Application Code. If you use option 4d1, you must provide the Installation Information in the manner specified by section 6 of the GNU GPL for conveying Corresponding Source.)

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You may charge a fee for the physical act of transferring a copy, and you may at your option offer warranty protection in exchange for a fee.

2. You may modify your copy or copies of the Library or any portion of it, thus forming a work based on the Library, and copy and distribute such modifications or work under the terms of Section 1 above, provided that you also meet all of these conditions:

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- b) You must cause the files modified to carry prominent notices stating that you changed the files and the date of any change.
- c) You must cause the whole of the work to be licensed at no charge to all third parties under the terms of this License.
- d) If a facility in the modified Library refers to a function or a table of data to be supplied by an application program that uses the facility, other than as an argument passed when the facility is invoked, then you must make a good faith effort to ensure that, in the event an application does not supply such function or table, the facility still operates, and performs whatever part of its purpose remains meaningful.

(For example, a function in a library to compute square roots has a purpose that is entirely well-defined independent of the application. Therefore, Subsection 2d requires that any application-supplied function or table used by this function must

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These requirements apply to the modified work as a whole. If identifiable sections of that work are not derived from the Library, and can be reasonably considered independent and separate works in themselves, then this License, and its terms, do not apply to those sections when you distribute them as separate works. But when you distribute the same sections as part of a whole which is a work based on the Library, the distribution of the whole must be on the terms of this License, whose permissions for other licensees extend to the entire whole, and thus to each and every part regardless of who wrote it.

Thus, it is not the intent of this section to claim rights or contest your rights to work written entirely by you; rather, the intent is to exercise the right to control the distribution of derivative or collective works based on the Library.

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This option is useful when you wish to copy part of the code of the Library into a program that is not a library.

4. You may copy and distribute the Library (or a portion or derivative of it, under Section 2) in object code or executable form under the terms of Sections 1 and 2 above provided that you accompany it with the complete corresponding machine-readable source code, which must be distributed under the terms of Sections 1 and 2 above on a medium customarily used for software interchange.

If distribution of object code is made by offering access to copy from a designated place, then offering equivalent access to copy the source code from the same place satisfies the requirement to distribute the source code, even though third parties are not compelled to copy the source along with the object code.

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14.11. XML 2

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15 ACRONYMS

ACRONYM	DEFINITION
AC	Alternative Current
ACT	Ethernet Activity
ALP	Local Protection Automatism
AWG	American Wire Gauge
BNC	Bayonet Neill–Concelman
CER	Chronological Events Recorder
CISPR	Special International Committee on Radio Interference
COMTRADE	Common Format for Transient Data Exchange
DC	Direct Current
DIR	Phase directional element
DNP3	Distributed Network Protocol
ECA	Element Characteristic Angle
HMI	Human-Machine Interface
HTTPS	Hypertext Transfer Protocol Secure
HSP	High-speed power
ICD	IED Capability Description
IEC	International Electrotechnic Commission
IED	Intelligent Electronic Device
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
IRIG-B	Inter Range Instrumentation Group, standard B
LED	Light-Emitting Diode
LK	Ethernet Link

Table 54 List of acronyms used in the manual

ACRONYM	DEFINITION
LOV	Loss Of Voltage
SCL	Substation Configuration Language
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
V/I_{RMS}	Signal's total RMS value
VPD	Voltage Peak Detector

Table 55 List of acronyms used in the manual (continued)