DESIGNING WITH SWITCHING AMPLIFIERS FOR PERFORMANCE AND RELIABILITY

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Introduction

The switching audio amplifier, while representing a departure from conventional linear audio amplifier technology, nevertheless presents a very manageable design task to the OEM system designer. Switching amplifier design, however, does involve disciplines not normally associated with conventional, linear amplifiers (e.g., power DMOS transistors and RF circuitry), in that issues such as EMI, coupling, and high currents must be managed at the same time that performance and reliability are being maximized.

Tripath Technology has already specifically addressed these issues in our driver modules, reference amplifier designs, and PCB layout reference designs in order to ease the OEM system designer's task. Even with the availability of these design tools, however, significant care is required of the OEM system designer in order for the final product to work optimally. Key design considerations ultimately left for the final system design include the PC board layout, gate resistance selection, power FET and clamp diode selection, break-before-make (BBM) programming, filter selection, and heat sink selection. In this application note we will discuss these and other issues, offer some guidelines for component selection, and present some proven techniques employed in the design of a high-quality, production-worthy, audio power amplifier product.

Sections:

Section 1: Board Layout

Tripath offers customers reference design and/or sample PCB layout for various market segments. These include, but are not limited to, home entertainment, automotive, and portable applications. These reference layouts are STRONGLY recommended as high currents flowing through PCB traces can cause undesirable interactions. It is impractical to cover all possible system design issues within this one document, but some primary points of consideration are offered here. The reader should also bear in mind that any particular system design would require some layout revisions.

Bypass Capacitors

Bypass capacitors (0.1uF) should be placed between +VBB and GND, and between GND and -VBB, to minimize the loop areas shown in Figure 1. The parasitic inductances formed by these loops contribute to overshoot and undershoot voltages on the FETs during transitions.

If the bypassing is inadequate with respect to the voltage rating of the FET, these over and undershooting voltages can contribute to FET reliability problems. Furthermore, although some protection is provided within the FETs themselves, bottom side ringing can damage the driver transistors. It can also cause overcharging of the topside FET driver's bootstrap capacitor and damage the topside FET. These problems can, in part, be mitigated by the use of external Schottky or fast-recovery clamping diodes (Schottky diodes are better) but the inductance within any such diode loop must also be minimized.

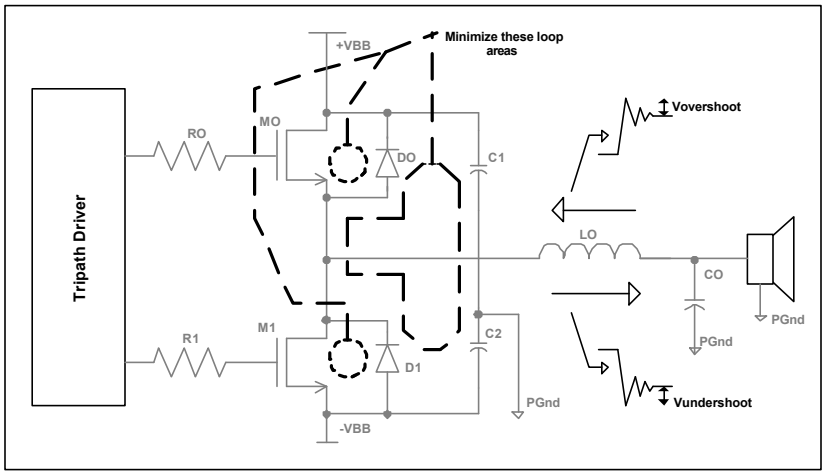

Figure 1: Output stage critical layout loops

Gate Drive Loop

Another layout area requiring consideration is the gate drive loop formed by traces connecting the driver IC, the FET gate, and FET source return to the driver IC. For the topside FET, this loop incorporates the HO driver pin, series resistor, gate-source capacitor, and VB driver pin. For the bottom side FET, the loop incorporates the LO driver pin, series resistor, gate-source capacitor and COM pin. Figure 2 shows these loops and the area that must be minimized to prevent resonant ringing with the gate and miller capacitors.

Gate ringing is undesirable as it can lead to destruction of the driver IC and/or FET gate. It can also cause the FET to turn off and on producing extra EMI and increased undesired coupling effects that can lead to oscillations and excess power dissipation.

Generally, a sound layout can resolve ringing problems associated with the gate drive loop. However, if this problem persists, a Zener diode can be placed close to the FET, connected between the gate and the source. Again, for this Zener diode to be useful, the loop formed by the gate-source and Zener must be small to reduce parasitic inductances.

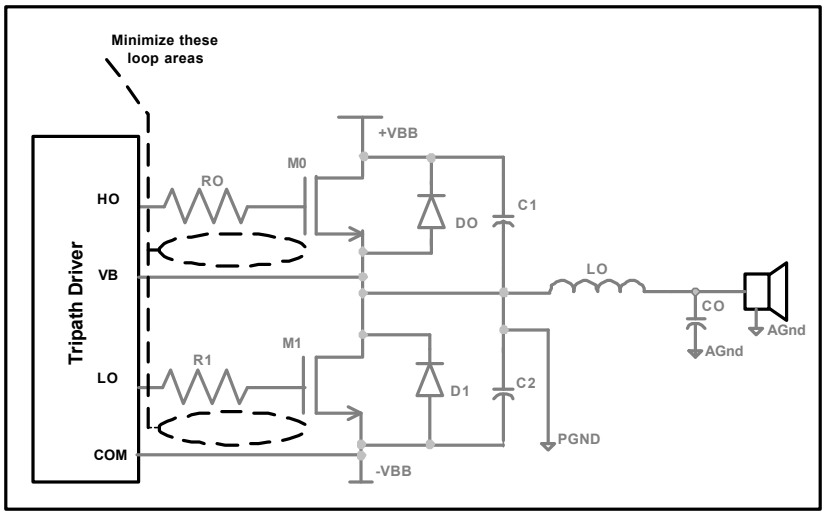

Figure 2: Driver stage critical layout loops

Kelvin Connections

Due to the large currents that flow in a power amplifier, the resistance and inductance of the metal traces cannot be ignored. For this reason, Tripath has recommended several “Kelvin” connections in its layouts (a Kelvin connection is one that goes directly to a target component’s terminals with no other connections along the same PCB trace). This prevents current from flowing through lines for a

first function causing undesired effects on a second function. For example, the large currents originating at the drain of the top side FET first pass through series metal, then past a small decoupling capacitor, through more metal, through small valued current sense resistors, through more metal, past larger capacitors, through more metal, and finally to the power supply. For this reason, the driver's over-current sensing pins (OSC_H+, OSC_H-, OSC_L+, OSC_L-) must make a Kelvin connection to the sense resistor. Traces that are best connected as Kelvin connections are summarized in Table 1. The penalty for not using Kelvin connection for these traces varies from reduced functionality (oscillations) to increased noise and/or distortion in the system, depending on the degree of violation.

Function	Trace Origin	Trace Ends At	Possible Penalty
Over current	OSC_H+	Resistor terminal	Early shutdown
Over current	OSC_H-	Resistor terminal	Early shutdown
Over current	OSC_L+	Resistor terminal	Early shutdown
Over current	OSC_L-	Resistor terminal	Early shutdown
Output Sense	FDBKN_	Inductor terminal	Extra noise
Speaker Sense	GNDKELVIN_	Speaker GND	Extra noise
Over current	OCR_	optional series R, then GNDA	Early shutdown
Input ground	AGND	Amplifier RCA jack GNDA	Extra noise

Table 1: Traces requiring Kelvin connections

Generally, Tripath recommends not connecting analog ground to power ground; this connection is done optimally in the driver. However, if this rule needs to be violated, a single line from the analog star ground to the power star ground is generally acceptable.

EMI

To optimize for system EMI, a ground fill is recommended wherever practical. This ground fill picks up field lines from the switching traces before they are allowed to radiate into free space. HOWEVER, THIS GROUND FILL SHOULD ONLY BE CONNECTED TO SYSTEM GROUND WITH A SINGLE CONNECTION AT A STAR GROUND NODE. There should be two ground fills: one for the input section connected to an input star ground point with a single trace, and one for the power section, tied to a power star ground node point with a single trace. This techniques forces currents to flow through the paths described above in a known and controlled manner, preventing undesired coupling that can degrade audio fidelity. An uncontrolled ground fill could potentially expose one to numerous problems that can be quite difficult to resolve. EMI is also effectively reduced by application of the above guidelines concerning the minimization of loop areas shown in Figures 1 and 2.

In general, any node which has high voltage and/or high current should be kept as small as possible to minimize radiation. If possible, a return current path to cancel fields (keeping the loop small) should also be placed in an adjacent position. These two adjacent traces should have an outer ground shield to pick up the remaining radiation. The ground fills described above are a convenient way to follow this shielding guideline. For more information on solving EMI issues, please refer to Tripath Application Note 9.0, "Designing for EMI Regulatory Compliance".

Section 2: Power FET and Series Gate Resistance Selection

Numerous parameters are contained within any given power FET data sheet, but only the pertinent ones for switching amplifier design are discussed here. The first parameters to consider when selecting a FET are drain-source break down voltage (BVdss), gate charge (Qg), and on-resistance (Rdson). The gate charge (the measure of gate capacitance) contributes to the power in the undesired gate resonance mentioned earlier. Since 1/2QgV must be dissipated with each gate charge/discharge to control overshoots, larger Qg's will result in a tendency towards larger gate overshoots and more power dissipation in the driver. The BVdss determines which supply voltages are possible and therefore the maximum output power.

Series Gate Resistor

Gate resonance ringing can be minimized several ways. These include placing a resistor in series with the gate to dampen overshoot, selecting FETs with less gate charge, and reducing the parasitic series gate inductance to allow for quicker dissipation (with smaller inductances, the current is larger and therefore I^2R can more quickly eliminate the gate charge power). Unfortunately, a larger series gate resistor also leads to slower gate transitions and results in more driver delay and therefore more required break-before-make (BBM) delay.

Excessive delay reduces the fidelity of the Tripath amplifier to less than optimal performance levels. With intermediate delays, high frequency distortion increases and with longer delays, the driver will not operate normally. Since the delay sensitivity depends on the specific driver product, delay-vs-performance numbers are not given here. Optimal gate resistance values can be obtained from Tripath for various Tripath products, gate charge values, and supply voltages (please refer to specific amplifier data sheet for additional information). However, these optimal numbers can be skewed if the layout has larger than normal parasitic inductance.

Small gate resistors also cause excessive heat generation in the driver. This is seen by considering a driver with a 2 Amp drive capability across 12V, allowing the user to estimate the driver Thevenin impedance as 6Ω. The power dissipated by each gate charge/discharge split between the series gate resistor and driver is fQgV where f is up to 1.2MHz. As the split between the driver and resistor is dependent on the resistor value, larger gate resistors help keep the driver cool by allowing the heat to dissipated outside of the package. For example, with a 6Ω gate resistor and a gate charge

of 70nC, the dissipation is (1.2M)(70n)(12) = 1 Watt, with an equal split of 0.5W to the driver and resistor (obviously this resistor's power dissipation rating needs to be suitably chosen). Since the driver feeds four power FETs, the total driver dissipation from the combined FET's can be as much as 2W.

Break Before Make (BBM)

Even under typical conditions the gate resistor and FETs run hot, so it is prudent to check for optimal BBM setting (which effects quiescent current) suitable for the full range of expected operating temperature. It has been observed that the BBM setting is generally required to be greatest at high temperatures in order to prevent a thermal runaway condition, wherein the FETs' own self-heating causes an increase in shoot-through current, causing the FETs to become hotter still, and so forth. A small additional amount of BBM delay provides margin for process variations, but excessive delay in BBM will adversely impact THD.

BVdss

Since there is inevitably some ringing on the power output node as shown in Figure 1, the BVdss rating of the FET needs to be selected to accommodate the voltage peaks to prevent damaged to the FET. This BVdss rating needs to be verified with the actual FET in the socket, with the lowest expected load impedance in place (at the worst case frequency for this load), under the worst thermal condition, bridged if allowed, and at the maximum possible output power. Typically, with a good layout, the FETs BVdss rating must be at least 50% higher than the power supply rails. For example, in a +/- 33V system, a 100V FET is a typical minimum required BVdss, although the actual number needed is determined by the layout and decoupling capacitors.

The voltage ringing measurement must be made with a low inductance scope probe or with a differential probe to avoid overestimating the overshoot.

Rdson

A low value of Rdson is advantageous for the obvious reason of increased efficiency and small heat sink size. It also helps prevent instantaneous overheating of the FET die inside the package. However, FETs with low Rdson also have larger parasitic components. This implies that any attempts to improve the peak efficiency by reducing Rdson usually come at the cost of reduced efficiency when the amplifier is running idle or at low output power levels. Incidentally, regarding the selection of heat sink size, it is noteworthy that unlike analog amplifiers the dissipated power delivered to the heat sink in a Tripath amplifier remains directly proportional to output power delivered to the load throughout the amplifier's power range, unless there are significant diode storage losses. In other words, the power delivered to the heat sink in a Tripath amplifier does not exhibit a peak near ½ - 2/3 of full output power as is typical of linear amplifiers.

Section 3: Clamping Diodes and Charge Storage

Clamping diodes can do more than simply prevent FET damage from ringing. They (especially Schottky diodes) are particularly useful because they reduce excessive dissipation from charge storage. Referring again to Figure 1, assume M1 is on and current is flowing out of M1's drain. Following the normal switching sequence, M1 turns off before M0 turns on to prevent shoot-through. During this intermediate time, the inductor current flows through D1. When M0 subsequently turns on, D1 has stored charge and M0 is forced to discharge D1 as it increases the output voltage. Since the voltage across M0 during this time is the full sum of the positive and negative supply voltages, this is a very lossy event.

Depending on the amount of charge stored in D1, the degree of loss will vary. For this reason, a fast-recovery diode or Schottky is generally used, the Schottky being preferred despite its usually larger capacitance. Interestingly, this issue is not a problem at low output powers (discussed in the inductor selection section).

Section 4: Low Frequency Supply Pumping

A curious but troublesome phenomenon seen within single-ended switching amplifiers is power supply "pumping." The supply pumping issue is caused by current sent "backwards" into the supply—i.e., opposite the normal current polarity. This pumps up the magnitude of the voltage in most power supplies because conventional power supplies can only provide low frequency currents in one direction.

Pumping Explanation

Figure 3 shows a single ended switching amplifier with typical power supply output stages. Since diodes D3 and D4 are in the power path, low frequency currents provided are unipolar. Consider a negative signal being produced on the speaker terminal. This produces current from ground to the negative voltage as shown. This current comes from the inductor with the same polarity, then flows through either the top or bottom side FET (as shown in dotted lines), depending which FET is on. Since the amplifier is constantly switching between each rail, this current alternates between each supply. When the output voltage goes negative, D4 accepts the current. When it goes to the positive supply, D3 is reverse-biased and C3 must accept the current. This pushes the positive supply above its desired regulation voltage and continues until the speaker voltage changes to a positive polarity. The converse situation, where the negative rail is pumped, also occurs when the speaker voltage is positive. It is important that capacitors C3 and C4 have a surge voltage rating greater than the peaks of the pumping.

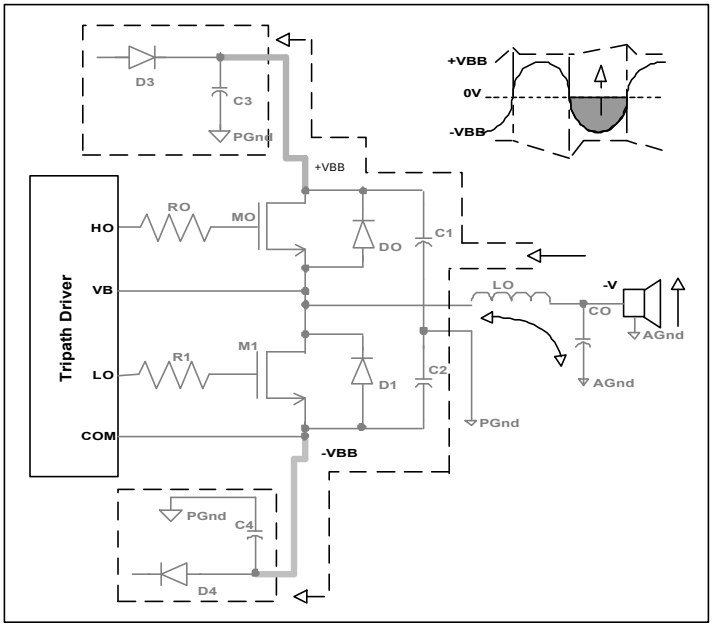

Figure 3: Low frequency supply pumping

DC Offset

The lower in frequency the signal, the longer the supply is pumped before an opposite polarity waveform discharges the capacitor, making this problem worse at low frequencies. When a system has a DC offset which is causing pumping greater than the normal quiescent current through the power FETs (typically requires >0.3V output offset with 4Ω loads), the supplies can be boosted to the point where over-voltage protection triggers. Although Tripath amplifiers have low output offset voltages to prevent this problem, a DC servo circuit guarantees that the over-voltage protection will not trigger.

Supply Capacitors

A common solution to the pumping issue is to use large supply capacitors (for example C3 and C4 each could be 4700uF or larger) to accept the pumped supply current. The low frequency pole created by the DC blocking capacitor and input resistance at the input to the driver determines the value of the supply capacitor required. The driver's input capacitor will roll off the input signal (and therefore output signal) and place a lower limit on the frequency at which supply boosting must be considered. Incidentally, when using large capacitors on the supply, care must be taken to discharge them before removing the Tripath driver as the large capacitors can retain a significant residual voltage after the power supply is turned off. Removing the driver with the supply capacitors still charged can result in driver failure.

Low Frequency Music

A workable solution to the supply pumping problem relies on the fact that music usually has low frequency information which is strongly correlated between left and right channels (i.e., it is largely in phase). This correlation can be used to eliminate the supply pumping if one intentionally places the channels out of phase at the inputs of the amplifier and restores normal phasing at the speakers as shown in Figure 4. When configured in this fashion, each channel is pumping out of phase with the other and thereby effectively cancels the pumping action of the other. This results in the net current being maintained in the desired direction from both supplies. This configuration is similar to a bridged amplifier, which does not exhibit pumping problems. However, it is not identical to a bridge configuration in that each load remains connected to ground, causing the above noted DC offset issue to remain a concern unless each channel's DC offset is coincidentally out of phase and similar in magnitude.

A desirable bonus of using the amplifier in this fashion is that no additional modification is required to configure it as a bridge configuration; the phase inversion necessary at one channel input is already in place. One simply needs to apply the same audio to both channels (configured as in Figure 4) and connect the speakers from the '+' terminal of the bottom channel to the '-' terminal of the top channel.

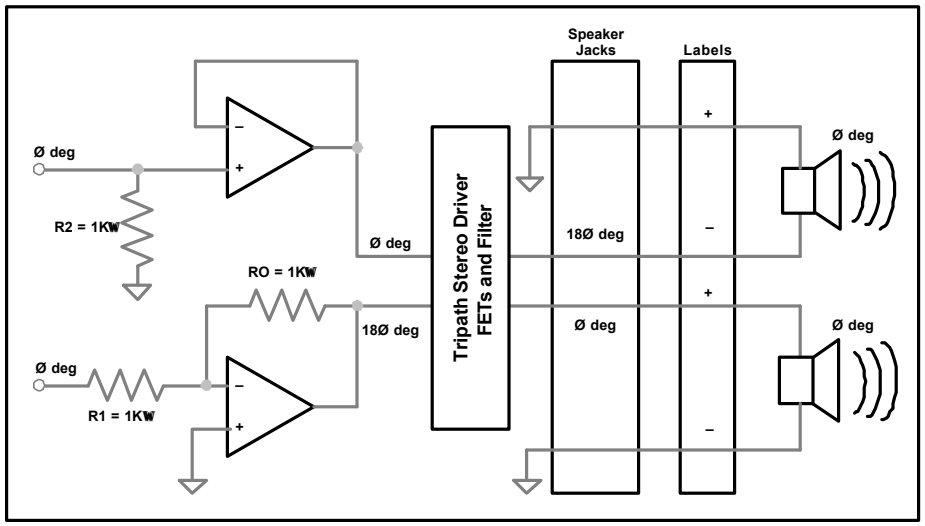

Figure 4: Power Supply Pumping Solution

Section 5: DC Offset in Mute Mode

There is normally a small DC voltage at the output of Tripath amplifiers in mute mode with no load present. The voltage is approximately 2.5V and should not be a cause for concern since its Thevenin impedance is approximately 10kΩ. This residual voltage is negligible once speakers are connected.

Section 6: Measuring THD, THD+N, IMD,..

Tripath recommends a 20kHz-30kHz high order low pass filter between the amplifier's output and any audio analyzer's input for proper measurement results. Refer to Tripath application note 6.0 for more details. Tripath also supplies a custom filter circuit at the customer's request to aid in achieving the appropriate testing bandwidth.

Lab Setup

Beyond simple filtering, a clean lab setup is also necessary in achieving accurate THD measurements. Adherence to the design guidelines in this application note will, in addition helping with reliability, also tend to optimize the amplifier for best THD.

An important consideration is to never connect earth ground to the input ground. This includes any and all instrumentation grounds such as those on oscilloscope probes. Depending on the setup, an inadvertent connection of earth ground to the amplifier input ground could allow large currents to flow through the input section of the amplifier. This can be detrimental to THD, or can even result in a destructive oscillation if the input section layout is not optimal.

Inductor Core Evaluation

Another possible source of distortion is the core of the output filter inductor. To determine if this is a source of distortion in a system, pre-filter measurements can be made (as shown in Figure 5) if the switching output is first passed through several RC filtering stages to help minimize aliasing/slewing problems with analyzers. Obviously, the roll off characteristic of the RC stage needs to be monitored before making assessments of the amplifier bandwidth or THD (attenuating the harmonics within the audio band gives artificially good measurements). Also, the input impedance of an analyzer must be configured to be significantly greater than the resistors used in the RC filter as not to affect the frequency response or to cause attenuation.

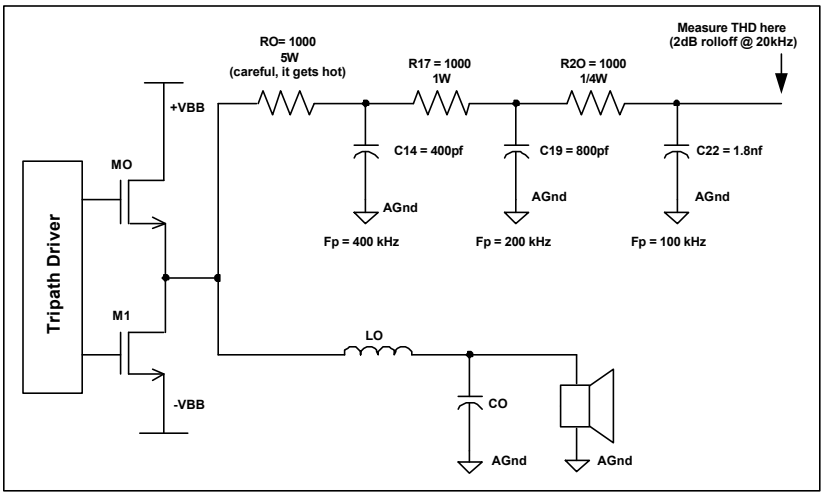

Figure 5: Example of a pre-LC anti-aliasing filter

Section 7: Filter Design

One advantage of Tripath amplifiers is the ability to use output filters having higher cutoff frequency than those in most PWM solutions. This implies that the load dependent peaking/droop in the 20kHz pass band can be made negligible. This is especially important for amplifiers that have unknown speaker loads. Furthermore, speakers do not present a purely resistive load to the amplifier and the impedance changes over frequency and speaker model. Output filters with higher cutoff frequencies are better able to accommodate these irregularities in speaker impedances.

LC Selection

Tripath recommends designing the amplifier output filter as a 2nd order, 80kHz LC filter, yielding 20kHz pass band perturbations that are 2 octaves lower than the resonance frequency. For a first pass design, a filter comprised of a 14uH inductor and a 0.28uF capacitor performs well. SPICE simulations show that this filter is centered for switching between 4Ω and 8Ω loads with +/-0.3dB pass band peaking and droop, respectively.

No Load Consideration

The case of the amplifier being operated with no load connected must also be considered. When this occurs, the damping effect of the speaker impedance is removed and the resulting voltage peaking in the LC filter is potentially huge. This produces strong resonant currents that potentially can overheat the FETs or the passive components, or even cause oscillations if the board layout is not optimal. To resolve this peaking problem, connect a capacitive coupled auxiliary load to the filter

output with a roll off at approximately 50kHz. This dampens the peaking and keeps related problems under control. Incidentally, if this auxiliary load resistor is connected to the LC node and the capacitor connected to ground (as opposed to the capacitor tied to the LC node with the resistor to ground), this forms a convenient, single pole anti-aliasing filter useful for measurement instruments. After the first pass, the filter design should be optimized with actual 4Ω and 8Ω speakers because the speakers' reactive impedance combined with the capacitively coupled auxiliary load can modify the filter's response. Tripath has achieved good results in this arena as demonstrated in customer evaluation boards using 18uH-22uH inductors combined with 0.22uF capacitors, with auxiliary RC load of 33Ω and 0.1uF.

Second LC Stage

Often, it is also desirable to add a second LC stage at the point where the speaker leads pass out of the chassis of the amplifier system to help block high frequency EMI. This is harmless to the audio, but should be designed to have a cutoff frequency that is significantly higher than the first LC stage's cutoff. This way, the intricacies of higher order filter design do not need to be pursued. Furthermore, conventional higher order filters (as opposed to two fundamentally unrelated LC stages) can have more severe speaker impedance dependencies.

Inductor Core Selection

Inductor core selection is an important design parameter when designing for high audio fidelity and low EMI. The most linear of inductors have an air core and can be used to determine the linearity of the system without concerns arising over core-related issues. However, they can become hot quickly since the eddy currents in the inner windings are prohibitively lossy and there is no metallic core doubling as a heat sink. They are also very prone to inter-inductor coupling which can cause numerous problems. Orienting the air cores orthogonal to one another mitigates crosstalk, but air core inductors remain problematic due to their tendency to produce EMI.

An ideal but relatively costly solution is to use an air-gapped core that encapsulates the windings and therefore effectively prevents EMI. More realistically, toroidal coils provide a good cost-versus-performance tradeoff. Be aware that core material selection will have a substantial effect on efficiency and linearity. Tripath currently recommends low-mu (10) type 2 iron powder cores for their low loss and high linearity.

Efficient Switching

There is an alternative filter design technique intended to increase efficiency at mid-to-high output power levels. It also illustrates an inherently low switching loss phenomena exhibited during conditions of low output power by many switching amplifiers, including Tripath's. Unfortunately, expanding this high efficiency region across the full power sweep, from low power to high output

power, is challenging to implement and causes increased idle dissipation and EMI. Nevertheless, understanding this issue is valuable because it helps the system designer grasp the various contributors to a system's efficiency. The high efficiency technique involves reducing the filter inductor to a small value (perhaps 1uH). As shown in Figure 6, where the output filter inductor is swapped in value between 4uH (CH2) and 18uH (REF1), the output LC resonant currents (which approximate a triangle wave, given that sin(x) ~= x for small values of x) become very strong. If the inductor is small enough, these currents can become greater than the peak currents going to the speaker load. This is desirable because these resonant currents change polarity with each cycle in such a fashion that they actually produce the next desired transition when the active FET is turned off. This can be understood by studying Figure 6 and noting the current measured by CH2 is positive when flowing into the power FETs from the inductor. Since the transition was caused by a change in filter inductor current instead of by a change in FET conduction, the output capacitance is charged and discharged with minimal loss. Furthermore, the body diode charge storage issue is eliminated because the full supply voltage no longer appears across the activated body diode.

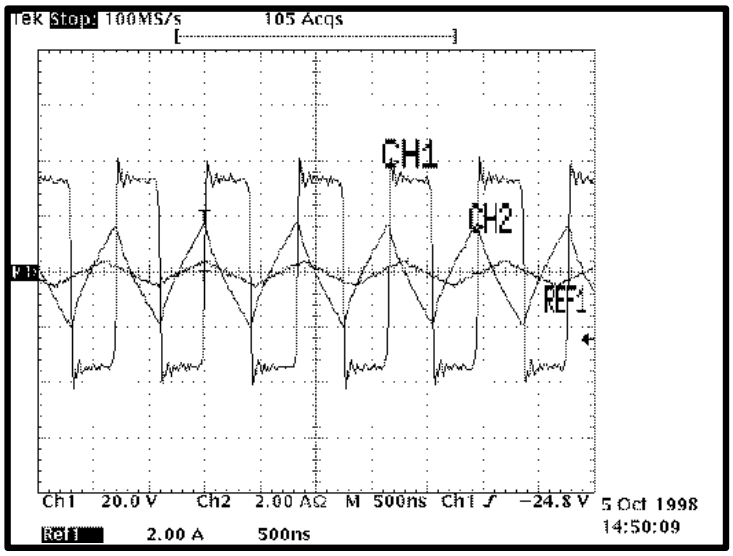

Figure 6: Switching voltage and current with 18uH inductors (CH1 and CH2) and a switching current with a 4uH inductor (REF1)

This high efficiency technique works well for moderate levels of output power. However, the constant, large resonant current causes undesired dissipation in the power FETs that is noticeable as dissipated heat. Obviously, the idle dissipation issue can be improved by using power FETs with lower Rdson, but this adds extra system cost.