Leading-Edge Memory Solutions
for UltraScale & UltraScale+ FPGAs

GSI Technology customers now have access to a free Controller IP for our SigmaQuad-IIIe™ and SigmaQuad-IVe™ SRAMs, for use with Xilinx UltraScale™ and UltraScale+™ FPGAs.

Turbocharge Your Memory Transaction Rate
- Burst of 2 (B2) and Burst of 4 (B4), x18 and x36 SRAM configurations are supported
- No bank/address restrictions up to 933 MHz—eliminates the need for complicated re-order buffers

Save Power, Pins, and Board Space vs. Competing Solutions
- Significantly lower power consumption at equivalent clock frequencies
- Fewer clock signals required—helps optimize FPGA I/O bank usage
- 14 mm x 22 mm, 260-pin BGA SRAM packaging

Example Solutions			Memory Performance			
FPGA	SRAM	Availability	Clock Speed	Read Latency	R/W Rate (max)	Data BW (x36, peak)
KU040	144Mb SQ-IIIe Quad B2	Today	800 MHz	3 cycles	1.60 GT/s	115 Gb/s
KU13P	144Mb SQ-IVe Quad B2	Spring 2017	933 MHz	5 cycles	1.86 GT/s	134 Gb/s

Note: The FPGAs listed are the specific versions GSI used or will use for validating the IP on its evaluation boards.

Controller IP Overview
- Utilizes a "4:1 Mux" configuration: SRAM clock = 4x FPGA User Interface clock
- Read Latency = ~15 FPGA User Interface clock cycles
- Validated by GSI on a KU040 evaluation board, with 800 MHz SigmaQuad-IIIe and SigmaQuad-IVe
- Verified by multiple customers with various FPGAs from the UltraScale family

www.gsitechnology.com

Questions?

Features/Downloads/Documentation:
apps@gsitechnology.com

IP Installation/Timing/Debug:
apps@gsitechnology.com

FPGA Resources Used (4:1 Configuration)

SRAM	LUT Used	Register Used	Block RAM Used
Quad B2 x18	6208	6672	0
Quad B2 x36	10216	10948	0

Engagement Process
- Review, or assist in creating, customer FPGA —> SRAM pinout
- Provide IP source code for simulation**, along with SRAM behavior model
- Provide IP source code for synthesis**/P&R/FPGA build

(**Note: IP source code is typically the same for simulation and for synthesis.)

Available Deliverables
- Controller IP Source Code (unencrypted Verilog)
- Design Constraints File
- Controller IP User Guide
- SRAM Behavioral Models, for simulation

Questions?
- Contact: apps@gsitechnology.com