SigmaQuad-IIIe™/SigmaDDR-IIIe™ Xilinx 7 Series Memory Port Product Brief

Features

- Support of up to 725 MHz I/O clock speed in a –3 commercial speed grade Xilinx 7 Series FPGA device
- Hardware Validated
- x18, x36 devices supported
- Burst of 2 words, Burst of 4 words modes supported
- Separate I/O, Common I/O devices supported
- 3.0 clock cycle read latency supported
- 2:1 and 4:1 memory to FPGA logic interface clock ratio
- Automatic signal delay skew compensation on SA, D and Q signals
- Built-in self-test with pseudo-random and incremental test patterns
- Debug support of peeking and poking GSI's IIIe memory locations, as well as 7 Series FPGA control parameters
- Memory Port IP delivered in Verilog source code with accompanying User Configuration File

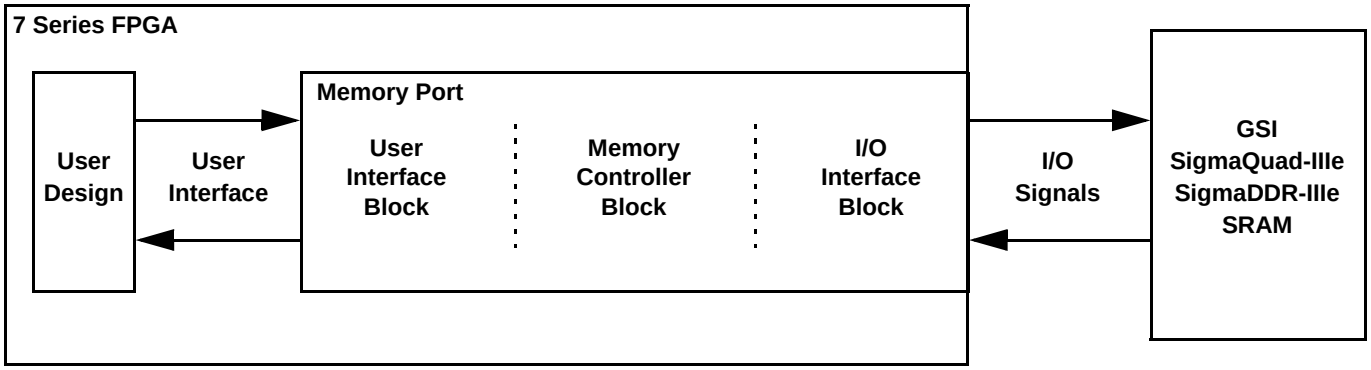
Introduction

The GSI Xilinx 7 Series Memory Port IP provides reliable high speed interfaces to the GSI SigmaQuad-IIIe and SigmaDDR-IIIe family of ECCRAM™ products. The support covers all six parts of this product family comprising the x18 and x36 versions of the Quad Burst of 2 (B2), Quad Burst of 4 (B4), and DDR Burst of 2 (B2) devices.

Functional Overview

Figure 1 shows the functional blocks of the Xilinx 7 Series FPGA Memory Port connecting a user design to GSI's SigmaQuad-IIIe or SigmaDDR-IIIe SRAM device. The physical layer side of the design connects to the SRAM device via FPGA I/O blocks, and the user interface side connects to the user design via FPGA logic.

Fig. 1: Memory Port Functional Blocks



I/O Interface Block

- Interfaces with the Memory Controller Block and translates data and control between the logic domain and physical signal domain
- Clock and data rate adaptation between the I/O signals and the Memory Controller logic because the FPGA core clock frequency is either 1/2 or 1/4 of the I/O clock
- Synchronizes Control and data signals between the FPGA clock domain and the I/O clock domain
- Performs I/O signal calibration under the control of the Memory Controller to adjust the I/O signal delay taps
- Identifies the valid window of the I/O signals and center the delay tap on the valid window

Memory Controller Block

- Accepts calibration commands from the user interface block and feeds back result and status
- Runs the calibration algorithm to control the I/O delay tap in the I/O Interface Block and verifies the calibration result
- Performs memory test using built-in pseudo random, incremental and fixed test patterns

User Interface Block

- Receives core logic clock and delay tap reference clock from the user design
- Accepts calibration commands from the user design and feeds back results and status
- Reports I/O delay tap values of calibrated signals to the user design
- Buffers memory read/write commands and data
- Accepts memory test commands from the user design and report results