

SigmaQuad-II+™/SigmaDDR-II+™

Xilinx 7 Series Memory Port Product Brief

Features

- Support of 200 MHz to 700 MHz I/O clock speed
- Hardware Validated
- x18, x36 devices supported
- Burst of 2 words, Burst of 4 words modes supported
- Separate I/O, Common I/O devices supported
- 3.0 clock cycle read latency supported
- 1.5 V I/O supported
- 2:1 and 4:1 memory to FPGA logic interface clock ratio
- Automatic signal delay skew compensation on SA, D and Q signals
- Built-in self-test with pseudo-random test patterns
- Debug support of peeking and poking GSI's II+ memory locations, as well as 7 Series FPGA control parameters
- Memory Port IP delivered in Verilog source code with accompanying User Constraint File

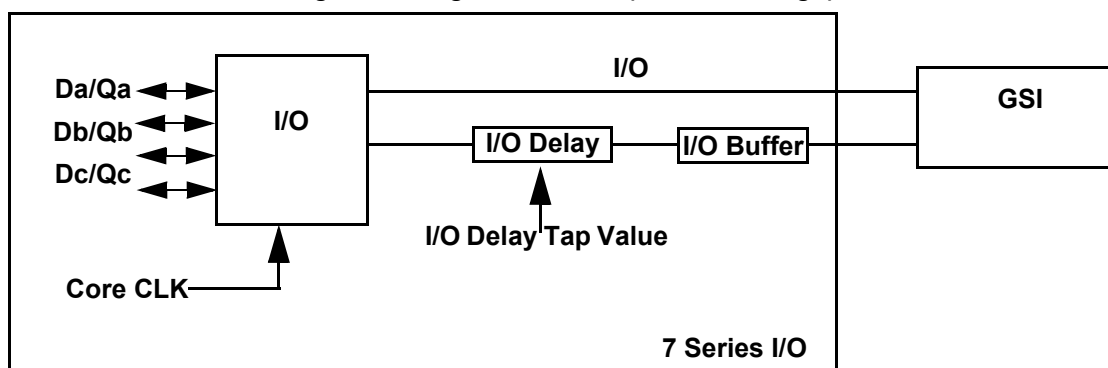
Introduction

The mission of this Xilinx 7 Series FPGA-based Memory Port is to maximize the valid windows among all related II+ SRAM I/O signals. It is intended for facilitating the PCB design involving the use of Xilinx 7 Series FPGA as the memory controller interfacing with any of GSI's II+ family of high speed memory parts (comprising the x18 and x36 versions of the Quad Burst of 2 (B2), Quad Burst of 4 (B4), and DDR Burst of 2 (B2) devices).

Functional Overview

Figure 1 shows a 2:1 Mux design I/O signal between the 7 Series FPGA and the GSI II+ SRAM. For the 4:1 Mux design, the number of Dx/Qx ports interfacing the I/O SerDes block would be 8. Each I/O delay block consists of an Input Delay block and an Output Delay Block. The Input and Output Delay block can be individually controlled with their own delay values.

Fig. 1: I/O Signal Interface (2:1 Mux Design)



I/O Interface Block

- Interfaces with the Memory Controller Block and translates data and control between the logic domain and physical signal domain
- Clock and data rate adaptation between the I/O signals and the Memory Controller logic because the FPGA core clock frequency is either 1/2 or 1/4 of the I/O clock
- Synchronizes Control and data signals between the FPGA clock domain and the I/O clock domain
- Performs I/O signal calibration under the control of the Memory Controller to adjust the I/O signal delay taps
- Identifies the valid window of the I/O signals and center the delay tap on the valid window

Memory Controller Block

- Accepts calibration commands from the user interface block and feeds back result and status
- Runs the calibration algorithm to control the I/O delay tap in the I/O Interface Block and verifies the calibration result
- Performs memory test using built-in pseudo random, incremental and fixed test patterns

User Interface Block

- Receives core logic clock and delay tap reference clock from the user design
- Accepts calibration commands from the user design and feeds back results and status
- Reports I/O delay tap values of calibrated signals to the user design
- Buffers memory read/write commands and data
- Accepts memory test commands from the user design and report results