Address Pin Labeling Mismatch

The purpose of this application note is to discuss differences between SRAM vendors' package pinouts. This paper will focus specifically on Address pins and will investigate whether the labeling mismatch between vendors will make one vendor's part incompatible with another.

Address Mismatch

Most SRAM vendors follow JEDEC SRAM pinout standards. JEDEC is an organization that, as one of its charters, defines package pinout standards for memory products, including SRAMs. JEDEC does not dictate that a certain pin is going to be at a certain address in situations where address differentiation makes no functional difference. For common I/O SRAMs, a certain group of pins are defined as addresses, another group is defined as I/Os, and so forth. This is why package layouts from different SRAM vendors have addresses, I/Os, power, ground and control pins in the same location on a given package. However, even though address pin locations are standardized, there is always the chance for address labeling mismatch. Address mismatch occurs when one SRAM vendor labels the address pins in a certain order and this is different from another vendor. Note there are two addresses on Synchronous SRAMs with burst functionality that are required to be on certain pins for all SRAM vendors—A0 and A1.

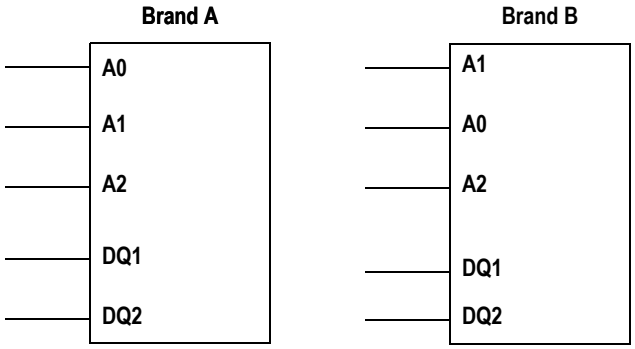

Figure 1: Two Generic SRAMs

Comparison of Two Generic SRAMs

Consider an example of two generic SRAMs with three address inputs and two data I/Os, shown in **Figure 1**. The design was built with Brand A's SRAM so that there is no address mismatch between the SRAM and the microprocessor, as shown in **Figure 2**. For this design, Brand A is the primary source, but a second source is required. Because a second source is need, Brand B's SRAM is being considered. The issue is whether the address labeling difference, as shown in **Figure 2**, will cause Brand B's SRAM to be incompatible with the design. To help answer this question, a simple write/read non-bursting example will be used. This example applies to both Asynchronous and Synchronous SRAMs. If the microprocessor writes to Address A0, A1, A2 = 101, Brand A's SRAM will write to an internal address of 101, but Brand B will write to an internal address of 011. Then when the microprocessor performs a read operation at the same address A0, A1, A2 = 101, Brand A will read from 101 and Brand B will read from 011. As can be seen in this simple example for any address written by the microprocessor, there is only one corresponding internal SRAM address. Thus, the microprocessor will always receive the expected data for a given address regardless of address labeling.

There is a special case where A0 and A1 must be in the same location on both SRAMs. This case occurs when the application is using the internal Burst Counters. The microprocessor will load the

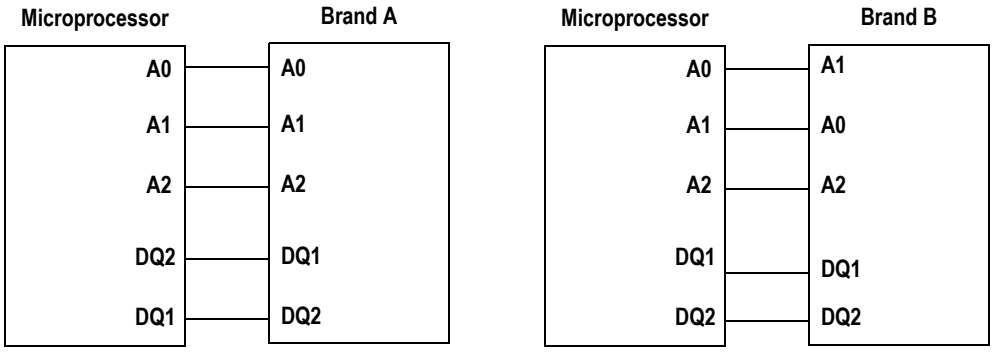

Figure 1: SRAMs Connected to a Generic Microprocessor

SRAM with the read or write start address and then the SRAM will use the internal 2-bit burst counter to generate the next three addresses. The microprocessor will need to supply data to the SRAM for the next 3 internally generated addresses. The reason that A0 and A1 locations matter for this case is that the microprocessor may have the option to a start address for a Burst Read that differs from the start address for the Burst Write. During the read, the microprocessor expects a certain sequence of data based on the addresses it assumes were generated by the internal burst counters of the SRAM. If A0 and A1 are scrambled, then the expected data may not be returned. For example, if the microprocessor starts a linear burst write supplying data of 1, 2, 3, and 4 and a start address of A0=0 and A1=1, then Brand A will start at 01 and generate internal address in the order or 10,11 and 00. However, Brand B will have a start address of 10 and generate internal addresses of 11, 00 and 01. When the microprocessor performs a burst read starting at 11, the expected data will be 2, 3, 4, and then 1. Brand A will start a 11 and produce data of 2, 3, 4, and then 1. Brand B will also start at 11 but will produce data of 3, 4, 1, and finally 2. This example shows that some bursting applications that allow the microprocessor to have read start addresses that differ from that of write is sensitive to A0 and A1 address scrambling. But even for this example, all of the other addresses do not need to match.

Conclusion

When comparing datasheets either to second source a current design or to replace an end of life product, as is often the case, the address labeling might not match from one vendor to another. This is does not mean that the SRAMs are incompatible. On the contrary, they are compatible and address labeling mismatches should not be taken into account when cross referencing SRAMs. With the only exception of synchronous burst applications where data bursting is required, then A0 and A1 must match between devices but all others do not need to match.