DVRFD630 Development Board
DVRFD631 Development Board

General Description

The DVRFD630 and DVRFD631 development boards are a general purpose circuit board designed to simplify the evaluation of the IXRFD630 and IXRFD631 gate drivers and provide a building block for power circuit development. The IXRFD630 or IXRFD631 gate driver is factory installed on the evaluation board and is fully tested. Two board configurations are available for each driver: The EVRFD63x 150/275 configuration enables the user to drive DE150 or DE275 sized MOSFETs, while the second EVRFD63x 375/475 configuration has a larger footprint pad for DE375 or DE475 sized devices. The board design allows both the driver and MOSFET to be attached to a heat sink, and in doing so allows the board assembly to be used as a ground referenced, low-side power switch.

IXRFD630 vs. IXRFD631

The IXRFD631is an improved version of the IXRFD630 with the addition of a Kelvin ground connection and additional bypass caps added on the substrate. Heavy drive currents exit the ground pins, and when pcb layout is less than ideal, inductance in the ground plane can cause ground bounce causing the input signal threshold to shift inducing missed triggers. The Kelvin ground pin avoids this by moving the inputs ground to its own pin. Additional bypass capacitors improve the decoupling at the die.

The DVRFD631 boards include zero ohm resistors or jumpers in positions R3 and R4 allowing a common mode choke to be used for particularly noisy environments. To insert choke simply remove R3 and R4 and use existing pads to attached wires of choke. A small low-medium permeability material 43 ferrite core with three turns that results in approximately 2-3 nH works best. Be careful with too much inductance that impacts performance.

The IXRFD630 works fine for the majority of users. The IXRFD631 is an improved version preventing missed input triggers due to ground bounce. While the addition of a common mode choke can be added for even more difficult applications.

Figure 1 is a picture of the DVRFD630 150/275 circuit board. The low-level input SMB connector is shown to the left with a test point connection, along with the ground test point and finally the Vcc test point. The Vcc test point provides power to the IXRFD630. It is suggested to run Vcc at a value of 12 V.

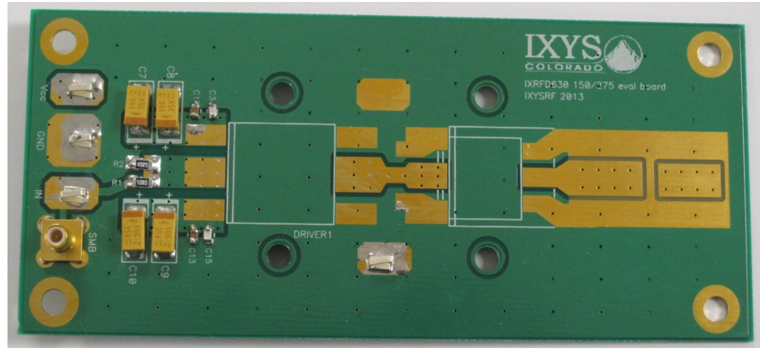

Figure 1– DVRFD630 150/275 Top Side

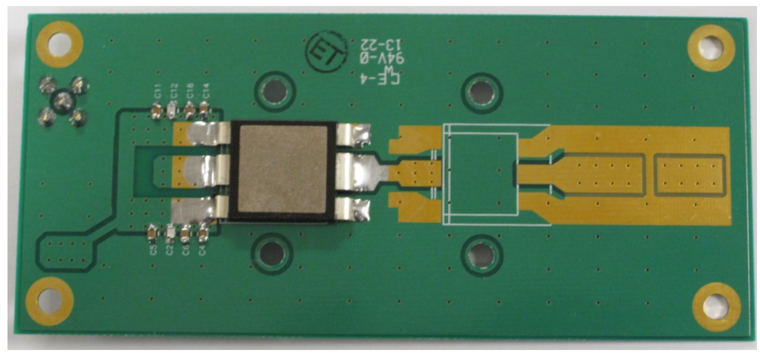

Figure 2– DVRFD630 150/275 Bottom Side

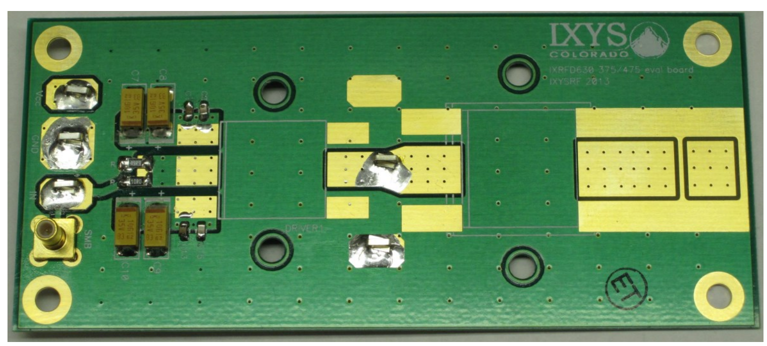

Figure 3– DVRFD630 375/475 Top Side

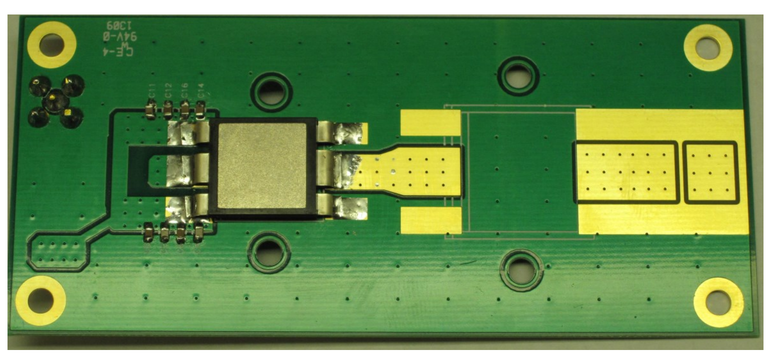

Figure 4– DVRFD630 375/475 Bottom

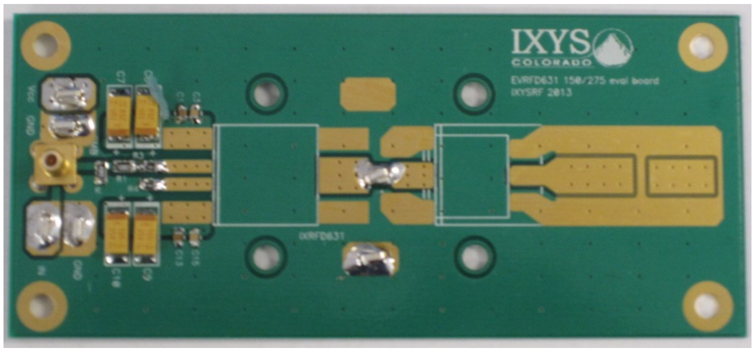

Figure 5– DVRFD631 150/275 Top Side

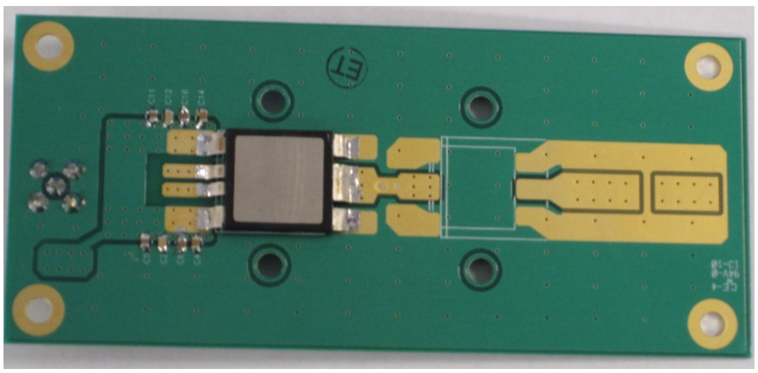

Figure 6– DVRFD631 150/275 Bottom Side

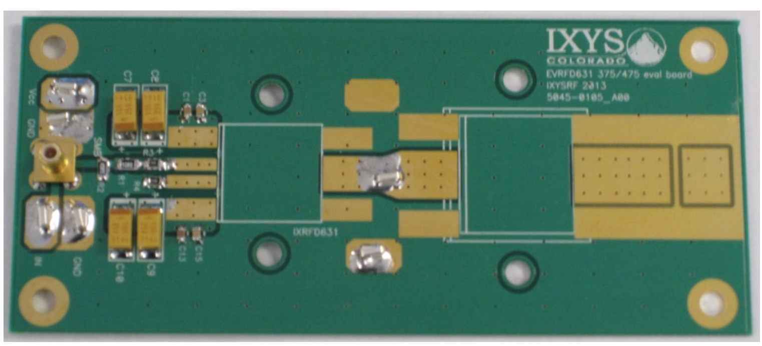

Figure 7– DVRFD631 375/475 Top Side

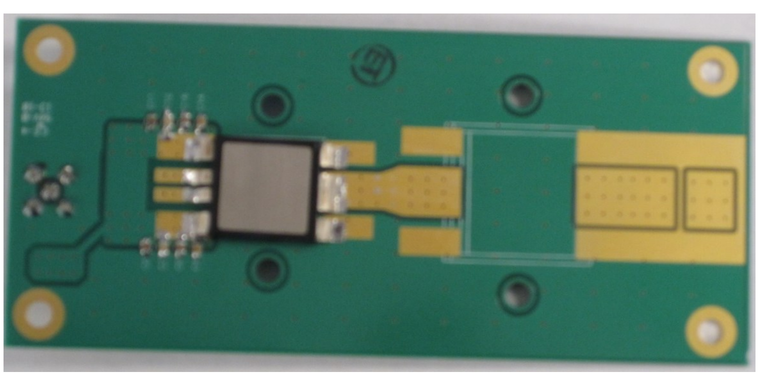

Figure 8– DVRFD631 375/475 Bottom Side

Figure 2 is a picture of the bottom side of the DVRFD630 150/275 board. In the high-power configuration the exposed metalized bottom of the driver is shown. It can be placed in compression against a heat sink or cold plate facilitating the very high power dissipation capabilities of the package.

Figures 3 and 4 show the larger footprint for the DE375 and DE475 devices on the DVRFD630 375/475 board.

Figures 5 through 8 are the equivalent board just described but utilizes the IXRFD631 gate driver in place of the IXRFD630. R3 and R4 of zero ohm or jumper resistors and can be removed to insert a common mode choke if desired.

Mounting Orientation

The evaluation boards top and bottom layers are mirror-imaged so that the driver and MOSFET can be placed on either side of the board. This has been done to increase flexibility of use. Note that the IXRFD630 can be mounted with either top or bottom side down. A low power configuration results when the metallized substrate tab on the back of the driver is mounted directly down on the circuit board because a heat sink can't be attached in this configuration. As supplied from the factory the IXRFD630 is mounted in the high power configuration with the metallized substrate tab exposed, as shown in Figures 2, 4, 6, and 8. Mounting holes on either side of the driver and MOSFET allow the board to be screwed down on to a heat sink, clamping the devices to the heat sink and utilizing the high power dissipation capabilities. Thermal compound on the exposed substrate is recommended to provide a better thermal interface between the device and heat sink.

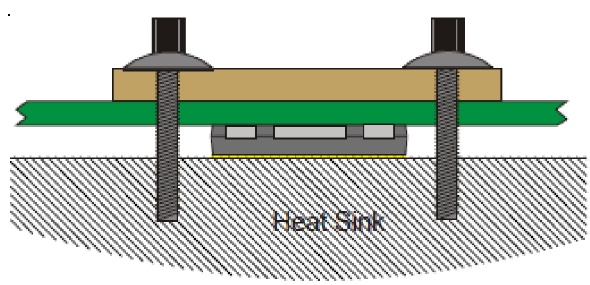

Figure 9– View of IXRFD630 mounted in high-power Configuration. For additional device installation instructions see technical note "*DE–Series MOSFET Mounting & Installation Instructions*" available on the IXYSRF web site www.ixyscolorado.com

Figure 9 depicts the high power configuration in a end view with the device sandwiched between the printed circuit board and heat sink. When using the circuit board to apply compressive force to the device, care must be taken not to over-tighten mounting screws that causes the board to flex.

Circuit Description:

The schematic diagram for the evaluation boards are shown in Figure 10 and 11 below. The circuit includes the IXRFD630 or IXRFD631 gate driver, input protection and impedance matching resistors, and bulk and bypass capacitance. While the MOSFET is depicted in the schematic, it is not included with the board due to the variety of MOSFETs IXYSRF offers.

The test points and connectors to operate the board are described in Table 1.

Input	Function
SMB	Input Signal Connector
IN	Input Signal Test Point
GND	Circuit Ground Test Point
Vcc	Power Supply Test Point (8 V-15 V)

Table 1– Test points and connector descriptions

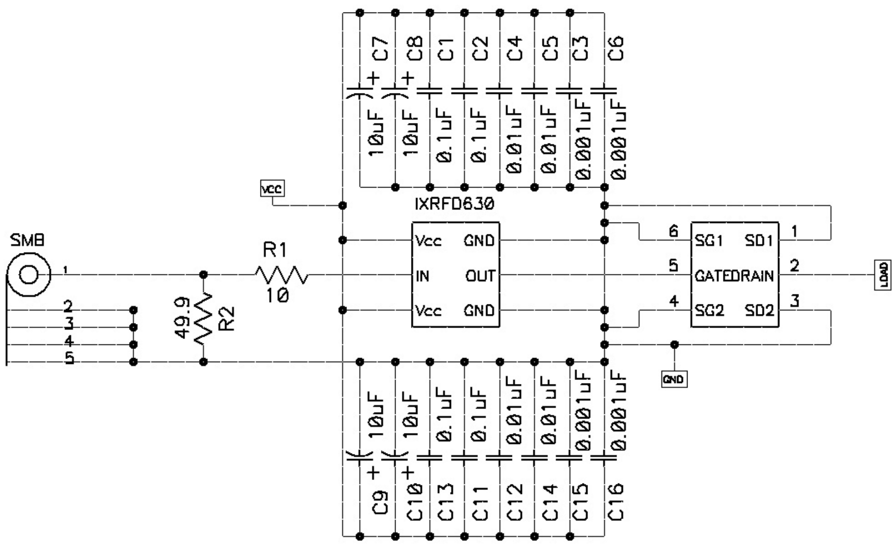

Figure 10– Schematic diagram for DVRFD630 evaluation board, MOSFET not included

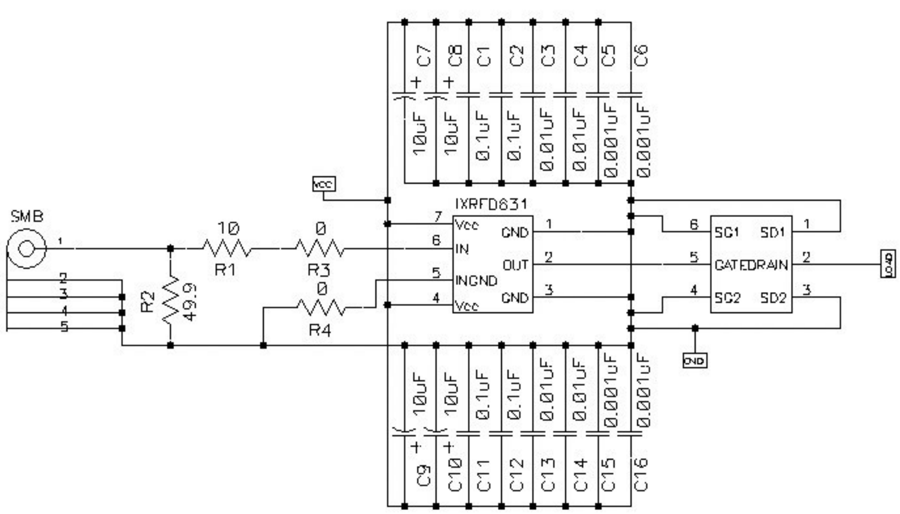

Figure 11– Schematic diagram for DVRFD631 evaluation board, MOSFET not included

The SMB connector is used to supply an input signal. The IN test point can also be used if no cables are available with an SMB style connector. Test points are straight forward, Vcc supply voltage, IN input signal, GND ground for entire board. It is suggested to operate the board at 12 V for general testing.

R1 limits input signal current but is not mandatory for all driver applications; it is more for general protection of the driver. R2 loads the typical 50 Ω output impedance of most bench top signal generators. The input of the gate driver can operate without R1 and R2, where R2 can be removed, if desired, in the case that the input signal generator can't support the loading. In most cases the output level of the signal generator will have to be increased in order to compensate for the input load.

Bulk storage capacitors C7, C8, C9, C10 provide energy storage local to the driver. During switching of the output stage of the driver, parasitic inductance of any wire and trace between the power supply and driver can inhibit fast delivery of energy to the driver. This will result in a voltage drop along the inductance and will cause the voltage at the Vcc pins to sag. To counter this, large valued bulk storage capacitors are placed as close to the Vcc pins of the driver to supply energy right at the driver pins. Tantalum capacitors are used and suggested for use as they can release their stored energy very quickly into the Vcc pins. Aluminum electrolytic capacitors are not used or recommended for bulk storage capacitors due to their high values of ESR, or Equivalent Series Resistance, that slows energy delivery.

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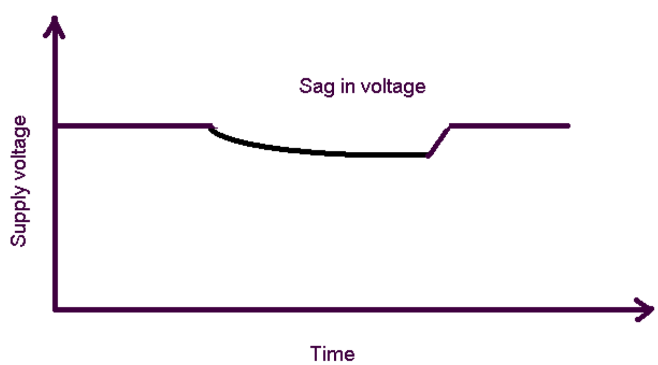

Figure 12– Sag in supply voltage at Vcc pins due to high series resistance from bulk storage capacitors

The network of bypass capacitors are made up of C1-C6, C11-C16 and includes a wide spread of values, 0.001 µF, 0.01 µF, and 0.1 µF. The purpose of the capacitance spread is to produce over-lapping response curves that lower the insertion impedance over a wider band. The bypass capacitors can be viewed as low pass filters, but the generally ignored series inductance causes a notch or V-shaped response in the impedance curve as frequency goes up. Figures 12-16 represent the progression of a single ideal capacitor response to the parallel combination of multiple capacitor networks.

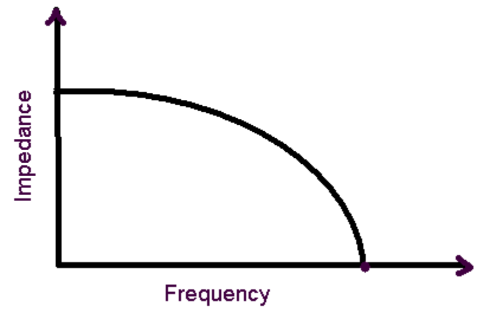

Figure 13– Ideal capacitor frequency response

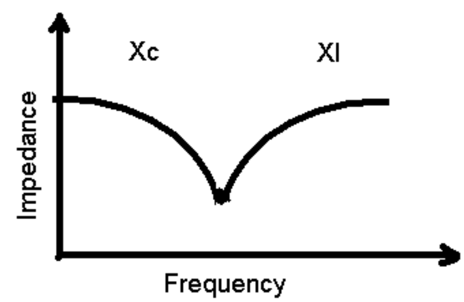

Figure 14– Capacitor frequency response due to self inductance

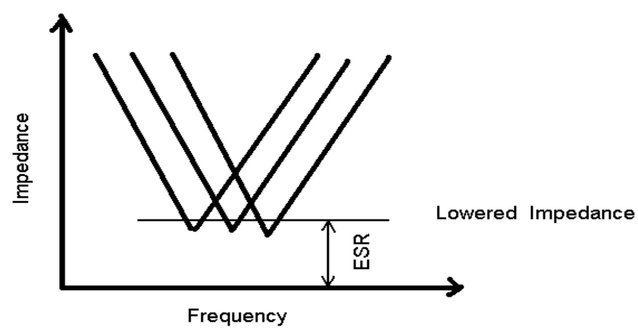

Figure 15– Over-lapping impedance curves

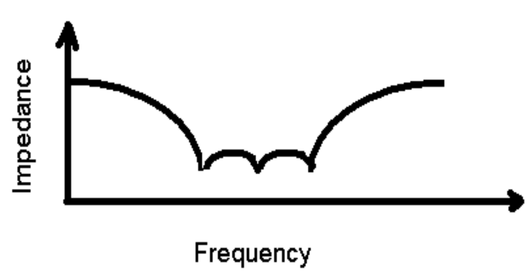

Figure 16– Broadband impedance lowered

The values of bypass capacitors are closely related to circuit performance and operation. Parasitic inductance is a characteristic of any circuit board and high drive currents cause high frequency ringing to occur at the corners of the rising or falling edge of the output signal as a result of this inductance. The value of this high frequency ringing is usually in the tens of megahertz and so the spread of capacitance values is in the tens of microfarads region. Each bypass capacitor is considered its own network with associated frequency response; replacing the individual capacitors with an equivalent capacitor of the total combined value does not have the same effect.

Circuit Operation

The input to the IXRFD630 has a positive going threshold of approximately 3.25 V with a hysterisis of 0.2 V. The typical input signal level range is 5 V up to Vcc.

Apply a signal to the SMB connector with minimum suggested amplitude of 5 V. If a SMB type connector and cable are not available, it is possible to take a small coax, unwind the outer conductor braid, twist it together, and solder the center conductor to the input pad IN and outer conductor to ground or GND.

Apply a supply voltage to the circuit, positive to the Vcc test point and ground to the GND test point. The suggested operating point is Vcc = 12 V.

Operation can now be observed by placing a scope probe on the output of the driver. Figures 17 through 19 show typical operation with no load attached to output of driver.

See the IXRFD630 or IXRFD631 datasheet for additional performance data at www.ixyscolorado.com

Ordering Information	
Part Number	**Device Layout**
DVRFD630 150/275 DVRFD631 150/275	Accommodates DE150 or DE275 series MOSFETs
DVRFD630 375/475 DVRFD631 375/475	Accommodates DE375 or DE475 series MOSFETs

Table 2– Ordering Information

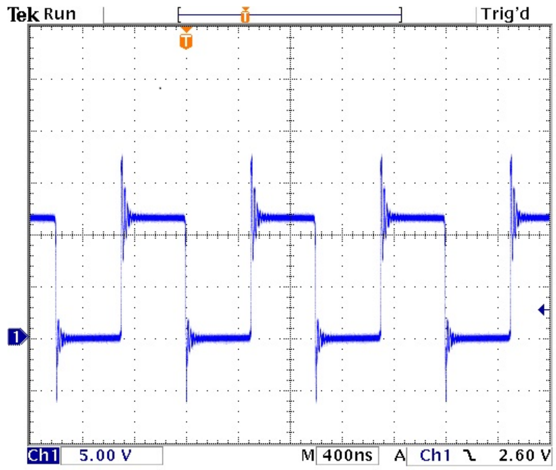

Figure 17– 1MHz output signal

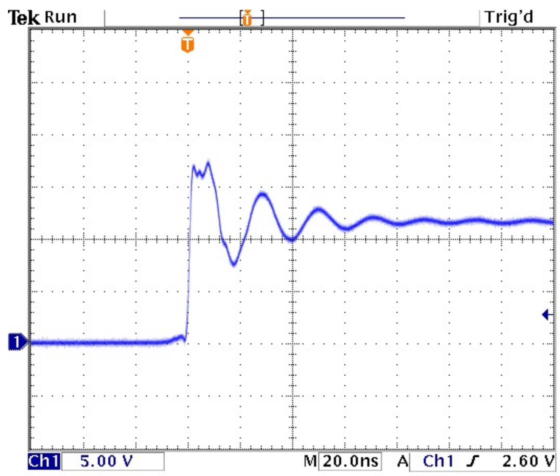

Figure 18– Rising edge of output signal

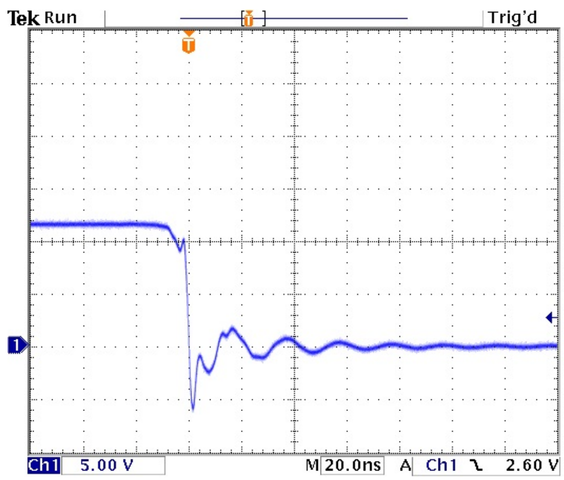

Figure 19– Falling edge of output signal

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