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Design of a Dual-Band Wireless LAN SiGe-Bipolar Power Amplifier

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Cost, performance and operating features were the design objectives for this dual-band WLAN power amplifier, implemented using technology that combines silicon and SiGe with improved grounding

This article describes an integrated dual-band multi-mode wireless LAN radio frequency power amplifier (Infineon PMB 8825) for 2.45 GHz and 5.25 GHz. The device has been realized in a 42 GHz-f_T, 0.35-µm SiGe-Bipolar high volume technology. The chip features two single-ended 3-stage power amplifiers for each frequency band and a control section that includes band select, standby and power control functions. The 2.45 GHz section achieves an output P_{1dB} of 28 dBm with a PAE of 40% and a saturated output power of 29 dBm. The 5.25 GHz section achieves an output P_{1dB} of 23.8 dBm, and a saturated output power of 25.9 dBm at 3.3 V supply voltage. Its PAE at the P_{1dB} is 24%. The small signal gain is 31 dB at 2.45 GHz and 26 dB at 5.25 GHz.

Introduction

Wireless LAN is one of the growing high-volume production markets. As customers desire more data throughput at low price, chipsets for IEEE 802.11a and IEEE 802.11b/g have become available. The first dual-band transceiver designs have been reported in [1, 2]. Currently, power amplifiers (PAs) are dominated by III/V compound semiconductors, which have very good RF characteristics, but cost disadvantages. Today, there exists only a small number of Si- or SiGe-based PAs [3, 4, 5, 6] with most of them focused on cellular phone applications. There does not exist any dual-band RF power amplifier solution for 2.45 GHz and 5.25 GHz as required for multi-mode WLAN.

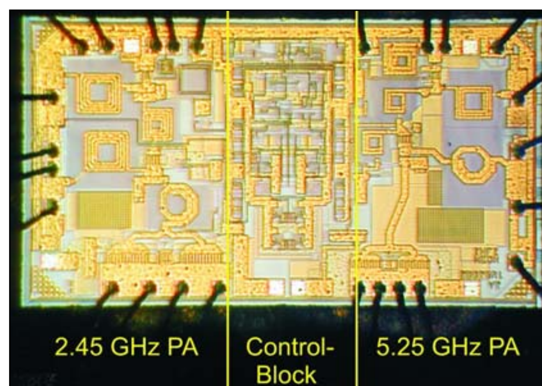

Figure 1 · Die micrograph of the dual-band power amplifier die.

This work presents a dual-band PA design for both the 5.25 GHz and 2.45 GHz bands, using two RF sections on one die. With these two frequency bands, the IEEE 802.11a standard for 5.25 GHz and IEEE 802.11b/g for 2.45 GHz were the main focus of the PA designs. The amplifier circuits are based on three stages, using on-chip inductors for inter-stage matching, plus a stripline for matching to the output stage in the 5.25 GHz part. In addition, a control circuit is included on the die to facilitate band selection, provide the bias control required for the power control, and implement the stand-by mode. The SiGe bipolar technology used for the device features a low-ohmic low-inductance on-chip ground-connection to enable fabrication of a single-ended PA at high frequencies without the need of any ground-bonds. This avoids the need for parallel bond-wires [7, 8] and the accompanying cost and variation problems, but requires some care in packaging issues. In

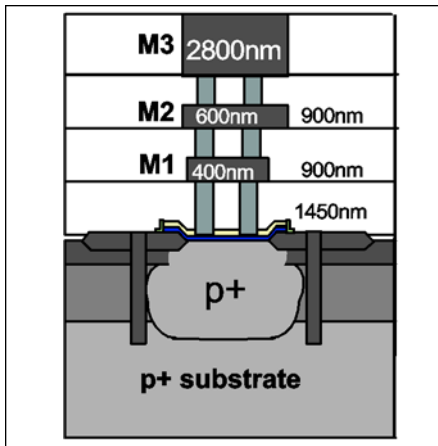

Figure 2 · The metal layer stack of the SiGe-Bipolar technology including the ground connection structure.

addition, die size is reduced, as no ground pads are required, which allows the use of smaller packages. Figure 1 shows the complete PA die micrograph. The PA was manufactured using a VQFN-24 package for the test setup.

SiGe-Bipolar Technology

The technology used in this work is a 0.35 µm SiGe-Bipolar process, based on a high-volume process presented in [9, 10] (Infineon B7HF). The heterojunction bipolar transistor (HBT) was modified for 3.3 V supply voltages and thus higher ruggedness by lower collector doping, and has an f_T of 42 GHz and f_{max} of 60 GHz. The resulting worst-case collector-base breakdown voltage of the HBT is BV_{CB0} = 15.5 V and the worst-case collector-emitter breakdown voltage is BV_{CE0} = 4.0 V. The technology features a three layer Al-metalization with a 2.8 µm thick upper layer used for inductor structures (Figure 2). Further devices are a vertical pnp transistor, poly-Si resistors, MIM capacitors, MIS capacitors, inductors and an on-chip low inductance ground contact comparable with [11]. Figure 2 shows the metal layer stack of the technology including ground connection structure.

In order to realize the mentioned low-inductance, low-ohmic connection the substrate resistance is enormously decreased—using highly doped substrate material—down to 15 mΩcm. Using high implanted epi layers, a low inductance connection between the lowest layer of metal and substrate is achieved. The structure created in this way has a series resistance of only 50 mohm for a chip area of 100×100 mm^2 and a negligible series inductance. The ground contact is used to overcome emitter degradation and enables defined ground contacts for matching circuits on-chip. This is furthermore advantageous to bonding deviations in volume-production. However the die has to be fixed into the VQFN package using a highly conductive glue, being a further issue in material and reliability considering the combination with typically high heat dissipation in PA applications.

Circuit Design

Figure 3 shows the simplified circuit diagram of the PA. It consists of three major parts:

- A three-stage 2.45 GHz PA for IEEE 802.11b/g
- A three-stage 5.25 GHz PA for IEEE 802.11a
- A control block

Both PA circuits have a single-ended topology and rely on the extensive usage of the ground contact feature of the used SiGe-bipolar technology.

2.45 GHz PA

Considering the 2.45 GHz path, the first stage used an external capacitor in addition to the internal found inductance for the input matching using the bondwire as a part of the input match. The shunt inductance in combination with the ground contact can further be used to check ground connection problems in the package, as all resistances are known. The first HBT T1 has an effective emitter area of 126 µm^2 and operates in class-A mode. To prevent a low frequency oscillation problem found by simulations, a biasing inductance was used and designed to shunt parasitic oscillations. On the emitter a resistor is used for controlled emitter degradation, as the overall small signal gain should not exceed 32 dB. Shunting the resistor will lead to small signal gain values reaching up to 38 dB. A benefit of this circuit is the reduced deviation of the input impedance vs. the input power. The second stage consists of the HBT T2 with an effective emitter area of 336 µm^2. It is T-network matched to T1 using a using a series inductance on the base of T2 and a shunt capacitor directly attached to a large ground contact. This type of matching was selected, as it represents a low-pass filter and the MIM-caps can be placed directly above the ground contacts with a lot of vias, improving the capacitors *Q*-factors by the reduction of the series resistance. Hence, no additional parasitics on the capacitor ground are found, making the matching design more accurate. However, the capacitor model differs from the series capacitor, as now the substrate part is shunted and the connection resistance is lowered. Greater design effort was required for matching between the second and third stage. To achieve the desired output power, the third stage HBT T3 has a large emitter area of 2184 µm^2 an thus an extremely low base impedance. With this, the matching between T2 and T3 reaches it limits with the quality factor of the matching inductances and the inductor requires a model as exact as possible. This can only be achieved, if the used high-conductive substrate is considered, as the parasitic conductor to substrate capacitances are increased. Simulations show *Q* factors in the range of 5-7 for the required current of the inductors. The designed octagonal inductor was

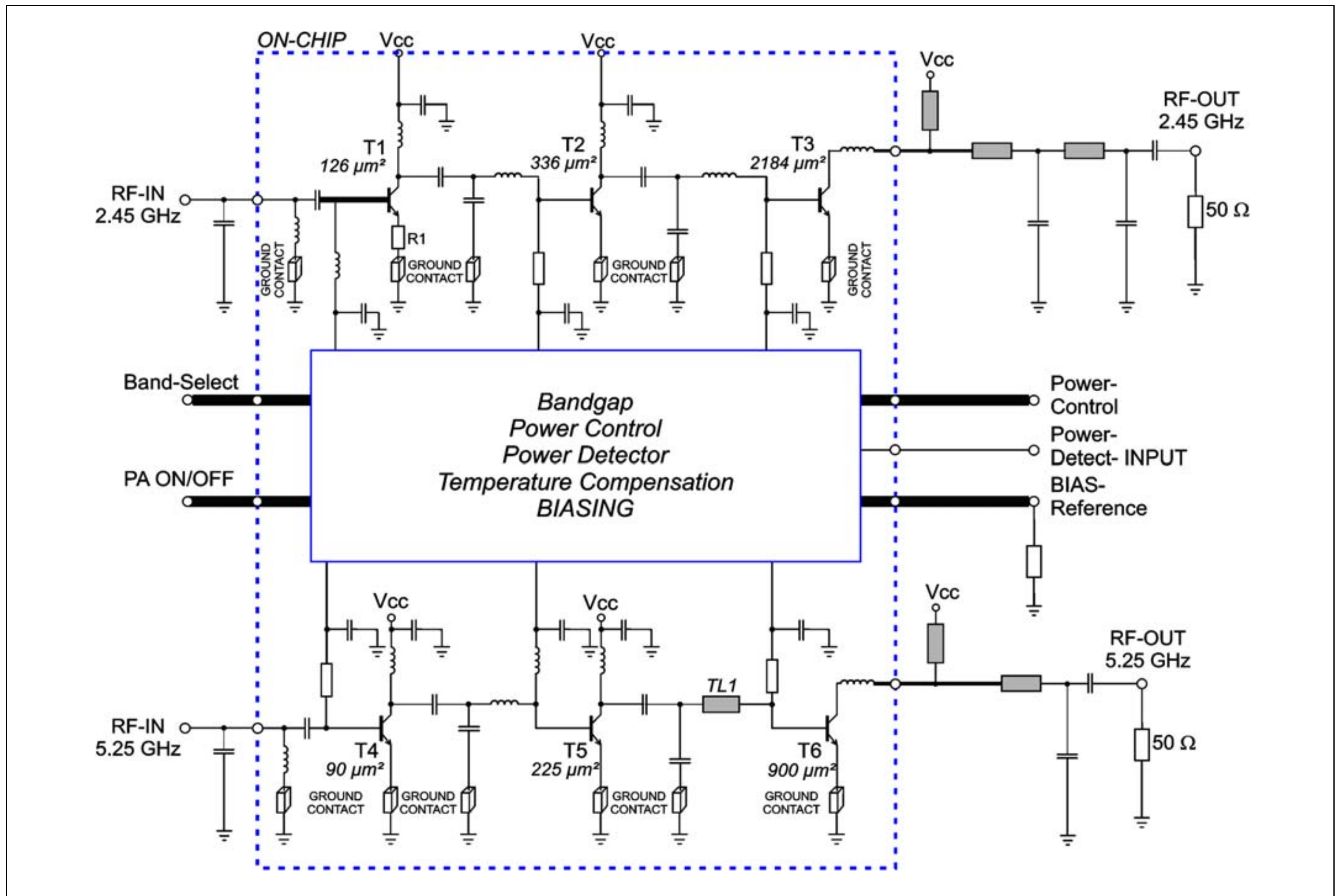

Figure 3 · Simplified Circuit diagram of the integrated power amplifier.

designed and simulated together with the base connection metalization of T3. This procedure ensures, that the modeled inductance and *Q*-factor fits into the sensitive part design. Furthermore, the biasing of T2 and the output HBT T3 is realized using resistors instead of inductances for feeding the bias current, as no mismatch due to the inductor parasitics occurs and—more important for cost issues—the chip area is kept smaller. The output match has do be realized as optimally as possible to achieve the maximum efficiency. Four bondwires were used to keep the output connection inductance to the VQFN-24 package low. The output matching was realized externally using two stages. However, load-pull tuning using a manual harmonic load-pull tuner was done to obtain the optimum matching to achieve a high Power Added Efficiency (PAE) as well as linearity considerations. The required output matching network was synthesized out of the load-pull data and realized using microstrip transmission lines and high-*Q* Epcos capacitors. The output match consists of the connection inductance, two transmission lines and two shunt capacitors. A 1/4-wave line is used directly at package output for the supply voltage feeding and the second order harmonic block. Efficiency issues for the optimum matching are discussed in [12, 13].

5.25 GHz PA

The 5.25 GHz section uses input matching similar to the 2.45 GHz PA. The first stage is matched to the input using a shunt inductance and the input DC-block capacitor. However, unlike the 2.45 GHz section, the bias current is supplied using a resistor connected to the current-source and no resistor is used at the emitter contact, as no oscillation problem was found during the simulations for the first stage. Another reason for not using a resistor at the emitter contact is that as much gain as possible was desired. The effective emitter area of the first stage transistor is 90 µm^2. This first stage is matched to the second amplifier stage using a T-network consisting of two capacitors and a series inductor. To improve the quality factor of the inductances, octagonal shaped inductors have been used.

The second stage effective emitter area is 225 µm^2. While the other stages are biased using a resistor, the

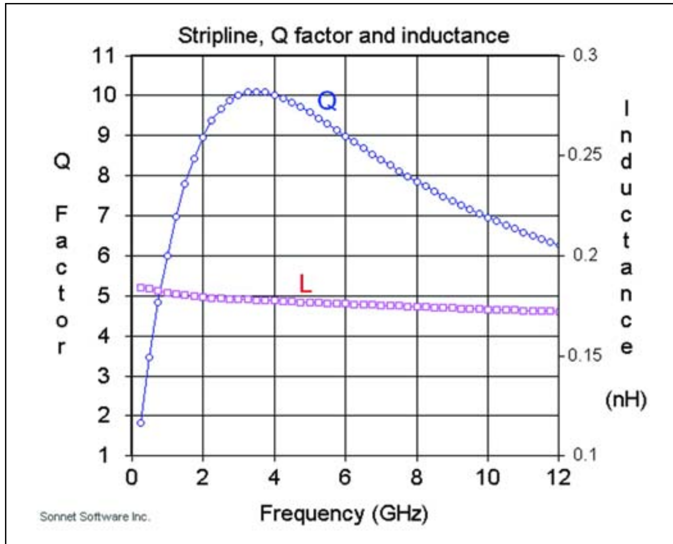

Figure 4 · Simulation results for inductance and quality factor of the microstrip transmission line structure.

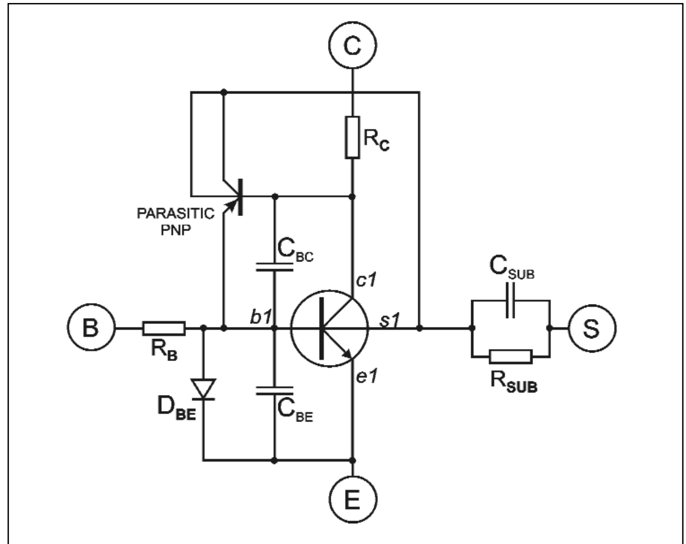

Figure 5 · Transistor equivalent circuit for the PA RF simulations.

bias connection for the second stage was realized using a small inductor to prevent parasitic oscillations, just as in the first stage of the 2.45 GHz section. The output stage transistor effective emitter area is 900 µm^2. Again, the large transistor has a very low input impedance, and a matching network with a highest possible quality factor is necessary.

As the designed octagonal-shaped inductor still did not achieve sufficient quality factor, and the required inductance is very low (about 200 pH), the inductance between output transistor and second stage was replaced by a structure similar to a microstrip transmission line. This is achieved using the additional capacitance-to-ground connection as part of the matching network. The transmission line is realized using the thick upper layer in Figure 2 for the signal line and the lowest Al layer connected to the ground contact. This ensures a very good ground connection at the lower ground metalization and thus guarantees impedances, since the parasitic capacitance and resistance due to the substrate material is shorted—no epi-layers are found below. Hence, lower loss in the matching network is obtained. The capacitance of the transmission line to ground is used in addition to the shunt capacitance and lowers the required shunt capacitance. Figure 4 shows the simulation results for the microstrip transmission line structure.

The inductors and the stripline are modeled with using Sonnet electromagnetic (EM) simulation software [14]. Pre-assumptions of the inductances are made using inductance equations found in [15, 8] using the in-house tool, Coilgen, presented in [16]. Additionally, based on EM-simulations for the RF currents, the inductors were rounded up at the edges to improve the inductor behavior. Capacitances were realized as metal/insulator/metal capacitors (MIM-CAPs), while blocking capacitors were realized as MIS-Caps to achieve higher capacitance values. Modeling issues for MIM-caps can be found in [17].

Control Block

Both RF PA sections are biased by a control block. The biasing itself was realized using current mirrors, with the current mirror transistor being placed directly next to the output transistor to achieve similar temperature levels. Using several current mirror circuits with different current mirror factors, the biasing is fixed by only one external resistor using a bandgap circuit as voltage reference. In addition, the control block features an integrated power detector (using a diode), a power-control and a power-down function by reducing the bias currents. A band-select function allows fast switching between both PA sections to change between IEEE 802.11a and 802.11b/g.

The complete design was simulated using Cadence Spectre with a modified SPICE Gummel Poon (SGP)-model [18, 19]. The transistor equivalent circuit is shown in Figure 5. It uses a parasitic pnp transistor to improve the input match simulation. The symbol 'S' represents the substrate contact.

Experimental Results

Figure 6 shows the power amplifier test-board used for the measurement setup. The substrate material is FR4, as used for volume production by the customers. External matching networks have been built and optimized to get the desired performance with use of transmission lines and high-*Q* Epcos capacitors. The 1/4-

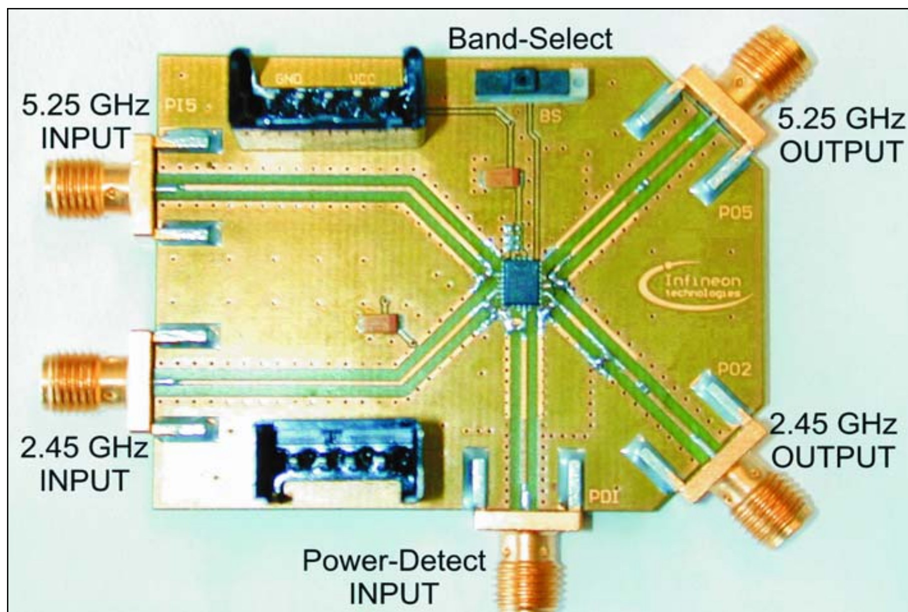

Figure 6 · Photograph of the power amplifier test board.

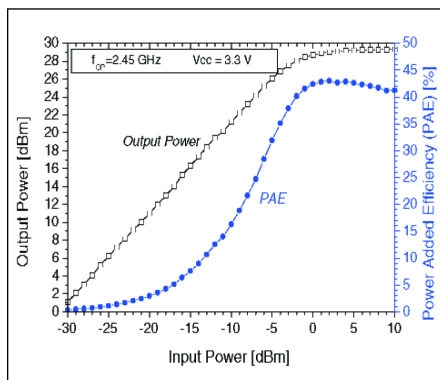

Figure 7 · Measured power transfer characteristic for the 2.45 GHz section.

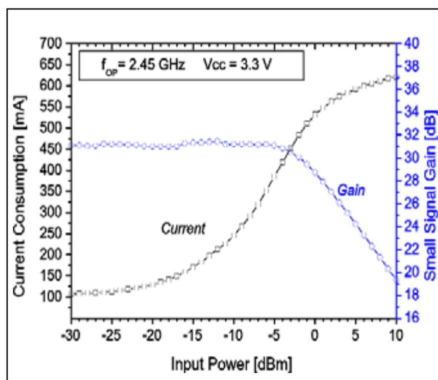

Figure 8 · Measured current consumption and small signal gain vs. input power.

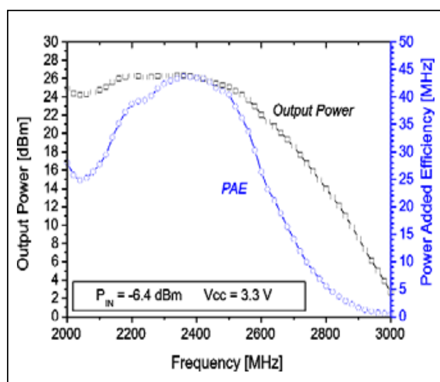

Figure 9 · Measured 2.45 GHz PA section frequency response for P_{IN} = –6 dBm.

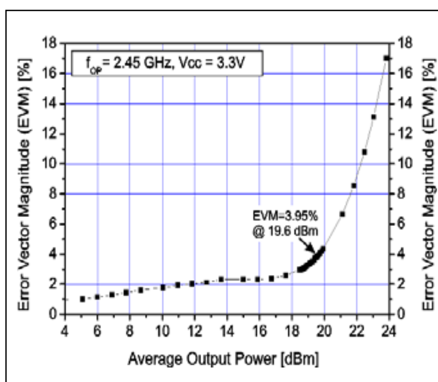

Figure 10 · Measured Error Vector Magnitude (EVM) vs. average output power for the 2.45 GHz section.

wave transformers are found on the backside of the PCB.

The chip shown in Figure 1 is packaged into a VQFN-24 housing and reflow soldered onto the test-board.

2.45 GHz PA Experimental Results

Figure 7 shows the measured power transfer characteristic for a supply voltage of 3.3 V, the typical supply voltage for PCMCIA cards. The power control voltage was set for maximum output power. The measurement curve shows a small signal gain of 31 dB. The input 1 dB compression point IP_{1dB} is –2 dBm and corresponds to an output power level OP_{1dB} of 28 dBm. The Power Added Efficiency (PAE) for the 1 dB compression is 40% and goes up to 42.8% for the saturated output power of 29 dBm. The small difference between saturation and compression is a result of having the design tuned for maximum linearity. The PAE power transfer curve shows a rise quite early for low output power levels, being advantageous for low power operation.

Figure 8 shows the corresponding current consumption and small signal gain vs. input power. A quiescent current of only 107 mA is achieved.

Considering the frequency tuning of the internal and external matching circuit, a frequency sweep is done in Figure 9. Operated at 3.3 V and for an input power of –6.4 dBm (for linear operation), it shows a definite tuned behavior with a deviation of 50 MHz for the maximum, but the resulting output power and efficiency are still in the specified range.

As linearity is a big issue for WLAN, an Error Vector Magnitude (EVM) measurement was performed. For this setup an Agilent vector signal analyzer was used. Figure 10 shows the EVM vs. average output power of a 64-QAM signal (54 Mbit/s). For a maximum EVM of 4% the respective average output power is about 19.6 dBm. The corresponding spectral

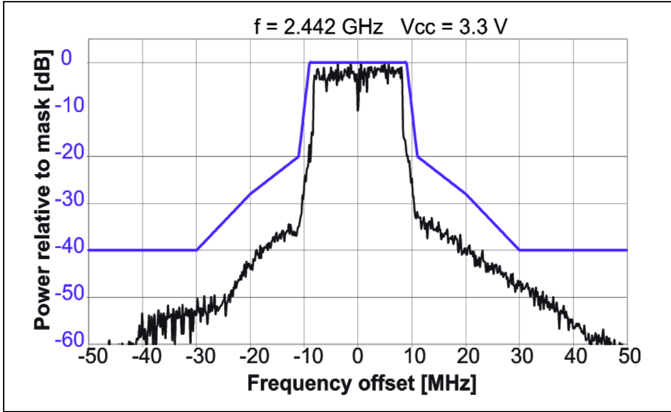

Figure 11 · Output spectral mask for a 54 Mbit/s 64-QAM for the average output power of 19.6 dBm.

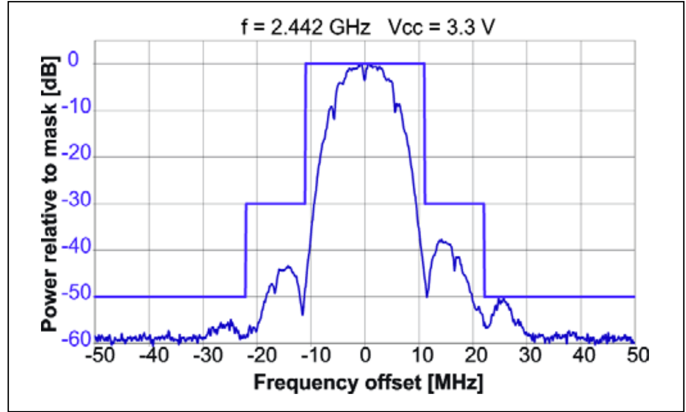

Figure 12 · Output spectral mask for the CCK-mode in IEEE 802.11b with an average output power of 18.6 dBm.

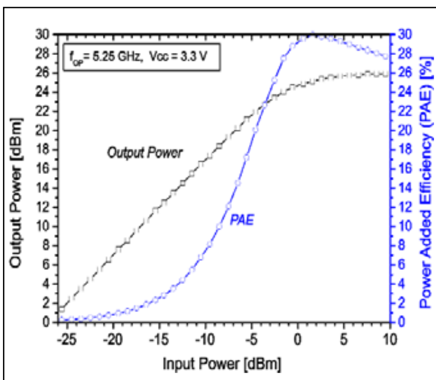

Figure 13 · Measured power transfer characteristic for the 5.25 GHz section.

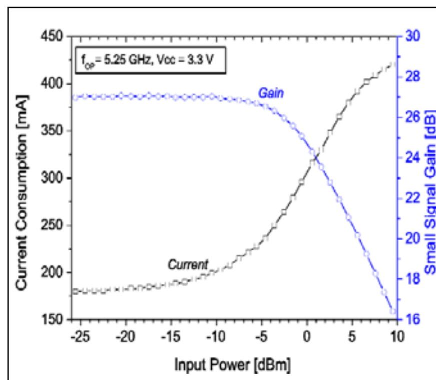

Figure 14 · Measured current consumption and small signal gain vs. input power for the 5.25 GHz PA.

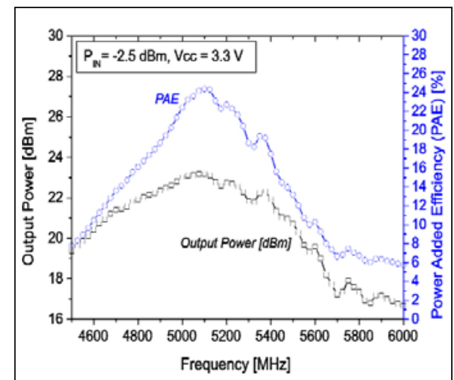

Figure 15 · Measured power amplifier frequency response for P_{IN} = –2.5 dBm.

mask is found in Figure 11. It shows high margins to the standard specifications. The most common mode is Complementary Code Keying (CCK) for IEEE 802.11b. The measured spectral mask for an average output power of 18.6 dBm is found in Figure 12. It is only limited by an upper sidelobe in the spectral mask.

5.25 GHz PA Experimental Results

Figure 13 shows the measured power transfer characteristic for the 5.25 GHz section. The maximum output power is 25.9 dBm at 3.3 V supply voltage and 5.25 GHz. The maximum PAE is 30%. The OP_{1dB} is 23.8 dBm with a PAE of 24%.

Figure 14 shows the corresponding current consumption vs. input power additionally to the small signal gain curve. The quiescent current is 180 mA and the small signal gain 27 dB.

Figure 15 shows the frequency response for linear operation using an input power of –2.5 dBm. It shows a small deviation from the center frequency.

For the IEEE 802.11a standard the linearity was measured using an 64-QAM 54 MBit/s input signal. The EVM vs. average output power is shown in Figure 17. For a maximum EVM of 3%, the maximum average output power is about 17 dBm. The corresponding spectral mask is shown in Figure 16 for several average output power levels. High margins are found, so that the specifications is met for up to 22 dBm. Hence, for lower data rates, much higher output power can be adjusted. The PA key performance is found summarized in Table 1.

Frequency	2.45 GHz	5.25 GHz
Small-signal gain	31 dB	26 dB
Supply voltage	3.3 V	3.3 V
Output power (max.)	29 dBm	25.9 dBm
Power-added efficiency (PAE)	42.8 %	30%
Output P_{1dB}	27 dBm	23.8 dBm
PAE @ P_{1dB}	40 %	24%

Table 1 · Performance summary.

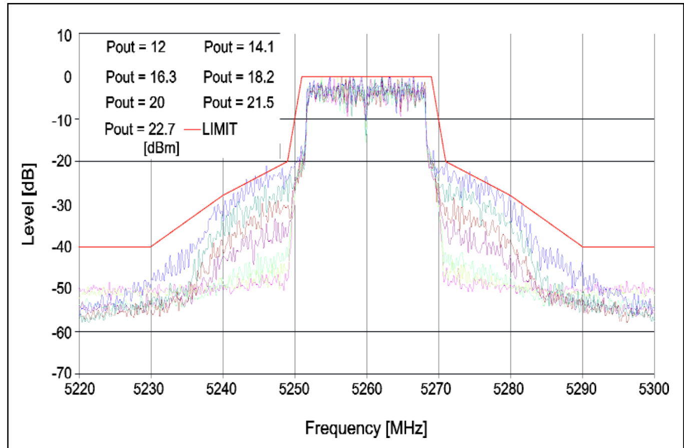

Figure 16 · Measured Spectrum Mask (OFDM 54 Mbit/s, IEEE 802.11a) frequency characteristic.

Summary

The design of an integrated dual-band multi-mode wireless LAN radio frequency power amplifier (Infineon PMB 8825) for the 2.45 GHz and 5.25 GHz supporting IEEE 802.11a/b/g is demonstrated. It has been realized in a 42 GHz f_T, 0.35 µm SiGe-Bipolar high-volume technology using on-chip low inductance ground connections for the reduction of emitter degradation and matching purposes. The chip features a power control block for all necessary controls and two single-ended 3-stage power amplifier with on-chip inductors and a short on-chip stripline for the interstage matching. It is a demonstration for a cost-efficient multi-mode WLAN PA solution, as it is a single-die solution using a minimum of external elements.

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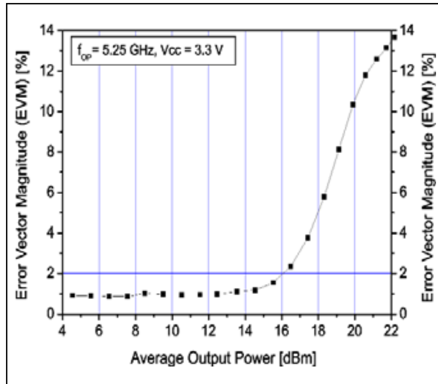

Figure 17 · Measured Error Vector Magnitude (EVM) vs. average output power.

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