From April 2004 *High Frequency Electronics*
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Linearizing Power Amplifiers Using Digital Predistortion, EDA Tools and Test Hardware

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This tutorial article describes the process for developing and implementing an effective linearization scheme using digital predistortion

This article presents a method for power amplifier linearization known as baseband adaptive digital predistortion. Using an EDA software package with both DSP (Digital Signal Processing) and RF capabilities, connected to a vector signal generator and a signal analyzer, this hardware/software connected system allows an actual hardware power amplifier to be optimally linearized for a specific wireless transmission standard.

Introduction

Spectral efficiency is increasingly important in today's mobile communications. The non-constant envelope (high peak-to-average ratio) digital modulation schemes used in many 2.5G and 3G wireless systems make RF power amplifier (PA) linearity and efficiency a crucial design issue. Typically, linearity is achieved either by reducing efficiency or by using linearization techniques. For a Class A PA, simply 'backing off' the input can improve linearity, but this reduces power efficiency and increases heat dissipation. When considering the vast numbers of base stations wireless operators need to account for, increased power consumption is not a viable tradeoff.

Not all linearization methods are equal. One method, known as feedforward technique, is frequently employed. Feedforward technique generally provides good linearity, but it results in poor PA efficiency. All linearization methods are limited in their maximum correctable range, which is region of power output level near the onset of saturation.

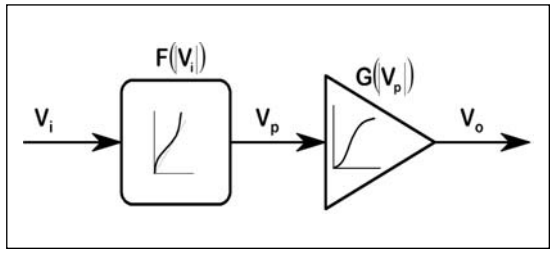

Figure 1 · Digital predistorter followed by a power amplifier.

In this article, we present a promising linearization method, known as baseband adaptive digital predistortion. To evaluate this technique, we built a system around an EDA software package with both DSP and RF capabilities, which can be connected to a vector signal generator and a signal analyzer. With this system we optimally linearized an actual hardware power amplifier for a specific wireless transmission standard.

The Adaptive Digital Predistortion System

Digital predistortion (DP) is used to linearize the nonlinear response of a power amplifier (PA) over its intended power range. It uses digital signal processing (DSP) techniques to predistort a baseband signal before modulation, up-conversion, and amplification by the PA. As a result, the cascade of the DP response and the PA response produces the desired linear response. Figure 1 shows the simplified block diagram. The gain, G, of the PA is modeled as a function of the instantaneous magnitude of the PA's input signal, V_p. The function G is assumed to be memoryless and nonlinear. The use of a memoryless model, that is only dependent upon input sig-

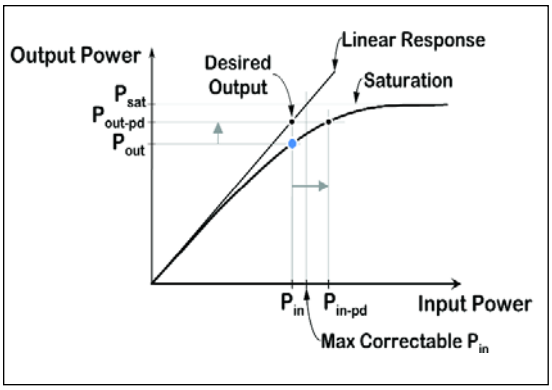

Figure 2 · Power amplifier P_{out} versus P_{in} and digital predistortion.

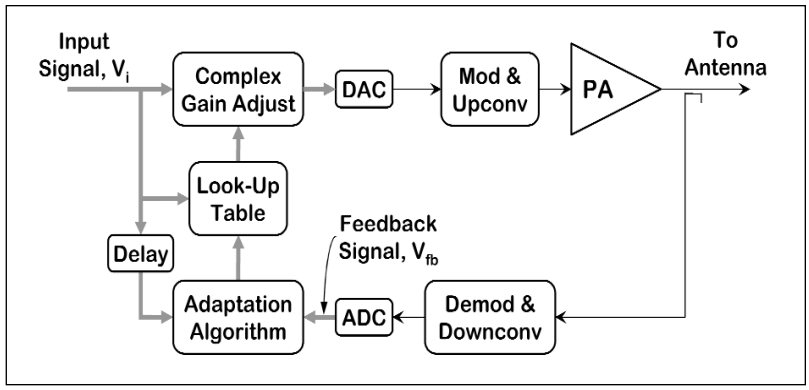

Figure 3 · Digital predistortion block diagram.

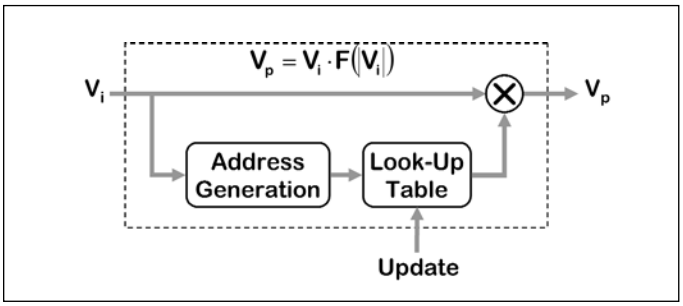

Figure 4 · Complex gain adjust and look-up table.

nal magnitude, is a simplification of the actual response of a typical PA. Other variables will impact the PA response, particularly the operating frequency band and instantaneous operating temperature.

Similar to G, the predistortion function, let's call it F, is made to be a function of the magnitude of the input signal V_i. The circuitry that implements the predistortion function may be referred simply as the predistorter. Thus, the cascade of the predistorter and PA will result in the desired linear response when $F(|V_i|)\,G(|V_p|) = k$, where k is a constant and $V_p = V_i\,F(|V_i|)$. Figure 2 illustrates the typical relationship between the input power and output power of a PA. The heavier dark curve shows that in the absence of DP the PA's P_{out} versus P_{in} curve is nonlinear. However, through the introduction of DP, the P_{out} versus P_{in} curve can be forced to have a linear response over a useful range of input power levels. The desired linear response of the PA is illustrated by the Linear Output curve shown in Figure 2. The slope of the Linear Output curve is the desired linear gain of the PA.

The way DP works is explained in Figure 2. If the amplifier is operating in compression, the P_{out} versus P_{in} curve falls below the Linear Output curve, and the actual output power of the PA is not sufficient for linear operation. Including DP before the PA introduces expansion—the amplitude of the input signal is increased so that the desired output power (falling on the Linear Output curve) is achieved. The expansion effect is shown in Figure 2, where the input power, P_{in} (resulting in P_{out} before DP), is increased to P_{in-pd} so that the PA output power is raised to P_{out-pd}, coinciding with the Linear Output curve. The region of the P_{out} versus P_{in} curve that can be linearized using DP is limited by a number of variables, including the number of coefficients available over the full input power range, the distribution of these coefficients within this range (for example, a higher density of coefficients at the larger input power levels where the PA is most nonlinear), and the dynamic range of the analog-to-digital and digital-to-analog (ADC and DAC) converters.

A block diagram of an adaptive digital predistortion system is shown in Figure 3. With the inclusion of DP, the digital complex baseband input signal samples are multiplied before the DAC by complex coefficients drawn from the Look-Up-Table (LUT). The LUT coefficients implement the predistortion function. The Adaptation Algorithm determines the values of the coefficients by comparing the feedback signal and a delayed version of the input signal. The complex gain adjuster and LUT blocks of Figure 3 are shown in more detail in Figure 4. The predistortion function is implemented using a complex multiplier, a LUT, and an Address Generation block that selects the appropriate coefficient from the LUT, given the magnitude of the input signal.

The size of the LUT employed determines the number of points at which the predistortion function is calculated. In addition, it is not necessary that the predistortion function points be evenly distributed across the range of the input signal magnitude. In some applications, it may be desirable to distribute the predistortion function points across the range of the input signal magnitude using a squared (power) or logarithmic relationship to provide a higher density of coefficients at the higher input power levels where the PA is most nonlinear [3, 4].

The function of the adaptation algorithm is to derive the predistortion function, F, in other words, the inverse

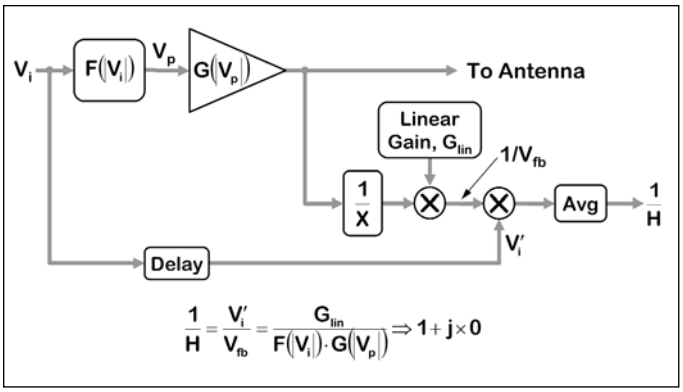

Figure 5 · Implementation of the adaptation algorithm.

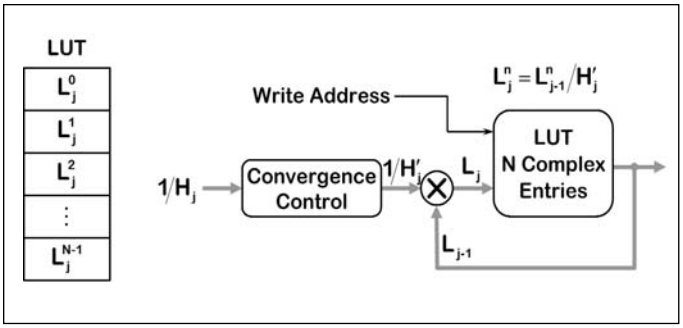

Figure 6 · Calculation of new predistortion function.

characteristic of the amplifier response. The predistortion function may be derived using either a modulated signal input (random signal) or a known training signal. The adaptation algorithm and its implementation are fundamentally different depending upon which type of input signal is utilized. The algorithms that are based on the use of a modulated signal employ statistical signal processing and typically require some type of curve fitting algorithm to generate a smooth predistortion function. The complexity of the adaptation algorithm and its implementation can be significantly simplified by using an alternative input signal—a known training signal [5].

The adaptation algorithm chosen for our implementation is based on the use of a training signal. The training signal is a single tone having a frequency equal to the carrier frequency and whose power is ramped up during the training period. The power of the tone is set to zero at the start of the training period and will typically peak at, or just below, the maximum correctable input power of the amplifier.

Using a single tone whose power is ramped as a training signal greatly simplifies the adaptation algorithm and its implementation. However, using the training signal requires interrupting the modulated signal while the training signal is transmitted. In addition, because the training signal is a single tone, the digital predistorter only corrects for the operation of the amplifier at a single frequency, and not across the entire transmission bandwidth. If the amplifier's passband is quite flat, using a single-tone training signal enables the predistortion function to be determined accurately. Be aware, however, that using a single complex coefficient to correct for distortion of the amplifier at a particular power level presupposes minimal amplifier memory effects.

Figure 5 shows a block diagram of the adaptation algorithm. This algorithm is based on the determination of the open loop gain H of the predistorter and amplifier combination, at the power level associated with each LUT entry. Recall that the desired linear response of the predistorter and amplifier cascade requires that $F(|V_i|)$ $G(|V_p|) = k$ for all inputs. Hence, if G_{lin} is set to be equal to k, the desired open loop gain of the system is unity. If the calculated open loop gain is not equal to unity, the predistortion function must be adjusted to drive the open loop towards unity. Figure 6 illustrates this.

The predistortion function is defined by a set of coefficients stored in the LUT, L_n, where each n corresponds to an input signal magnitude that is mapped to a LUT address. To drive the open loop gain to unity, the predistortion function's coefficients are updated by dividing each coefficient by the calculated open loop gain.

The delay in the feedback path is estimated by calculating the correlation between the magnitude of the input signal and the magnitude of the feedback signal. The benefit of using the signal magnitude is that it does not require phase synchronization in the feedback path. Because the delay in the feedback path will not necessarily be equal to an integer number of DSP sample periods, interpolation is employed. The correlation between the input and feedback signal is performed on a modulated signal that precedes the training signal because the gain compression of the amplifier potentially degrades the accuracy of the correlator's estimation process during the training signal. In general, the accuracy of the estimation improves as the block size increases. However, a larger block size requires more memory and takes longer to calculate.

The predistortion function cannot be determined exactly by following the transmission of a single training ramp. It requires an iterative calculation of the LUT coefficients. A series of training ramps must be transmitted, although significant improvement to the amplifier Adjacent Channel Power Ratio (ACPR) is often observed following just two or three training ramps.

Connected Test Hardware-EDA Software Solution

The traditional design process for modern communication systems typically uses Electronic Design Automation (EDA) tools (software) to create the first design using functional blocks and models. This is followed by intensive sim-

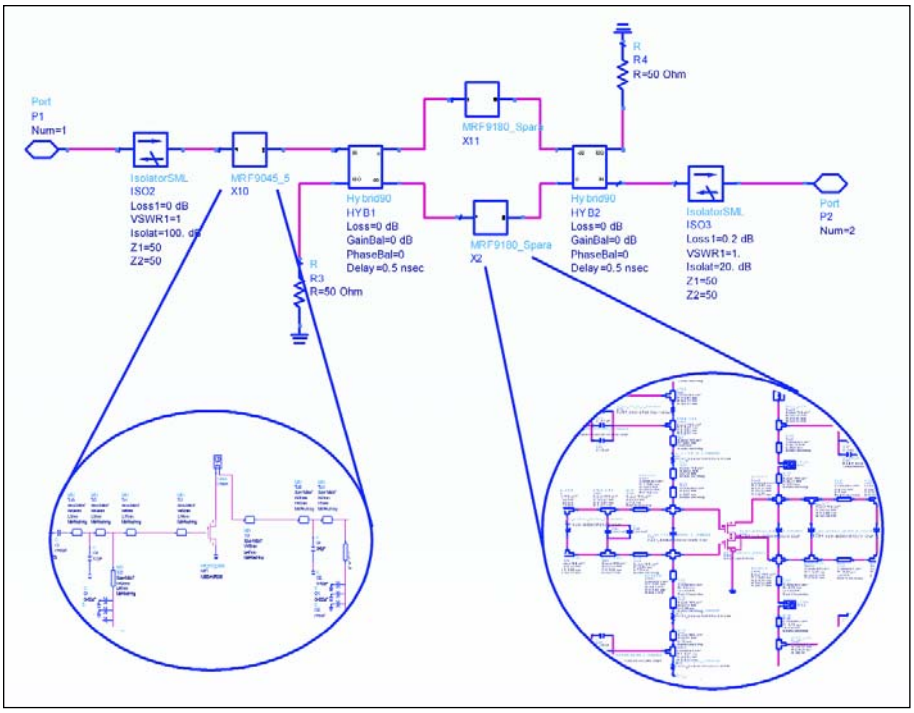

Figure 7 · The PA block diagram defined in ADS.

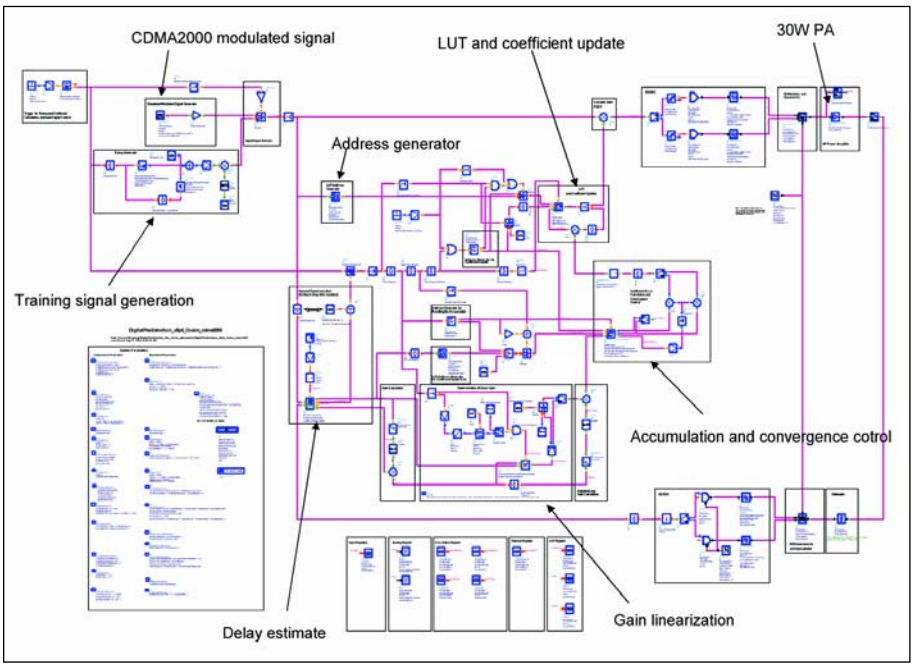

Figure 8 · The complete simulation schematic of the digital predistortion linearizer.

ulation to understand the behavior of the design. Modifications are made until acceptable performance is achieved. Finally, a prototype is fabricated and evaluated with test and measurement hardware. During this hardware measurement process, unexpected problems can arise due to model imperfections and simulation variables.

With our method, we combine EDA software with the test and measurement equipment to help meet emerging requirements that are not addressed by design software or instruments alone. In general, adding real measurements to a simulation helps ensure a successful prediction of the final performance.

Our method used the Advanced Design System (ADS, from Agilent Technologies) for EDA design and simulation. We also used the Linearization DesignGuide, which provides a complete tool kit to interactively explore dynamic linearization systems at the top level as part of an integrated design process. We connected these EDA software tools with test and measurement equipment (signal generator, signal source, and signal generator, also from Agilent Technologies) to create a connected software-hardware digital predistortion system. The system allowed us to work with realistic, complex, and customized test signals and measurements to gain added insight about the performance of the device-under-test.

Simulation and Measurement Results

A 30 W_{rms} power amplifier was designed in ADS using a 170 W Motorola Laterally Diffused Metal Oxide Semiconductor or LDMOS device (MRF 9180) and simulated with the adaptive digital predistortion system in the 880 MHz band. Figure 7 illustrates the PA block diagram as defined in ADS. The PA consists of 3 stages: 1) a MRF9045 amplifier that has a drive amplifier (MHL9236), 2) a MRF9045 amplifier, and 3) a balanced MRF9180 amplifier. The PA, as designed, has 49 dB gain and 54 dBm saturated power. Figure 8 shows the entire ADS schematic of the digital predistorter wherein all subsystems have been implemented in the ADS Agilent Ptolemy simulation environment. Figure 9 illustrates the simulation

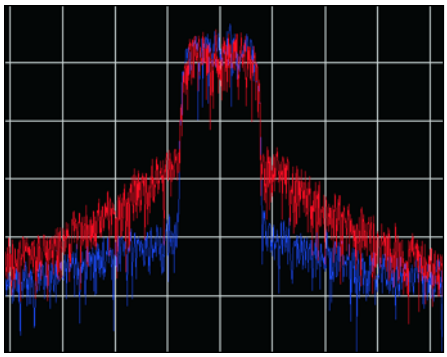

Figure 9 · PA output with and without DP of the modeled PA in ADS (Red: without predistortion; Blue: with predistortion).

results. Approximately 20 dB of distortion correction is achieved at the 45 W output power level.

Figure 10 illustrates the setup for interconnecting the Electronic Signal Generator (Agilent ESG E4438C), amplifier under test (DUT), Vector Signal Analyzer (Agilent VSA 89641A) and the ADS digital predistorter system design. The DUT is illustrated in Figure 11.

The overall simulation of the predistorter consists of two separate ADS simulations—the ESG simulation and the VSA simulation.

The ESG simulation generates and predistorts a modulated signal conforming the desired wireless standard, passing it on to the ESG where the signal is modulated onto an RF carrier. Data files containing both the ideal signal and the predistorted signal are also saved. The RF output of the ESG is directed to the power amplifier whose output is connected through an appropriate attenuator to the VSA. When the VSA simulation is run, the VSA instrument captures the received and downconverted signal, then transfers the signal into the ADS environment. ADS then performs the signal processing necessary to align the received signal with the saved reference signals and adaptively calculate and update the LUT coefficients. A CDMA2000 forward-link-modulated signal with a chip rate of 1.2288 MHz and 9.6 dB Peak-to-Average Ratio (PAR) was utilized for the simulations and measurements. Figure 12 shows the PA output with digital predistortion. The power levels shown include attenuation to protect the VSA's input circuitry. Following three iterations at 45 watts of output power, the out-of-band spectra were reduced by over 15 dB. Compared with the simulation results, a 5 dB difference was observed. This discrepancy may be due to factors such as temperature-based memory effects, test equipment bandwidth limitations (in this case the particular VSA used provided 39 MHz of bandwidth), and the inherent accuracy of the particular MOSFET device model used in ADS.

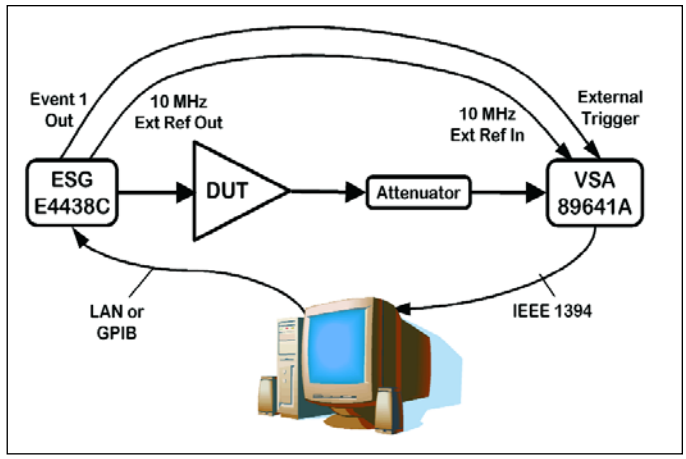

Figure 10 · ESG, VSA, and PC hardware set-up in the connected solution.

Conclusions

The adaptive digital predistortion system was implemented using the Advanced Design System EDA software package with the Linearization DesignGuide, connected to test equipment (ESG signal source and VSA signal analyzer). Through the use of a training signal, a simple adaptive algorithm was employed to update the LUT coefficients used to linearize a candidate Power Amplifier. Significant reduction in out-of-band distortion products was observed. The connected test hardware-EDA software solution approach can also provide key information to design engineers for optimizing the DSP architecture of a candidate PA linearized using digital predistortion. For example, the effect of changing the number of LUT coefficients may be rapidly observed. Further improvements may be possible by addressing other issues, such as temperature and electrical memory effects, as well as by using wider measurement bandwidths.

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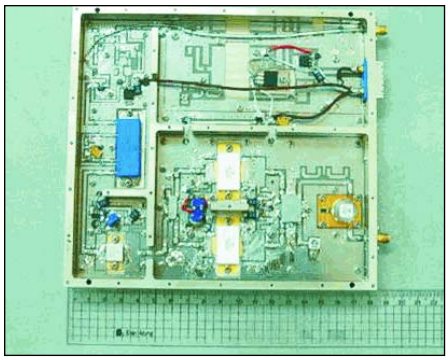

Figure 11 · The 30 W_{rms} power amplifier developed for the linearization experiments.

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Professor Shawn P. Stapleton has taken a leave of absence from Simon Fraser University, and is currently employed as CTO at PropheSi Technologies. His research at SFU has focused on integrated RF/DSP applications for wireless communications, GaAs MMIC circuits and PA and optical linearization. He received his BEng in 1982, MEng in 1984 and PhD in 1988 from Carleton University, Canada. Before joining Simon Fraser University, Shawn worked on a wide variety of projects including optical communications, RF/Microwave communications systems, and adaptive array antennas. While at Simon Fraser University he developed a number of adaptive linearization techniques ranging from feedforward, active biasing and work function predistortion to digital baseband predistorters. He has developed PLL, linearization and communications design software for the wireless industry. Earlier in his career, he was a Staff Scientist at Scientific Atlanta where he worked on CATV headend equipment.

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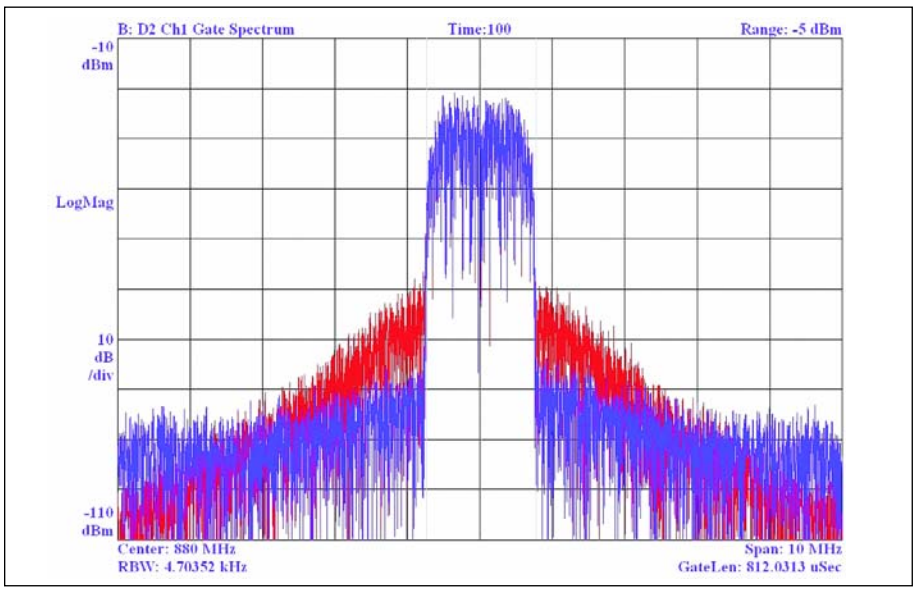

Figure 12 · PA output with and without DP of the actual hardware PA (Red: without predistortion, Blue: with predistortion).