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A Balanced 24-Volt GaAs FET Amplifier for 2.11to 2.17 GHz

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This article describes the device characterization, design, construction and testing of a power amplifier built using a push-pull 24-volt GaAs FET

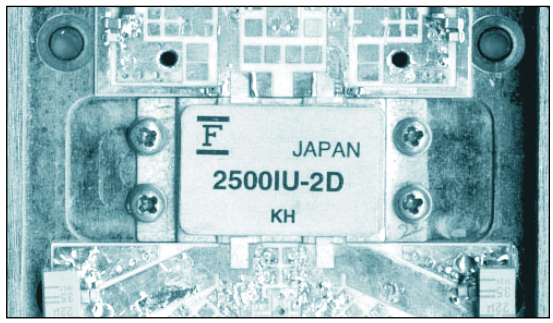
The development of 24-volt drain bias GaAs FETs has been the "holy grail" of power device design. For a long time, the achievement of 24-volt devices seemed just around the corner. Fujitsu has now placed into volume production a series of 24-volt V_{ds} GaAs FET quasi-enhancement-mode devices. The three devices have equivalent modulated output power of 250 W, 150 W and 10 W. These devices have modulated performances equivalent to higher power devices and cover a 2.11 to 2.17 GHz instantaneous bandwidth.

This article describes the characterization of the FL2500IU-2D push-pull device and the design, construction, and performance test results for an amplifier biased at Class AB, deep into Class B.

Design Goals

GaAs FET quasi E-mode devices running on 12 volts V_{ds} have long been in production with P_{out} up to 240 W. Now the same series of high-reliability GaAs FET quasi E-mode devices are available operating on 24 volts V_{ds} for better linearity. This article covers the 250 W equivalent device in the chain, the FLL2500IU-2D.

The FLL2500IU-2D push-pull device was fully characterized across its potential application frequency range and these parameters were used to design an easy-to-produce amplifier for use over the 2.11 to 2.17 GHz bandwidth. After the amplifier was built by modifying an existing design, an initial evaluation was performed.



The amplifier uses a Fujitsu FLL2500IU-2D GaAs FET in a push-pull design.

Device Description and Characterization

The FLL2500IU-2D [1] is an L-band pre-matched dual independent device (push-pull) using four Quasi-E-mode chips optimized at 24 V for high efficiency and good linearity at high modulated drive levels in the L-band. To achieve 24 V operation, breakdown voltage was increased to over 50 volts. The chips and the input and output pre-matching circuits were mounted in an IU package.

FLL2500IU-2D Load- and Source-Pull Data

The device was first characterized with a Focus load/source-pull automated tuner system in the 1.8 to 2.8 GHz band at V_{DS} = 24 V and I_{DSQ} = 1 A on one of the two identical sides only. The S-parameters were measured on the same side from 1.0 to 4.4 GHz at V_{DS} = 24 V and I_{DSQ} = 1 A. Z_{in} and Z_{out} are the input and output impedances when, simultaneously, Z_{source} is optimized for gain, with Z_{load} optimized for output power, P_{out}. The S-parameters were used to optimize the input circuit for gain and gain flatness and to analyze the amplifier stability.

Amplifier Board Material

The board material selected was Rogers 4350, with consideration for its low loss tangent of 0.004, its relative dielectric constant of $\varepsilon_r = 3.48$ (which allows reasonable amplifier dimensions) and its relatively low cost. One-ounce copper, plated up to 2 ounces (.068 mm copper thickness) in processing, was used to minimize I^2R losses in the board copper.

DC Bias Circuit Topology

Gate Biasing Circuit: A 0.5 ohm gate resistor, R_g, was connected in series with the gate-biasing circuit for gate protection and stability. It was placed at the input of the quarter-wavelength transmission line. Note that the gate driver must be able to both source and sink a significant amount of current. An op amp or transistor follower placed between the rails is recommended in the end application. For lab testing, a 0.2-ohm resistor was placed across the gate power supply before the current meter was encountered.

Next came a quarter-wave length high-impedance microstrip line short-circuited at its extremity by a capacitor with a series resonant frequency near 2.2 GHz. A 70-ohm transmission line was used due to the "low" (>0.5 A) gate current. Additional capacitance was needed on the bias line for IF bypassing on the supply side of the RF bypass capacitor [2].

Drain Bias Circuit: The amplifier drain biasing circuit consisted of a quarter-wave length microstrip line connected at one end to the output matching circuit. It was short-circuited at the opposite end by a capacitor with a series-resonant frequency near 2.2 GHz. The quarter-wavelength microstrip line is low impedance since it has to carry high maximum drain current when the device is in compression, in order to improve IF impedance. In this initial evaluation an ultra-wide 6-mm line was used (for more information, see [2]). The electrolytic capacitors must have rated working voltages above the application voltage, so 10 µF 35 WV tantalum low ESR surface mount capacitors were used. All ceramic capacitors had ratings in excess of 50 WV.

DC Blocking Capacitors: In each input and output circuit a high quality multi-layer chip capacitor (ATC 100A series) with a series resonant frequency at or above 2.14 GHz was used as the DC blocking element. Their impedance at $f = 2.14$ GHz was very low in comparison to the 50-ohm system impedance and thus insertion loss was also very low.

Coupler and Coupler Resistor Selection: A number of manufacturers make acceptable surface mount couplers for this band. Soshin makes the smallest parts for the highest power ratings, using ceramic construction. Merrimac, Mid-Atlantic, and Anaren also make stripline surface mount couplers. All are rated at 100 W in the .35 x .50 size used in this design, although in reality they are capable of withstanding higher power than their ratings. Only RF Power (Anaren) and Soshin make parts rated for 200 W. The existing design used an Anaren coupler at the input and an RF Power high power coupler at the output.

A 50-ohm coupler termination resistor was required in the terminated leg of each coupler. The rule of thumb is that the coupler termination should be rated at 10 percent of the power applied to the coupler. For the input power requirement—10 percent of the applied power of 2 W max.—this is fairly low. For the output, the rating should be 10 to 20 W minimum. The author is aware of four vendors in the U. S. that make the required high-power, small-size resistor. This resistor must be a thin- or thick-film single-layer design with wrap-around ground at one end for required RF performance, on either BeO or TaN material for required power performance. TaN is preferred for toxicity reasons, when available. Florida RF Labs (leaded devices only), RF Power, IMS (ANX series), and SOTA all make suitable devices. The resistor must be soldered directly to the amplifier housing through a slot cut out of the PC board to achieve the required rating. To simplify assembly and parts procurement, the same resistor was used at the input and output of the sample design. A 100 mil x 200 mil size resistor is required, rated from 14 to 35 W depending on the manufacturer.

Circuit Design

Design Methodology: The amplifier circuit design for a balanced amplifier using 90 degree hybrids was created in several steps (a balun or 180 degree splitter approach is similar except for the substitution of 25-ohm for 50-ohm impedance in a balun design).

1. Z_{out} to 50-ohm impedance was matched with best return loss possible in the bandwidth of interest. The output match circuit was not modified since no compromises should be made concerning the output power.
2. Z_{in} was matched to 50-ohm impedance in the band of interest with best return loss possible. This defined the input circuit configuration and the initial values of its elements.
3. The gain and gain flatness of the amplifier was optimized. The S-parameters of the device were used with both match circuits and only the elements of the input circuit were optimized. Normally the initial and final values of the input circuit elements are very close, as Z_{in} is easy to match.
4. The amplifier stability in broadband with the S-parameters of the device was analyzed. This had to be done without the input and output quadrature couplers.
5. Two instances of the amplifier were placed between couplers to predict the final performance.

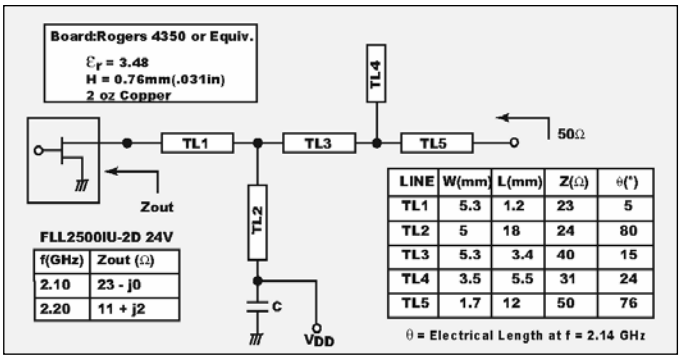


Figure 1 · Amplifier simplified output matching circuit (2.11-2.17 GHz).

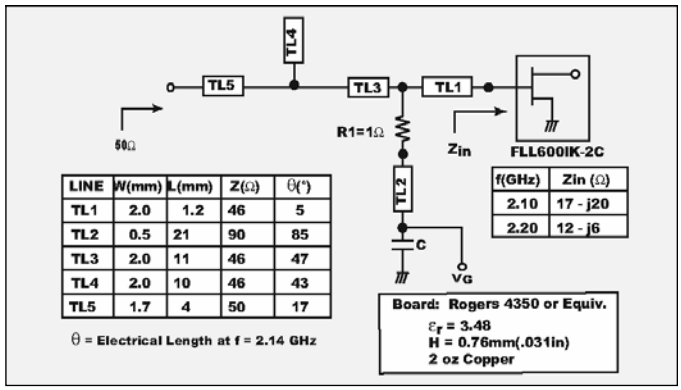


Figure 2 · Amplifier simplified input matching circuit (2.11-2.17GHz).

Output Matching Circuit Design

The output matching circuit is shown in Figure 1. This circuit consists of:

- A line, TL1, that allowed the device to be mounted without cutting its drain leads.
- A line, TL2, for drain bias. The parasitics of the via hole and bypass capacitor were included in the model. This is not part of the matching circuit in this case since it is practically a quarter wave length line (80 vs. 90 degrees), although due to the wide line length this is not universally true.
- A line, TL3, to bring the conductance, G, of the output admittance, $Y = \Gamma + jX$, to a value G = 20 mS.
- A parallel open-circuited stub, TL4, to cancel the susceptance, X, of the admittance and obtain a real impedance, $Z = 1/\Gamma = 50$ ohms.
- A line, TL5, is available to transform the real impedance, Z, to 50 ohms. Since Z = 50 ohms, TL5 simply connects the output circuit to the amplifier output port.
- The DC blocking capacitor was placed in a convenient position in line TL5.

The above explanation is a simplified one, since an instantaneous band of 2.11 to 2.17 GHz should be covered for power.

Input Matching Circuit Design

Figure 2 shows the input matching circuit for optimal gain and gain flatness. A simplified circuit description starting from the device gate is:

- A line, TL1, that allows the device to be mounted without cutting its gate leads.
- A line, TL2, short-circuited at its extremity by a capacitor, was placed in series with Rg. In this case the circuit has no matching function, since 86 degrees is practically a quarter wave-length line. The gate bias circuit was connected as close to the plane of the gate as possible for stability and protection purposes.
- A line, TL3, to bring the conductance, G, of the input admittance, $Y = \Gamma + jX$, to a value $\Gamma = 20$ mS.
- A shunt resonator, TL4, to bring the input impedance as close as possible to 20 mS (50 ohms) across the band
- A series 50-ohm line, TL5, connects the input circuit to the amplifier input port. The amplifier circuit was analyzed using the device S-parameters measured from 0.1 to 4.4 GHz.

The amplifier input circuit was optimized for gain and gain flatness for a 2.11 to 2.17 GHz bandwidth. Performance was also looked at outside the band for smooth roll off.

Stability Factor

The stability of the single-ended device broadband was analyzed by using its S-parameters. The stability K-factor was calculated from 1 to 4.4 GHz and found to be greater than 1. Since the amplifier has no feedback, it is also unconditionally stable. The gate resistors, drain R_d resistor/capacitor network, and decoupling capacitors should stabilize the amplifier at lower frequencies.

Balanced Amplifier

The completed single-ended amplifier model was turned into an instance and placed between couplers. Coupler S-parameters from the vendors were used in the model. The results differed very slightly from the single-ended model except that the input and output return losses were considerably improved.

Amplifier Layout

The final amplifier circuit consisted of the input and output matching circuits, DC blocking, and bypass circuitry. A partial set of decoupling capacitors recommend-

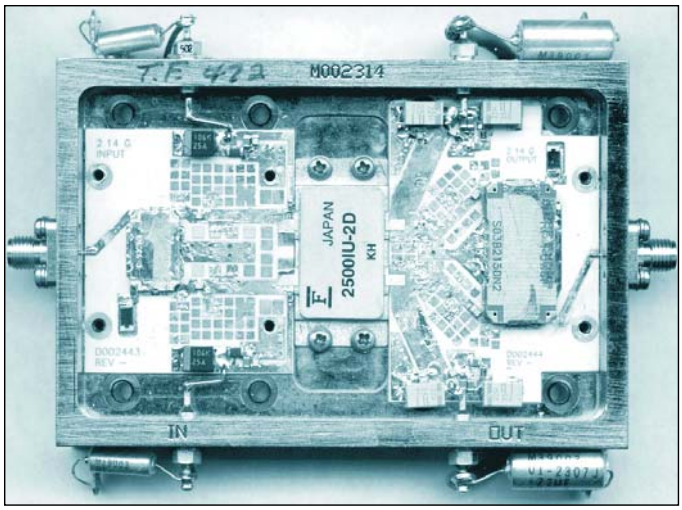


Figure 3 · A photo of the amplifier, which is tuned for best two-tone ACPR performance.

Specification	Target	Performance
Linear Gain	14.0 dB	14.7 dB min
Gain Flatness 2.11-2.17 GHz (peak-to-peak)	1.0 dB	0.4 dB max
Saturated Output Power (tuned for IM3 performance)	52 dBm	52.2 dBm
Power-Added Efficiency η_{add} at P_{sat}	45%	53%
η_{add} for W-CDMA signal at 44 dBm Average	17%	20%
IM3 Two-Tone CW 44 dBm P_{out} Average	–32 dBc	–38 dBc
IM3 Two-Tone W-CDMA 44 dBm P_{out} Average	–35 dBc	–35 dBc
ACPR at 44 dBm P_{out} Average	–39 dBc	–39.5 dBc

Figure 4 · Table of FLL2500IU-2D target specifications vs. test results.

ed in AN-010 [2] was connected in the gate and drain bias circuits. See Figure 3 for a photograph of the tuned amplifier. The amplifier internal dimensions (boards plus device) measure 95 x 44 mm [3].

Large-Signal Circuit Tuning

The best load/source-pull data are only accurate to within about 10 percent. Therefore, to obtain optimum results some fine tuning was necessary after amplifier assembly. The FLL2500IU-2D internal pre-matching circuit made the optimization of the external circuit easy to achieve. Once the correct tuning was found, consistent performance was observed as the tuning was very similar between amplifiers.

The power performance of the FLL2500IU-2D demonstrates a very soft power knee, similar to a TWT or an LDMOS part. This suggests that linearity should be significantly improved while preserving good efficiency. Note that the optimal match to get P_{out} and power-added efficiency, η_{add}, with a CW signal is slightly different from the optimal match for ACPR. Optimal tuning for IM3 performance with a two-tone W-CDMA signal occurs at yet a different match point. Since the units were tuned for two-tone WCDMA performance the maximum P_{out} was degraded significantly.

Measured Results

The performance obtained with the FLL2500IU-2D device is presented in the table in Figure 4. It shows a summary of performance compared to original targeted specifications. This table shows that all the targeted goals were met or exceeded. The data presented are from a single representative device chosen from three tested in the same amplifier.

Conclusion

The FLL2500IU-2D device is a useful device for driving high-power output stages or as a stand-alone output stage for medium-power applications . A balanced amplifier using 90-degree hybrids designed around this device demonstrated excellent performance. Gain was 14.5 dB minimum, with less than 0.3 dB peak-to-peak flatness. External match was excellent. Linearity was shown three ways, with ACPR of <–39 dBc at 44 dBm output, and IM3 for both CW and WCDMA modulated signals being <–35 dBc for 44 dBm average power output. Class AB operation yielded high efficiency of 23% at the back-off point of 40 dBm, and 52% at P_{out} max. This design can be used as a basis power output stage for base amps.

Notes

1. A data sheet for the FLL2500IU-2D can be found at the Fujitsu web site: www.fcsi.fujitsu.com)

2. R. Basset, "Biasing High Power FET Devices (Part I)", *Microwaves & RF,* Jan 2002, pp. 66-76; "Setting Bias in High-Power GaAs FET Devices (Part II)," *Microwaves & RF,* Mar 2002, p. 80-84. (Complete article can be found as App. Note AN010 on the Fujitsu Web site *www.fcsi.fujitsu.com*)

3. R. Basset, "Understanding Thermal Basics For Microwave Power Devices," *Microwaves & RF,* October 2000, pp. 101-110.

Author Information

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