AN3008 Application Note

Using the DR65-0109 to Drive SPDT PIN Switches

V 1.00

Introduction

For use as a replacement part to the DR65-0003 PIN Driver.

This Application Note describes how to use the M/A-COM DR65-0109 Single Channel Driver for FET Switches as a SP2T PIN Diode Driver. When configured per the directions herein, the DR65-0109 will provide the same functionality as the DR65-0003 in the same package style, HOWEVER THE PINOUT IS DIFFERENT. **USING THE DR65-0109 AS A DIRECT DROP-IN REPLACEMENT WITHOUT DOING A PCB CHANGE WILL NOT WORK!**

Pin Assignments

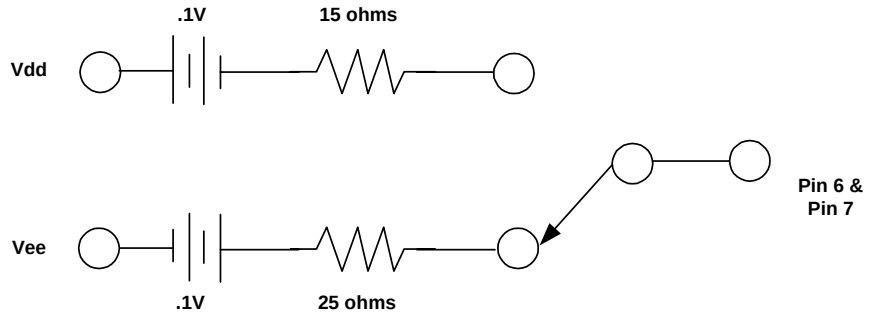
Pin#	Function	Pin #	Function
1	Vcc	5	Ground
2	Logic Input	6	Non-Inverting Output
3	Vdd	7	Inverting Output
4	Ground	8	Vee

Electrical Specifications: T_A = +25°C, +Vcc = + Vdd = + 5.0V ± 5%, -Vee = - 5.0V ± 5%

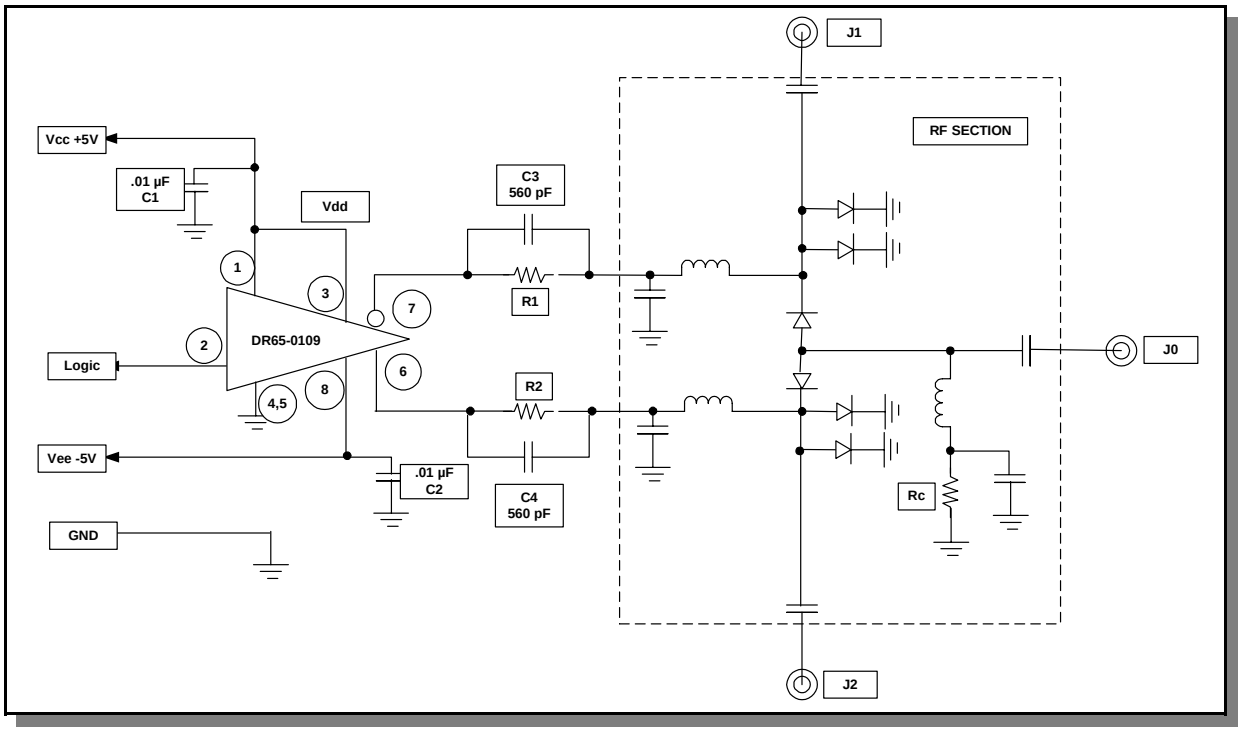
Parameter	Test Conditions	Units	Min	Typical	Max
Switching Speed [1] Delay Rt/Ft	Spike current into 10 ohm load 50 % TTL to 90% 10%-90%; 90%-10%	 nS nS	 — —	 25 2	 35 5
PRF	50% duty cycle	MHz	DC	—	5
Output Voltage Drop, No Load	With reference to supply voltage	V	—	—	.25
DC Output Current Peak Spike Output Current	Load Dependent Spiking Capacitor in Circuit	mA mA	— —	±30 ±150	±50 ±200
Output Stage on Resistance	Positive Output FET, Qp Negative Output FET, Qn	W W	— —	15 25	— —
Quiescent Supply Currents	+5V -5V	mA mA	— —	— —	1.0 .2
TTL Levels	Logic “0” @ 20 µA sink current Logic “1” @ 20 µA source current	V V	0 2.0	— —	.8 5.0
Package Dissipation	—	mW	—	—	200

1. Decoupling capacitors (.01 µF) are required on power supply lines.

Equivalent Output Circuit for Pins 6 & 7



Typical Application for SP2T Circuit



Description of Circuit

The DR65-0109 provides 2 complementary outputs that are each capable of driving a maximum of ±50 mA into a load. In addition, with proper capacitor selection (C3 & C4) used in parallel with the current setting resistor (R1 & R2), a maximum of ±200 mA of spiking current can be achieved. Configurations using DC steering diodes and a lower Vdd supply will decrease the peak spiking current available to the user.

To achieve the Non-Inverting and Inverting complementary voltages, each output is switched between two internal FETs. The FETs are connected to Vdd for the positive output and Vee for the negative output. Vdd and Vee are adjustable for various configurations and have the following limitations: Vee can be no more negative than –5.5volts; Vdd can be no more positive than 5.5 volts AND Vdd must always be less than or equal to Vcc. Increasing Vdd beyond Vcc will prevent the device from switching states when commanded to by the logic input. Recommended configurations are to drive Vee at –5.0 volts and Vcc and Vdd should be tied together at 5 volts.

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