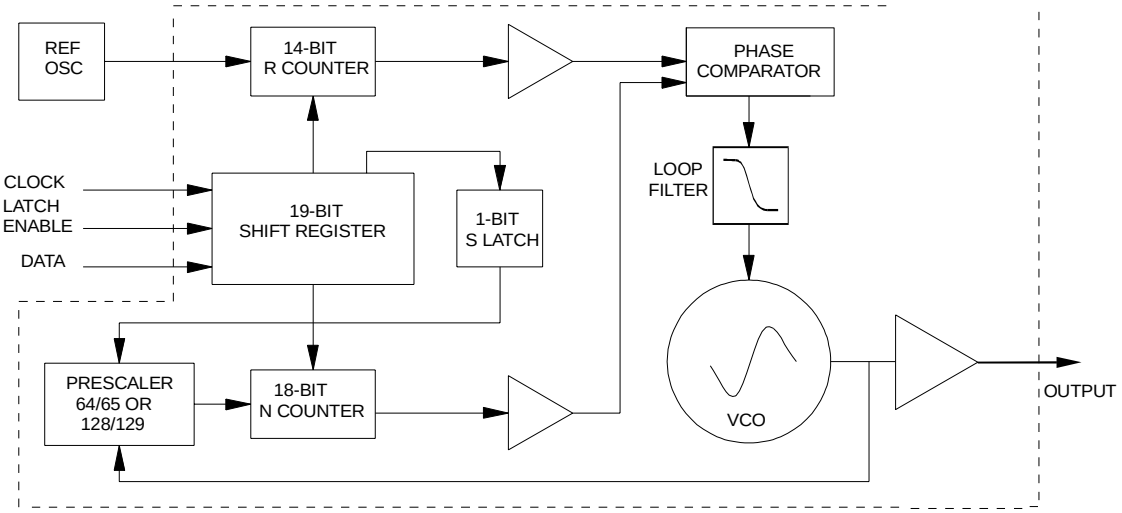
Programming Guide
Integer N PLL Synthesizer 35 to 1100 MHz

Introduction

M/A-COM's surface mount frequency synthesizers integrate a low noise buffered VCO, phase locked loop circuit and low pass loop filter. The VCO output is coupled into the PLL circuit where the VCO frequency is divided down in a dual modulus prescaler and 18 bit N Counter or feedback divider (7 bit swallow counter and 11 bit programmable divider) to the phase comparison frequency or step size of the PLL. This is usually in the range of 10 kHz to 5 MHz for most applications. The external reference oscillator is also divided down in the 14 bit programmable R Counter or reference divider to the same phase comparison frequency.

The divided VCO and divided reference signals are then fed into the phase comparator which produces an error signal whose magnitude is proportional to the phase difference between the two signals. The error signal is then passed through a loop filter to produce the desired performance characteristics and the result is a voltage which is applied to the tuning input of the VCO. The frequency of the VCO is then steered to the desired frequency, at which point the phase difference in the phase comparator will be zero. The phases of the divided VCO and the divided reference signals are then said to be 'locked' to one another, hence the term phase locked loop.

Any subsequent phase or frequency perturbation on the VCO output results in an error signal at the output of the phase comparator. This error signal in turn produces a modification of the tuning voltage to maintain the phase locked condition. A typical synthesizer bock diagram is shown below.



TYPICAL BLOCK DIAGRAM

Programming Overview

The programmable dividers and counters are serially programmed using a standard 3-wire CMOS or TTL interface. The programming data is input using the Clock, Data and Latch Enable input pins. The Clock input latches one bit on the Data input into the PLL shift register on the rising edge of each clock pulse (MSB first). When the Latch Enable input is HIGH the stored data is transferred into the latches. If the last or control bit of the data word is HIGH, data is transferred into the 14 bit latch to programme the R Counter reference division ratio and into the 1 bit S Latch to select the dual modulus prescaler value of either 64/65 or 128/129. This reference word is programmed into the synthesizer first. If the control bit is LOW, data is transferred into the 18 bit latch to programme the N Counter feedback division ratio, this is the frequency word. Once the reference word has been sent the frequency word can be changed to step the output frequency of the synthesizer without re-sending the reference word.

Prescaler Selection

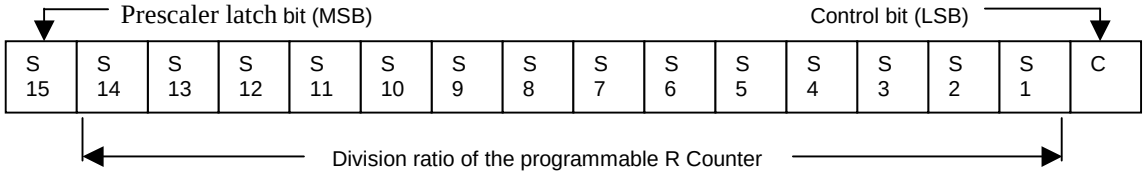
The selection of either the 64/65 or 128/129 prescaler is determined by the maximum step size allowable for the minimum synthesizer output frequency required. The maximum step size or phase comparison frequency allowable for a given output frequency is given by.

$\Delta F < F_{MIN} / P (P - 1)$

Where ΔF = phase comparison frequency or step size, F_{MIN} = minimum synthesizer output frequency and P = prescaler modulus.
For example, the maximum step size allowable to programme F_{MIN} = 825 MHz using the modulus 128 prescaler would be.
ΔF < 825 MHz / (128 x 127) = < 50 kHz Using the modulus 64 prescaler would allow step sizes up to 200 kHz.

Programming the Reference Word (R Counter and S Latch)

If the control bit (C) is HIGH, data is transferred from the 19 bit shift register into a 14 bit latch which sets the R Counter (S14 – S1) and a 1 bit S Latch (S15) which sets the dual modulus prescaler value. The serial data format of the reference word is shown below together with programming tables for the S Latch and R Counter.



1 Bit Prescaler S Latch

Prescaler Select (P)	S 15
128/129	0
64/65	1

14 Bit Programmable R Counter

Division Ratio (R)	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
16,383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes
R division ratios less than 3 are prohibited.
R division ratios from 3 to 16383 are allowed.
S1 to S14 bits select the divide ratio of the programmable reference divider.
C control bit set to HIGH level to load R Counter and S Latch.
Data is shifted MSB first.

Example

The reference division ratio for the programmable R Counter is calculated using: $R = F_{REF} / \Delta F$.

Where R = R Counter division ratio, F_{REF} = reference oscillator frequency and ΔF = phase comparison frequency or step size. Note that the reference frequency used must be an exact multiple of the required phase comparison frequency and synthesizer step size.

For example, programme the synthesizer to use a phase comparison frequency and synthesizer step size of 30 kHz using a reference frequency of 12 MHz and to select the 128 modulus prescaler.

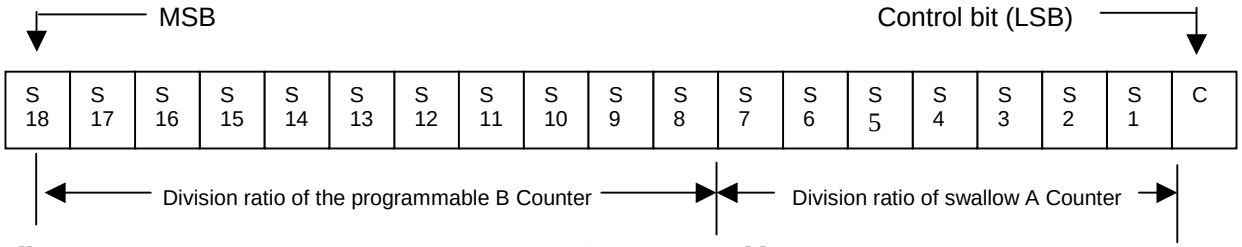
This would require an R Counter division ratio of R = 12 MHz / 30 kHz = 400 = 110010000 in binary
Selecting the 128 modulus prescaler would require S15 = 0
Selecting the reference word would require C = 1

The complete 16 bit binary reference word to be programmed would then be as below.

MSB																LSB
	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1

Programming the Frequency Word (N Counter)

If the control bit (C) is LOW, data is transferred from the 19 bit shift register into a 7 bit latch which sets the 7 bit swallow A Counter (S7 – S1) and an 11 bit latch which sets the 11 bit programmable B Counter (S18 – S8). The serial data format of the frequency word is shown below together with programming tables for the A Counter and B Counter.



7 Bit Swallow A Counter

Division Ratio (A)	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
●	●	●	●	●	●	●	●
127	1	1	1	1	1	1	1

Notes A division ratios from 0 to 127 are allowed.
B ≥ A

11 Bit Programmable B Counter

Division Ratio (B)	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
●	●	●	●	●	●	●	●	●	●	●	●
2047	1	1	1	1	1	1	1	1	1	1	1

Notes B division ratios less than three are prohibited.
B division ratios from 3 to 2047 are allowed.
B ≥ A
C control bit set to LOW level to load A and B Counters.
Data is shifted MSB first.

Example

The feedback division ratio for the programmable N Counter is calculated using: $N = F_{OUT} / \Delta F$

Where N = N Counter division ratio, F_{OUT} = synthesizer output frequency and ΔF = phase comparison frequency or step size. Note that the output frequency must be an exact multiple of the phase comparison frequency and synthesizer step size. The step size is usually determined by system specifications or the required channel frequency resolution.

In order to program the A and B Counters the following mathematical relationship is used: $N = (P \times B) + A$

Where P = modulus of the prescaler (64 or 128), B = B Counter division ratio determined by the integer of N/P, and A = A Counter division ratio determined by the remainder of N/P.

For example, programme the synthesizer to an output frequency of 825 MHz using a phase comparison frequency or step size of 30 kHz and prescaler modulus equal to 128.

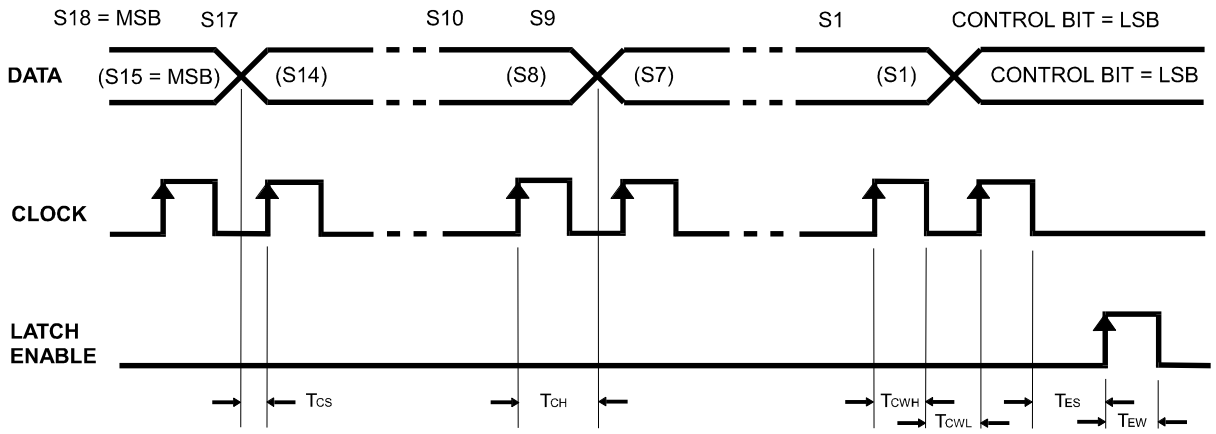
This would require an N Counter division ratio of $N = 825 \text{ MHz} / 30 \text{ kHz} = 27500 = (P \times B) + A$
Using the modulus 128 prescaler B = integer of $N / P = 27500 / 128 = 214 = 11010110$ in binary
And A = remainder of $N / P = 27500 - (128 \times 214) = 108 = 1101100$ in binary
Selecting the frequency word would require $C = 0$

The complete 19 bit binary frequency word to be programmed would then be as below.

MSB																			LSB
	0	0	0	1	1	0	1	0	1	1	0	1	1	0	1	1	0	0	0

Serial Data Input Timing Diagram

Data in parenthesis indicates reference word data. Data shifted into register on rising edge of clock pulses, MSB first.



Electrical Characteristics

Vcc = 5.0V and -40°C <T_A < 85°C except as specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage		$0.7V_{CC}$			V
V_{IL}	Low-Level Input Voltage				$0.3V_{CC}$	V
I_{IH}	High-Level Input current (Clock, Data)	$V_{IH} = V_{CC} = 5.5V$	-1.0		1.0	µA
I_{IL}	Low-Level Input current (Clock, Data)	$V_{IL} = 0V$ $V_{CC} = 5.5V$	-1.0		1.0	µA
I_{IH}	High-Level Input current (LE, FC)	$V_{IH} = V_{CC} = 5.5V$	-1.0		1.0	µA
I_{IL}	Low-Level Input current (LE, FC)	$V_{IL} = 0V$ $V_{CC} = 5.5V$	-100		1.0	µA
V_{OH}	Lock Detect Voltage	$I_{OH} = -1.0mA$	$V_{CC} – 0.8$			V
V_{OL}	Lock Detect Voltage	$I_{OL} = -1.0mA$			0.4	V
T_{CS}	Data to Clock Set Up Time	See Data Input Timing	50			ns
T_{CH}	Data to Clock Hold Time	See Data Input Timing	20			ns
T_{CWH}	Clock Pulse Width High	See Data Input Timing	50			ns
T_{CWL}	Clock Pulse Width Low	See Data Input Timing	50			ns
T_{ES}	Clock to Enable Set UP Time	See Data Input Timing	50			ns
T_{EW}	Enable Pulse Width	See Data Input Timing	100			ns