iC-NG
APPLICATION NOTES

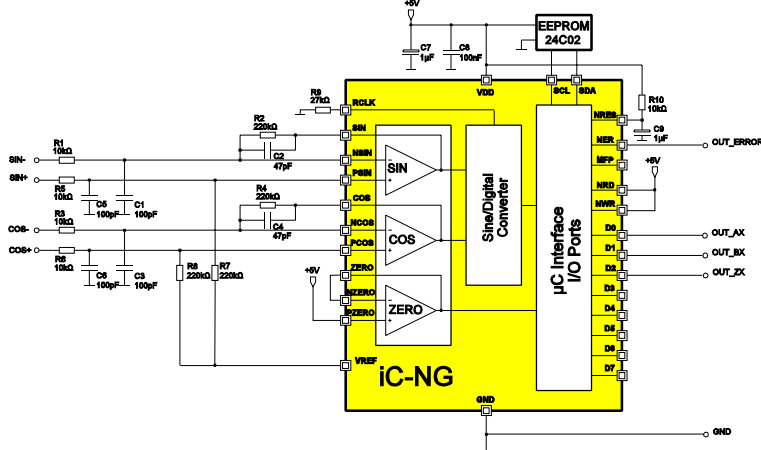## APPLICATION CIRCUITS

Basic circuit (incremental mode)

Fig. 1: basic circuit with low-pass filters for complementary input signals.

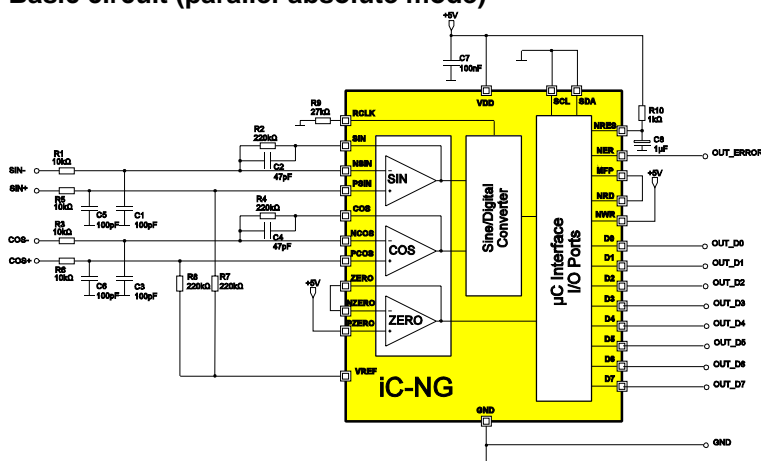### Basic circuit (parallel-absolute mode)

Fig. 2: circuit as an 8-bit sine/digital converter.

iC-NG can be directly connected as an 8-bit sine/digital converter, where the data output in parallel-absolute mode is controlled by the iC's own interrupt signal.

To this end, signal output MFP must be connected to read signal NRD; parallel operation is set by SCL= 0 and SDA= 0 (or configured via EEPROM). Output value register NG(7:0) is addressed after the device has been switched on by presetting the address to "0";

a negative edge for read signal NRD accepts the contents of register NG for output to data lines D7..0. Since the signal enables for NGUPDT and MAXFREQ are also issued as presettings, any signal change automatically appears on the data lines.

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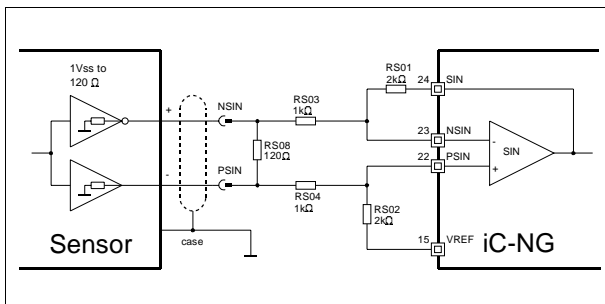
Possible input circuits

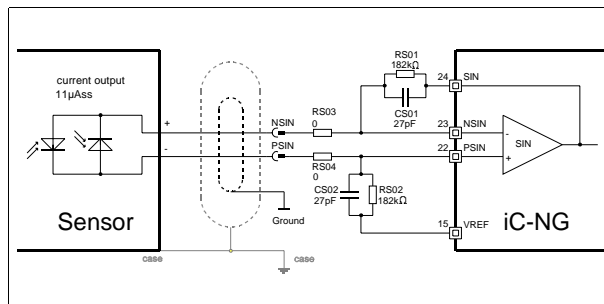
Fig. 3: input circuit for voltage signals with 1Vss.

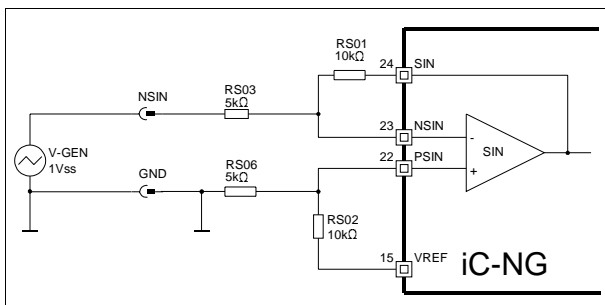Fig. 4: input circuit for current signals with 11µAss.

Fig. 5: input circuit for non-symmetrical voltage signals.

Input circuit with offset compensation
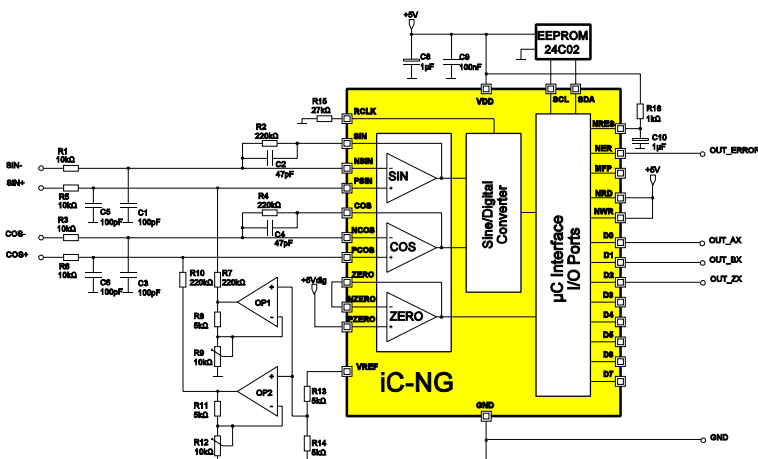
Fig. 6: circuit with external offset compensation.

With iC-NG, the offset parameters are evaluated with the amplitude of the input signal not used in the segment in order to keep the intersections of the segment junctions stable. This concept is required to correct the signals of phase-shifted and distorted sine/cosine signals.

External offset compensation may be necessary for sensor applications with varying signal amplitudes; the linearity of the converter suffers if the signal amplitude changes once the compensation parameters have been set.

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Application circuitry for an MR sensor system
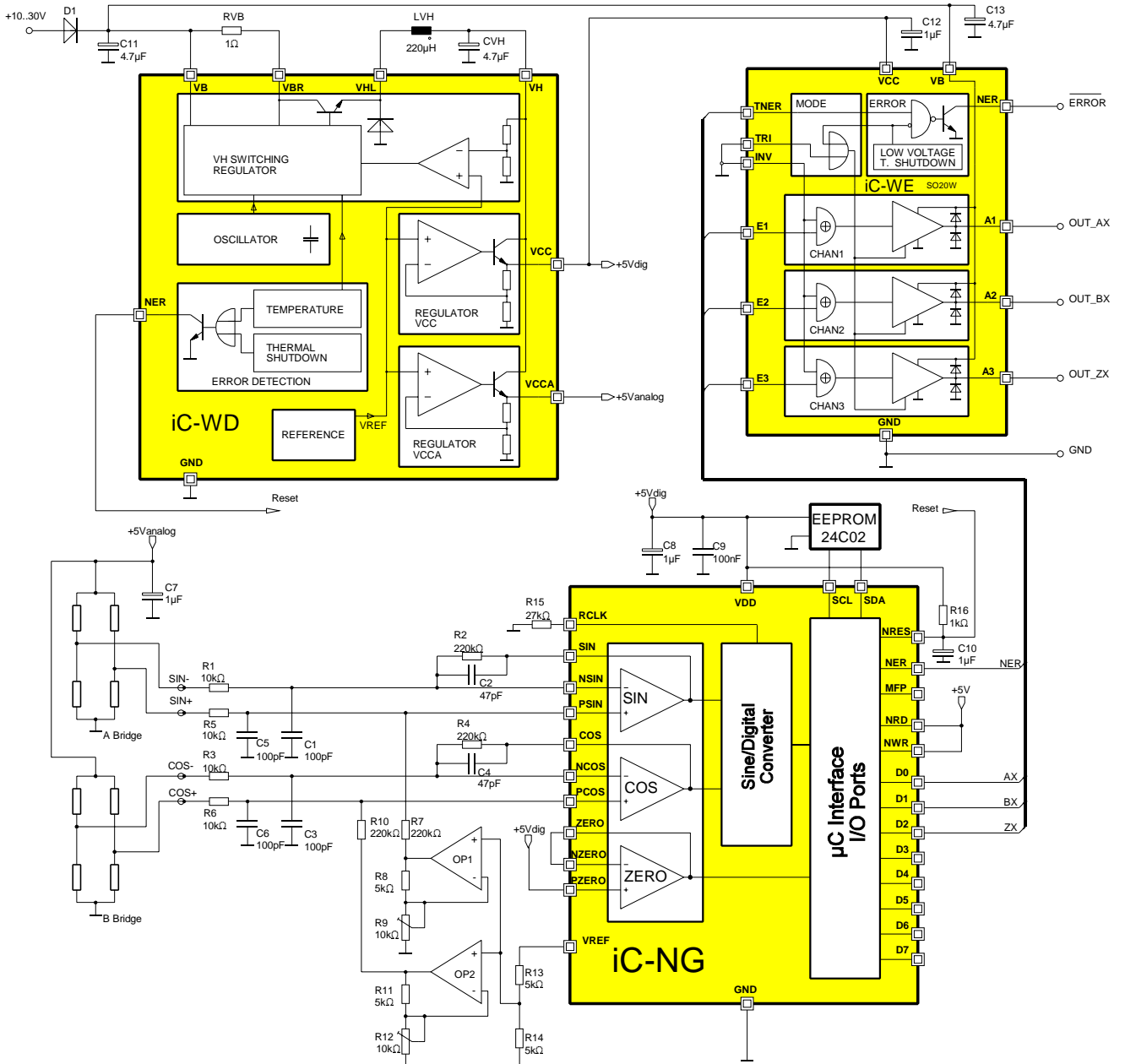
Fig. 7: MR sensor circuit with a line driver and 10−30V voltage supply.

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DEMO BOARD

An iC-NG demo board with an 8OC51 controller and insulated serial interface is available for test purposes. The package includes a partially-equipped circuit board, a 3.5" floppy disk with PC software (system requirements: processors from 80386, DOS 6.x, OS/2, Windows 3.11, Windows NT 3.51, Windows 95 and upwards), a lead for the serial interface and operating instructions.

Fig. 8: demo board circuit diagram.

Demo Board PCB

Fig. 9: iC-NG demo board, component side.

Demo board control program

The user interface depicts the iC's internal registers. By selecting the letters printed in bold in the input mask, individual registers can be directly accessed and altered. Data transfer to the demo board and to iC-NG runs in the background.

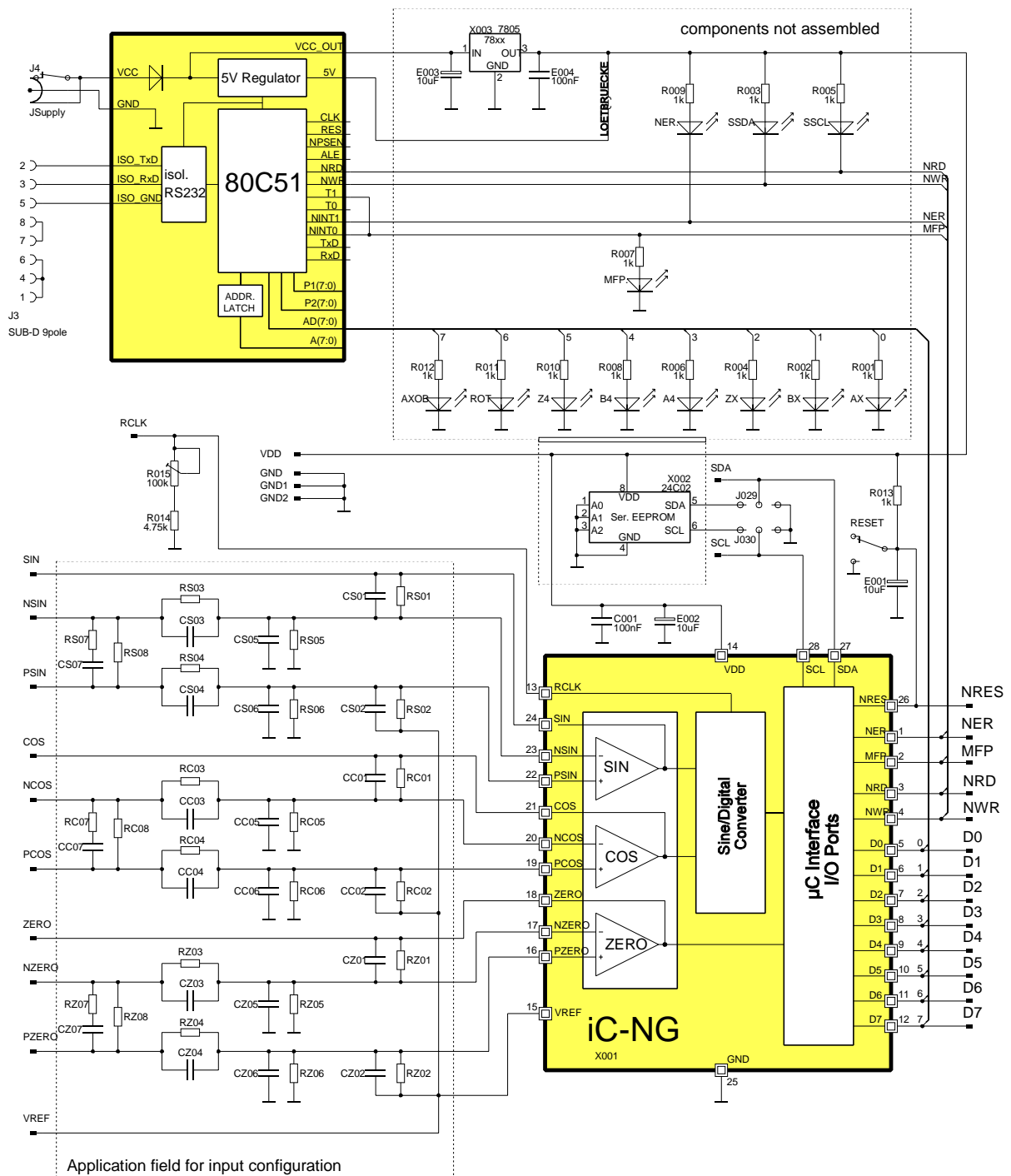Complete sets of data can be stored on floppy or hard disk and can be used to transfer information to EEPROM programming units, for example. Various special functions are also available; among other things, these permit the cyclic readout and on-screen display of certain iC-NG registers, the continuous measurement of pulses or segments, or the approximate, automatic determination of parameters which adapt the converter for distorted signals.

```
              iC-NG  Winkeldekodierer Sinus/Digital             V1.8
NG:00 00 00 3E  TPOS:00 00 00 00
AX:0  A4:I  NGUPDT :O,I  RES   :256    ROT   :O  SIC    :O  CSIN :12.0pF
BX:0  B4:I  POSKOMP:O,O  HYS   :R100%  ADAP  :O  SLCNTEN :O  CZERO:12.0pF
ZX:0  Z4:I  MAXFREQ:O,I  ZCONF :O      NGLJ  :O  COUNTEN :O  FREQ :O
AB:0  RO:I  STEPINP:O,O  OUTSEL:O      LATINT:O  CBZ    :O
TACHO:D7    ERRV  :O,O  ACCMOD:O       LATERR:O  CLC    :O
     G    O  Funktionsanpassung(FA)
SEG1  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG2  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG3  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG4  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG5  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG6  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG7  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
SEG8  -0   0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
           00  3E 00 00 00 FA D7 C0 1F 30 00 00 05 FF F8 F8 F8
           10  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           20  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           30  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           40  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           50  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           60  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           70  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
           80  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
 F1 HELP  F2 SAVE  F3 LOAD  F4 READ  F5 OREAD  F6 ADR  F7 PULS  F8 FIT  F10 QUIT
```

On-screen mask

GENERAL

Generating trigger signals
Option 1 (incremental mode)

Through external wiring, a zero signal can be preset (static) and the display at pin ZX/D2 influenced using relevant programming. To this end, the zero signal input is configured so that iC-NG contains "ZERO = 1". This is made possible by pin NZERO being connected to GND and by pin PZERO being connected to a higher potential, such as +5V, for example. Output ZERO remains open.

For each sine cycle, iC-NG now generates a zero pulse at ZX/D2 which can be used to trigger the oscilloscope. The position of the zero pulse can be programmed via ZCONF (address 9) and shifted in steps of 45°.

Generating trigger signals
Option 2 (parallel-absolute mode)

A trigger signal at pin MFP can be generated for any desired stage of interpolation by comparing the target marker of register TPOS with the NG output value.

To do so, the 32-bit output value and target position comparison are limited to the 8 bits of the interpolation steps (counter depth OUTSEL(1:0)= 00, address 9). The desired target position and trigger point are written under address 0 (TPOS 7:0, zero after a reset). Position comparison POSCOMP must be enabled (EN1= 1, address 11); the change in output value via NGUPDT the pin MFP would otherwise signal must be disabled (EN0= 0, address 11). Following this, pin MFP now issues a trigger signal each time the target position is reached.

Basic correlation between the resolution, input and output and necessary clock frequencies

The minimum clock frequency required is determined by the 2-fold input frequency multiplied by the internal resolution of the converter (high accuracy error).

We recommend that the clock frequency be set so that this is equivalent to the 8-fold value of the input frequency multiplied by the internal resolution of the converter, which of course depends on how high the permissible maximum error of rotation may be.

The maximum output frequency in parallel-absolute mode at port D0 and in incremental mode at port

D7/AXB is equivalent to half the clock frequency.

Attention must be paid to the fact that higher resolutions are used in special cases where RES(6:5) is not equal to "00".

Example 1: resolution of 200, 500Hz input signal fclk = 500Hz x 8 x 200 = ca. 800kHz. Taking the diagram for the oscillator frequency characteristic, R(RCLK) has ca. 47kΩ.

At 500Hz input frequency, the pulse frequencies for AX and BX are 25kHz and 50kHz for AXB.

This high clock frequency means that up to 100kHz pulse frequency are possible for AX and BX and 200kHz for AXB. Calculating backwards, the highest possible input frequency is thus 2kHz. If this frequency is exceeded, this is signalled at error message output NER (which must be enabled).

Example 2: resolution of 8, 100kHz input signal fclk = 100kHz x 8 x 8 = ca. 6.4MHz. Taking the diagram for the oscillator frequency characteristic, R(RCLK) has ca. 5kΩ, if 5MHz clock frequency are selected.

Output frequencies of up to 1.25MHz are possible for AX and BX. In this instance, the highest input frequency possible without an error message being generated is ca. 300kHz.

Notes
Clock frequencies which exceed 800kHz significantly increase the level of system noise (jitter). The (resistive) hysteresis appears to be reduced, pulse positions are shifted and come temporally slightly earlier. Capacitive hysteresis also reacts sensitively to system noise.

Despite this, the system still functions if very high clock frequencies of 3MHz, for example, are selected. AXB pulse frequencies of up to 800kHz are possible.

Higher signal amplitudes improve the output signal; 3Vss are recommended. Looping in the programmable gain amplifier (PGA) can influence the quality of the signal (address 8, ADAP= 1). If the converter adaptation function is used, the clock frequency should not be changed once the adaptation parameters have been set.

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Table for operating frequencies

Clock frequency fclk	800 kHz	1.6 MHz	3.2 MHz
Resistor R(RCLK) for clock oscillator	ca. 47 kΩ	ca. 27 kΩ	ca. 9 kΩ
Max. output frequency (an output change requires 2 clock pulses)	400 kHz	800 kHz	1.6 MHz
Max. AXB pulse frequency Max. AX resp. BX pulse frequency	200 kHz 100 kHz	400 kHz 200 kHz	800 kHz 400 kHz

RES 200			
Max. input frequency	2 kHz	4 kHz	8 kHz
Recommendations (4-fold over-sampling at fmax) max. input frequency resulting AXB pulse frequency (AXB shows 100 pulses) resulting AX resp. BX pulse frequency	< 500 Hz < 50 kHz < 25 kHz	< 1 kHz < 100 kHz < 50 kHz	< 2 kHz < 200 kHz < 100 kHz
Example: possible moving speed with a scale where the length of a cycle is 500 µm at a resolution of 2.5 µm	0.25 m/s < 1 m/s	0.5 m/s < 2 m/s	1 m/s < 4 m/s

RES 8			
Max. input frequency	50 kHz	100 kHz	200 kHz
Recommendations (4-fold over-sampling at fmax) max. input frequency	< 12.5 kHz	< 25 kHz	< 50 kHz

Period counter, **parallel or SSI output mode** (2 clock pulses per change required)			
Max. input frequency	200 kHz	400 kHz	800 kHz
Example: possible moving speed with a scale where the length of a cycle is 500 µm (resolution of 500 µm, resolution of 2.5 µm is valid with low speed only)	< 100 m/s	< 200 m/s	< 400 m/s

CORRECTING SIGNALS AND ADAPTING FUNCTIONS
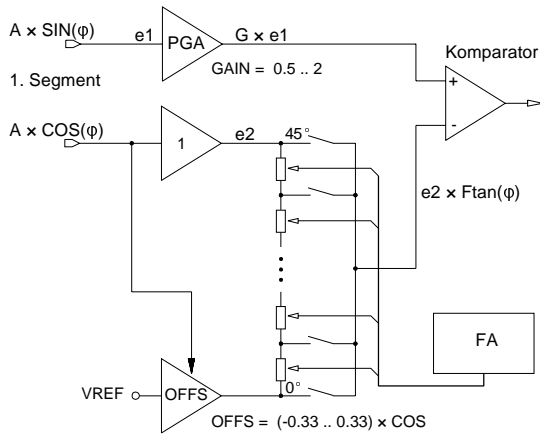
Fig. 10: schematic circuit diagram of the converter analog section.

Compensation possibilities

1. Different signal amplitudes for sine and cosine

The PGA permits various signal amplitudes to be compensated for. It is, however, prudent to compensate externally if it is not permissible to enlarge the dynamic error (settling times when changing segment).

2. Varying signal amplitudes

Varying signal amplitudes are automatically compensated for when the tangent is formed.

3. Signal-independent offset voltages

External compensation is essential. The iC-NG offset correction facility is only suitable for signals whose voltage at a zero crossing changes with the amplitude, as it is the case with phase-shifted signals.

4. Signal-dependent offset voltages

The programmable, amplitude-weighted zero crossing correction feature means amplitude-dependent offset voltages can be compensated for.

5. Phase errors

Phase errors, e.g. through inexact sensor placement, can be eliminated by the programmable compensation facility.

6. Signal distortion caused by harmonics

The iC-NG converter can also resolve distorted input signals without detriment to the converter's linearity via the programmable TAN-function adaptation feature. If the form of the signal is known, it is possible to predict the adaptation parameters, taking Fourier coefficients as a basis for calculation, for example.

Setting correction and adaptation parameters

Step 1: correcting the gain of the PGA and the offset.

Using gain setting G1, the signal at the end of the first segment is adapted to the cosine signal (sin45°= cos45°). Offset O1 is then set to G1 x e1 = sin(0°).
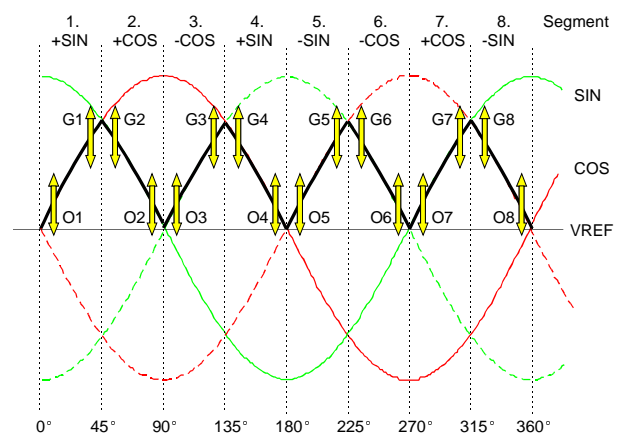

Fig. 11: effects of parameters OFFSET and GAIN.

A decisive factor for the sine-cosine intersections is the gain adaptation performed for the 1st + 2nd segments, 3rd + 4th segments, etc. Offset settings alone only affect intersections with the VREF reference voltage.

The following order of compensation is practical:
First gain, then offset.

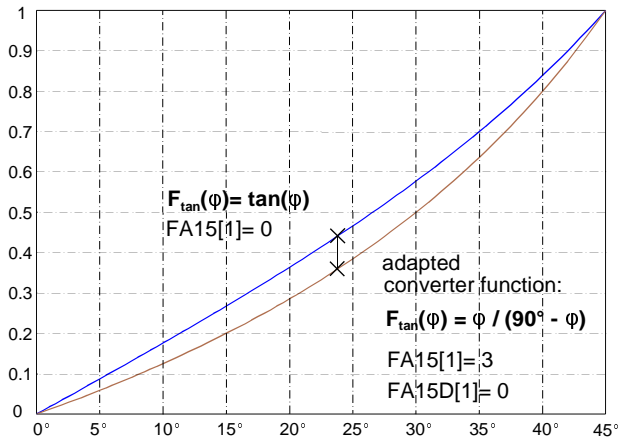**Step 2:** setting the transfer function of the TAN-D/A converter to the value of e_1/e_2 (e= input signal).

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Fig. 12: effect of parameters FA. Example for triangular input signals (1st segment).

In its basic setting (e_1 = sin, e_2 = cos), the PGA has a gain of one and an offset of zero. The tangent function is formed in the feedback loop. For non-sinusoidal signals, the transfer function can either be more sharply curved or straightened in the feedback loop (Fig. 12).

Adaptation of functions should be carried out for each of the eight segments separately.

Example: manual adaptation procedure

The following diagrams show the **first step of adaptation** in a correction process for adapting the converter, here for distorted input signals with an additional phase error.

The diagrams show the AXB output pulse train in incremental mode at a resolution of RES= 8, from which point compensation should be started. The various stages of resolution are represented by the eight edges of the 4 pulses; each edge can be individually positioned by correcting the offset and gain.
Emulating incremental mode in parallel-absolute mode by performing a cyclic readout of address 4 (output D7/AXB) is favorable to iterative compensation.
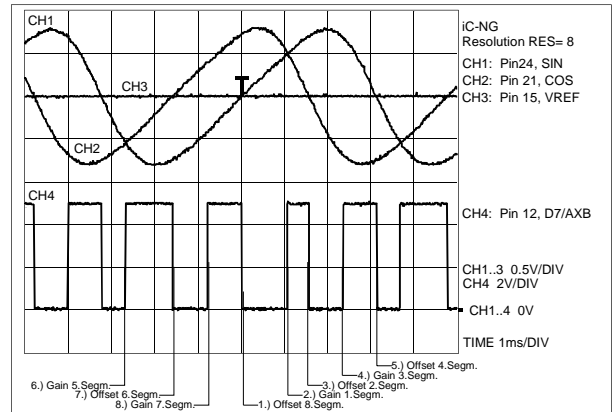
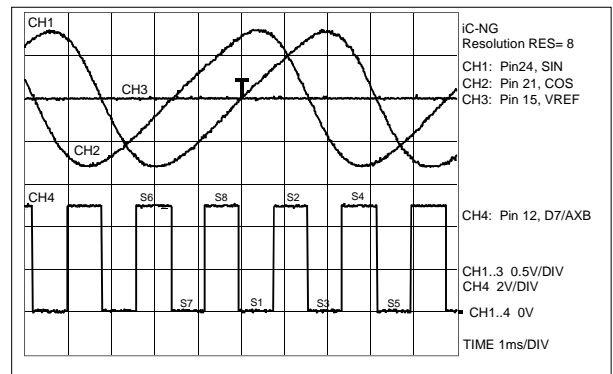Fig. 13: the 8 steps of compensation in clockwise operation.

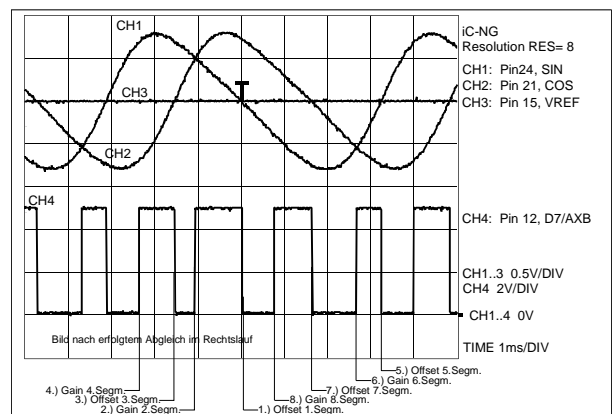Fig. 14: output signal following compensation (clockwise). S1..8 index the compensated segments.

Fig. 15: the 8 steps of compensation in counter-clockwise operation. The output signal shown here has been compensated in clockwise operation already.
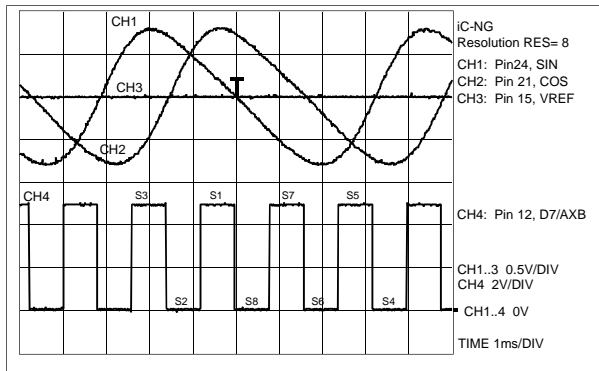
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Fig. 16: output following compensation (counter-clockwise).

Fine tuning at higher resolutions can be performed once the clockwise and counterclockwise steps of compensation have been completed. In doing so, it is important that the input frequency is low to avoid false settings being made due to dynamic errors.

Incorrectly positioned segment junctions can be adjusted clockwise by offset 1, 3, 5, 7 and by gain 2, 4, 6, 8. The sequence is discretionary.

If the input signal requires, the transfer function of the TAN-D/A converter can be adapted by way of detuning in the **second step of adaptation**. The signal forms given in this example would also require that this second stage of adaptation be carried out.

Example: calculating adaptation parameters offset and gain using approximation formulae.

In the following example, we assume that the amplitude and offset values for the sine and cosine input signals are known and that the phase shift is free from error.

Formulation:

$$SIN() = As \cdot Fsin(\varphi + \varphi_{serr}) + Os$$

$$COS() = Ac \cdot Fcos(\varphi + \varphi_{cerr}) + Oc$$

SIN()	Sine input signal at angle φ
As	Sine amplitude
Fsin	Sine-similar function
Os	Sine offset
φ_{serr}	Sine phase error
COS()	Cosine input signal at angle φ
Ac	Cosine amplitude
Fcos	Cosine-similar function
Oc	Cosine offset
φ_{cerr}	Cosine phase error

Simplifications:

$\varphi_{serr} = \varphi_{serr} = 0$, Fsin()= sin(), Fcos()= cos()

Formulation for the offset of segment 1:

$$COS(\varphi=0) \cdot O1 = G1 \cdot SIN(\varphi=0)$$

$$O1 = \frac{G1 \cdot SIN(\varphi=0)}{COS(\varphi=0)} = \frac{G1 \cdot (As \cdot 0 + Os)}{Ac \cdot 1 + Oc} = \frac{G1 \cdot Os}{Ac + Oc}$$

Formulation for the gain of segment 1:

$$G1 \cdot SIN(\varphi=45°) = COS(\varphi=45°)$$

$$G1 = \frac{COS(\varphi=45°)}{SIN(\varphi=45°)} \approx \frac{\dfrac{Ac}{\sqrt{2}} + Oc}{\dfrac{As}{\sqrt{2}} + Os} = \frac{Ac + \sqrt{2} \cdot Oc}{As + \sqrt{2} \cdot Os} \approx \frac{Ac}{As}$$

The resulting approximation formulae for the individual segments are collated on the following page.

| Segment	Gain	Offset
1	$\dfrac{Ac + \sqrt{2}\cdot Oc}{As + \sqrt{2}\cdot Os}$	$-384 \cdot G1 \cdot \dfrac{Os}{Ac + Oc}$
2	$\dfrac{As + \sqrt{2}\cdot Os}{Ac + \sqrt{2}\cdot Oc} = \dfrac{1}{G1}$	$-384 \cdot G2 \cdot \dfrac{Oc}{As + Os}$
3	$\dfrac{As + \sqrt{2}\cdot Os}{Ac - \sqrt{2}\cdot Oc}$	$384 \cdot G3 \cdot \dfrac{Oc}{As + Os}$
4	$\dfrac{Ac - \sqrt{2}\cdot Oc}{As + \sqrt{2}\cdot Os} = \dfrac{1}{G3}$	$-384 \cdot G4 \cdot \dfrac{Os}{Ac - Oc}$
5	$\dfrac{Ac - \sqrt{2}\cdot Oc}{As - \sqrt{2}\cdot Os}$	$384 \cdot G5 \cdot \dfrac{Os}{Ac - Oc}$
6	$\dfrac{As - \sqrt{2}\cdot Os}{Ac - \sqrt{2}\cdot Oc} = \dfrac{1}{G5}$	$384 \cdot G6 \cdot \dfrac{Oc}{As - Os}$
7	$\dfrac{As - \sqrt{2}\cdot Os}{Ac + \sqrt{2}\cdot Oc}$	$-384 \cdot G7 \cdot \dfrac{Oc}{As - Os}$
8	$\dfrac{Ac + \sqrt{2}\cdot Oc}{As - \sqrt{2}\cdot Os} = \dfrac{1}{G7}$	$384 \cdot G8 \cdot \dfrac{Os}{Ac + Oc}$

The following values must be programmed into the adaptation registers:

Gain = 255 - G * 128   , when G > 1
Gain = G * 255   , when G <= 1

Offset = 255 - O   , when O >= 0
Offset = 127 + O   , when O < 0

Examples: adapting the converter to real sensor signals
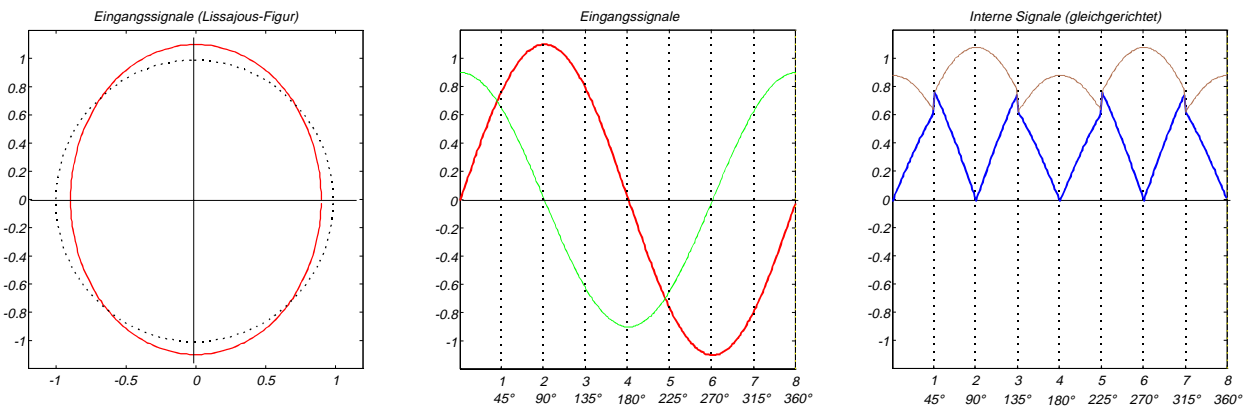
Ideal sine/cosine input signals
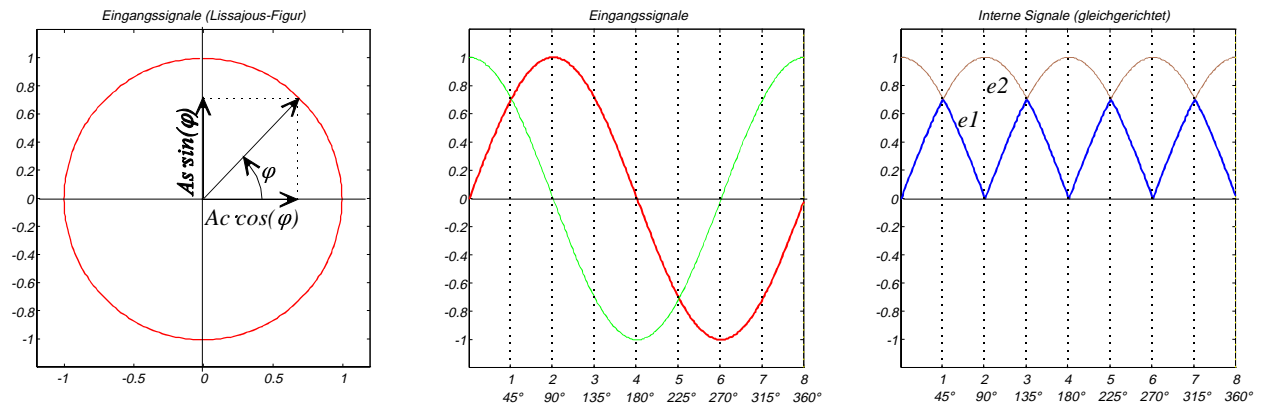
$$G = [1.0000 \quad 1.0000 \quad 1.0000 \quad 1.0000 \quad 1.0000 \quad 1.0000 \quad 1.0000 \quad 1.0000]$$
$$O = [0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000]$$
$$FA() = 0$$

Fig. 17: ideal sine/cosine input signals (Fsin= sin, Fcos= cos, As= Ac, Os= Oc= 0, φ_{serr}= φ_{cerr}= 0)
It is not necessary to alter the GAIN, OFFSET and FA parameters.

As= 1.1, Ac= 0.9

$$G = [0.8182 \quad 1.2222 \quad 1.2222 \quad 0.8182 \quad 0.8182 \quad 1.2222 \quad 1.2222 \quad 0.8182]$$
$$O = [0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000 \quad 0.0000]$$
$$FA() = tbd.$$

Fig. 18: input signals with amplitude errors. The FA parameters should also be adapted, especially when resolutions of higher than RES= 8 are used.

The adaptation of the gain necessary at the junction from 1st to 2nd segment, from 3rd to 4th segment, etc. leads to alterations in the pulse width of the interpolation steps (see signal AXB) which follow a changeover of segment, especially at higher input frequencies. This dynamic error is caused by settling times and becomes more noticeable the larger the differences in gain are. Vice versa, it follows that good sine/cosine sensor signals also generate considerably better incremental converter output signals.
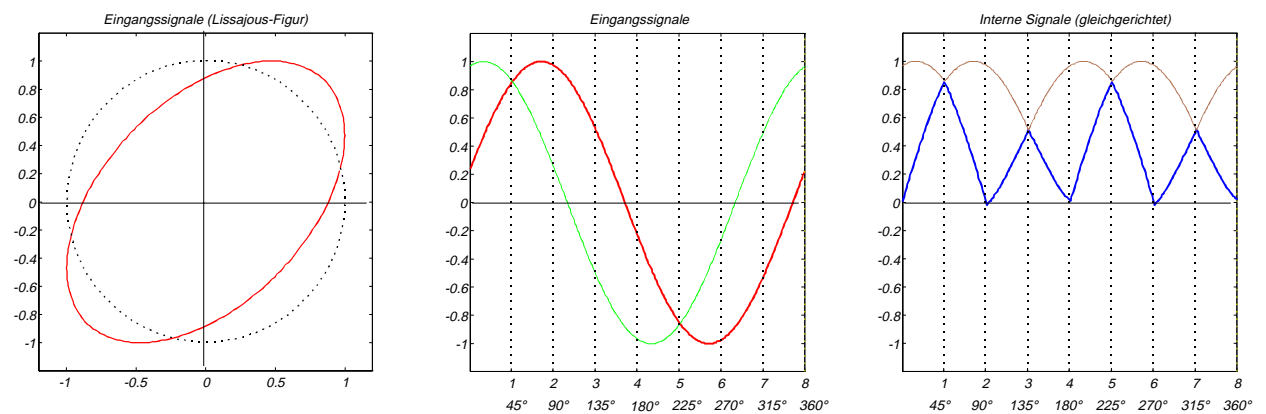
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Os= +0.1, Oc= -0.1

Eingangssignale (Lissajous-Figur)	Eingangssignale	Interne Signale (gleichgerichtet)
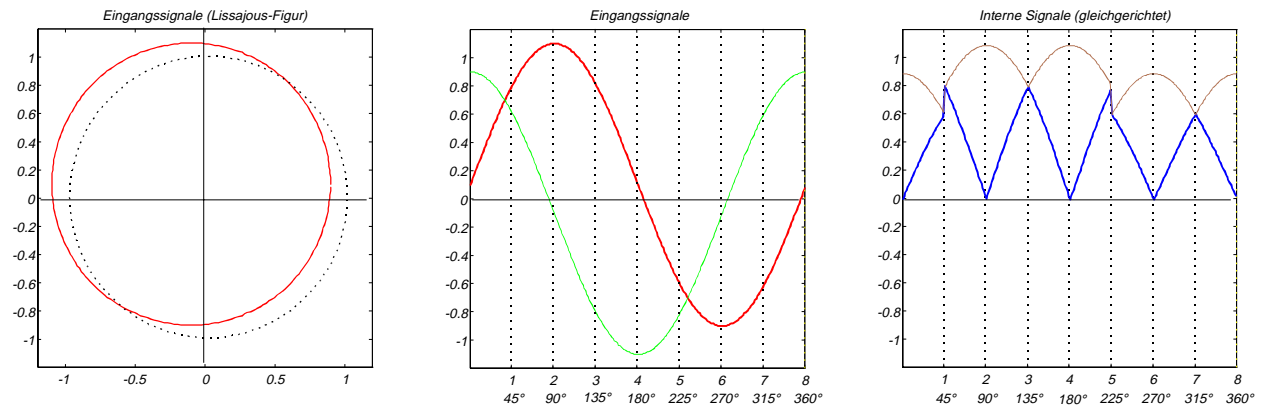
G = [0.7522   1.3294   1.0000   1.0000   1.3294   0.7522   1.0000   1.0000]
O = [0.0836   -0.1209   0.0909   0.0909   -0.1209   0.0836   -0.1111   -0.1111]
FA()= tbd.

Fig. 19: input signals with offset errors.

φ serr= +15°, φ cerr= -15°

Eingangssignale (Lissajous-Figur)	Eingangssignale	Interne Signale (gleichgerichtet)

G = [1.0000   1.0000   1.0000   1.0000   1.0000   1.0000   1.0000   1.0000]
O = [0.2505   0.2505   -0.2505   -0.2505   0.2505   0.2505   -0.2505   -0.2505]
FA()= tbd.

Fig. 20: input signals with phase errors.

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Signals with superimposed harmonics
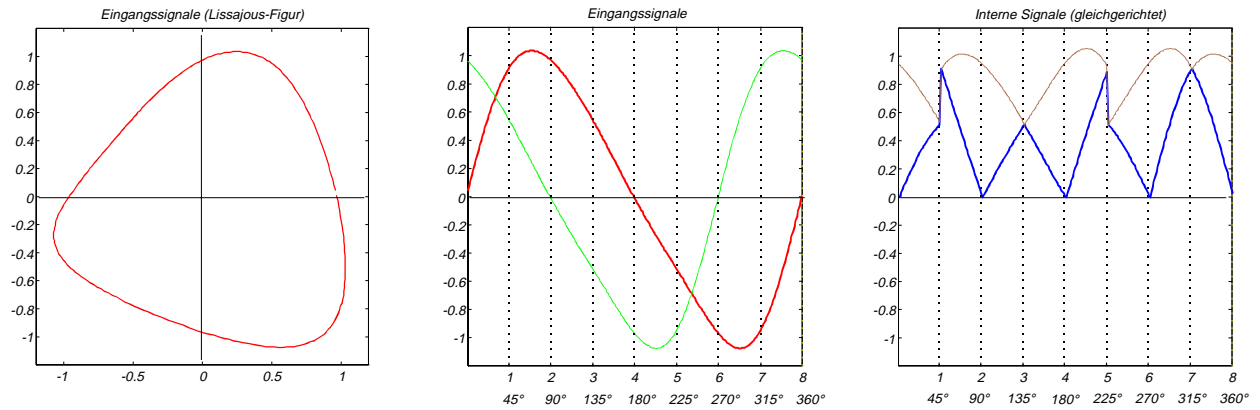
$Fsin()= 1*sin(\varphi) + 0.2*sin(2*\varphi) + 0.03*sin(3*\varphi) + 0.015*cos(\varphi) + 0.01*cos(2*\varphi) + 0.02*cos(3*\varphi)$
$Fcos()= 1*cos(\varphi) + 0.2*cos(2*\varphi) + 0.03*cos(3*\varphi) + 0.015*sin(\varphi) + 0.01*sin(2*\varphi) + 0.02*sin(3*\varphi)$

$G = [0.5751 \quad 1.7388 \quad 1.0135 \quad 0.9867 \quad 1.7757 \quad 0.5632 \quad 1.0076 \quad 0.9924]$
$O = [0.0270 \quad -0.0453 \quad 0.0264 \quad -0.0252 \quad 0.0453 \quad -0.0259 \quad 0.0463 \quad -0.0465]$
$FA()= tbd.$

Fig. 21: input signals with superimposed harmonics.

An algorithm for predicting adaptation parameters can be provided on request. Methods of calculation can also be used to check if the setup ranges of the adaptation parameters are sufficient for a given sensor signal. If no formula is available for the sensor signals, sampled oscilloscope signals can also be taken as a basis for calculation.