ICmic
IC MICROSYSTEMS

APPLICATION NOTES
AN002

ICmic DIGITAL TO ANALOG CONVERTER (DAC) GLOSSARY

Shahab A. Najmi

DAISY-CHAIN

It is a configuration in which the serial data output of one devices is connected to the serial data input of the next device. This allows several devices to be addressed simultaneously by only one data line.

DNL (DIFFERENTIAL NON-LINEARITY)

In a DAC, the Differential Non-linearity measures the deviation from the ideal case of 1 LSB transitions in the analog output value. An ideal DAC has a DNL of zero. It is measured in units of Least Significant Bits (LSB).

EXT/INT REFERENCE DAC

It is the type of DAC in which either external or internal reference voltage source can be used.

The internal reference ($V_{ref,int}$) is an accurate reference built on the chip which can be used for accurate conversion if no external reference is used. (Output = (G^* x D / 2^n) x $V_{ref,int}$)

External voltage reference (V_{ref}) can be used so that the output of DAC would swing from 0 to (G^* x V_{ref}) depending upon the input code provided. (* G depends upon the device)

GAIN ADJUST DAC

It is the type of DAC in which the gain of the output amplifier of the DAC can be adjusted. Thus the DAC can be configured to have different output gains using either internal or external reference. The output voltage would be given by ((V_{ref} x D / 2^n) x Gain) where the gain is set by the value of the external resistors connected to the output and the gain adjust pin.

GAIN ERROR

Gain Error indicates how well the slope of the output transfer function compares with the slope of the ideal transfer function. It is typically expressed as a percentage of the Full scale range (% of FS) and is usually measured at full-scale.

INL (INTEGRAL NON-LINEARITY)

In a Digital to Analog Converter INL is the deviation at any given code from the ideal transfer function. It can also be measured by taking the sum of the differential non-linearities from the lowest value to the given step. It is measured in units of Least Significant Bits (LSB).

MONOTONIC

A DAC is said to be monotonic if for every increase in the input code the output always increases.

OFFSET ADJUST

The output amplifier typically has some offset due to non-idealities. This can be adjusted externally to cancel the effect of those non-idealities to cater to the particular application to provide an accurate output in the region of interest. This is called offset adjustment.

OFFSET ERROR

Offset Error indicates how well the actual analog output of the DAC matches with the ideal output at zero scale.

RAIL-TO-RAIL

The output can swing from the maximum voltage on the chip (e.g. Vdd) to the minimum voltage (e.g. Ground). This behavior is called Rail-to-Rail output swing.

SETTLING TIME

It is the amount of time that the output of the DAC takes to change its value from the current output to the new output value once it is instructed to change the output. On the datasheet it is usually specified for a full-scale transition from GND to full-scale. (Some manufacturers specify quarter-scale transition settling time which is typically much less than full-scale settling times figure).

SHUTDOWN MODE DAC

Shutdown modes are used for power saving when the converter output is not being used. This type of DAC can have many different programmable output modes. User can program the output to have high impendence, terminated with 1 k-ohm or 10 k-ohm resistance etc. depending upon the requirement of the particular application.

SLEW RATE

It is the measure of the maximum rate that the output of the DAC can change. It is typically limited by the slew rate of the output amplifiers of the DAC.

PROTOCOLS

Microwire is a simple three wire serial communication interface. The three wires are the serial clock (SCLK), serial data out (MISO) and serial data in (MOSI). The data is shifted in on the rising edge of the clock and is shifted out on the negative edge of clock. The clock in this protocol has a fixed polarity and phase.

SPI (Serial Peripheral Interface) is a newer version of the Microwire protocol. The clock polarity and phase can be configured giving four distinct combinations allowing the SPI to communicate with protocols like microwire and microwire/plus (slight variation of microwire). All other operations are similar to microwire protocol.

QSPI (Queued Serial Peripheral Interface) is an abstraction layer above the basic SPI hardware specification. Allows interrupt driven buffered I/O for the Motorola SPI between IC level components

Contact Information

For any other questions / queries please feel free to contact us at support@icmic.com or contact us at the following address.

IC MICROSYSTEMS Sdn. Bhd.
Suite S06, 2320 Century Square,
63000 Cyberjaya, Selangor D.E.,
Malaysia
Tel: (603) 8319 1919
Fax: (603) 8319 1918

Disclaimer

IC MICRSOYSTEMS (ICmic) reserve the right to make corrections, modifications or changes to any of its products and services at any time and to discontinue any of its product or service without notice.

The information in this document is believed to be accurate and correct. However ICmic does not assume any liability for any loss or damage caused to any party due to the usage of the information in this document. Contents of this document are not to be released to any third party without written consent of the owner.

