Application Note

ODT (On-Die Termination) function of QUADP/DDR-IIP SRAM

Introduction:

Signal integrity is critical for high speed applications. Electrical signals are reflected back when they reach the end of a transmission line. Those reflections cause noise, which adversely affects signal integrity. One way to reduce reflections is to properly terminate signals. On-die termination (ODT) is an effective signal termination scheme that embeds the termination resistors on the die.

Basic ODT Concept:

A basic ODT resistive termination scheme consists of a symmetrical pull-up and pull-down circuit between V_{DDQ} and V_{SS}, and the real termination values are calculated by a Thevenin-Equivalent, as depicted in Figure 1 below.

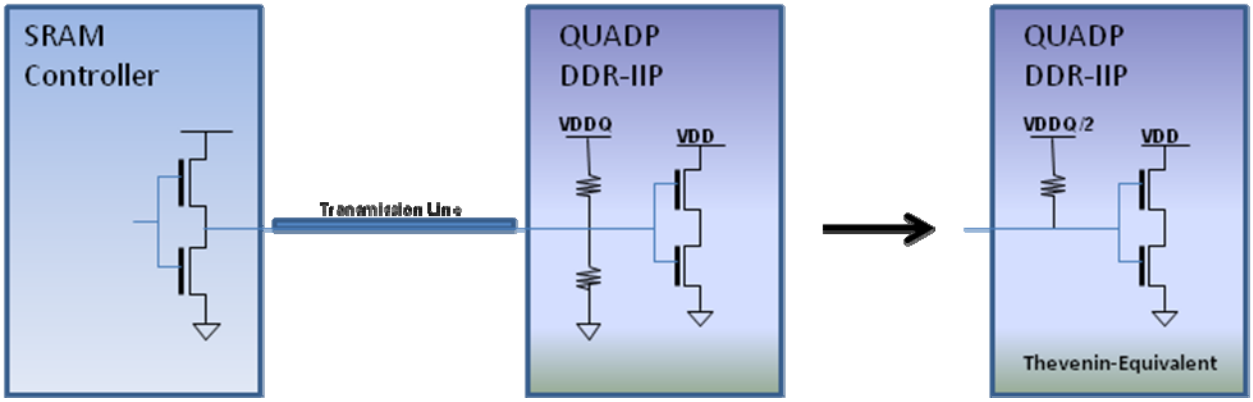


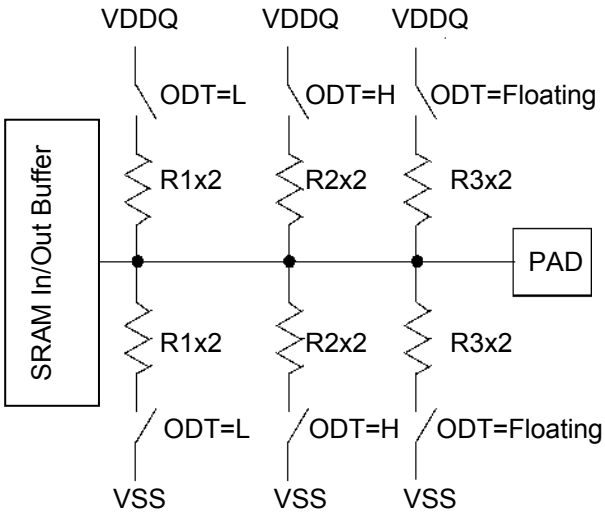
Figure1. ODT interface between SRAM controller and QUADP/DDR-IIP

ODT Options of QUADP/DDR-IIP:

ISSI's QUADP and DDR-IIP products feature three types of resistive controls for the pull up and pull down termination, which allows an SRAM to turn on/off termination resistance for the pins that have ODT. The ODT pin can have three values: High, Low, or Floating, and each of these values allows for different ODT termination impedance (a certain percentage of RQ as seen in Figure 2). With DDR-IIP devices, which have a common I/O bus, ODT is automatically enabled during Writes to the SRAM and is disabled during SRAM Read operations. With QUADP devices, which have a separate I/O bus, ODT is always enabled during Writes and Reads to the SRAM. Each option is distinguished by the ISSI device top mark.

Example) 72M QUADP Products

IS61QDPB42M36**A** : No ODT
IS61QDPB42M36**A1** : ODT Option 1
IS61QDPB42M36**A2** : ODT Option 2



	R1	R2	R3
Option1[3]	0.3x RQ[1]	0.6x RQ[2]	0.6x RQ[2]
Option2[4]	ODT disable	0.6x RQ[2]	ODT disable

Figure2. Functional representation of ODT

Notes
1. Allowable range of RQ to guarantee impedance matching to a tolerance of ±20% is 175Ω<RQ<350Ω.
2. Allowable range of RQ to guarantee impedance matching to a tolerance of ±20% is 175Ω<RQ<250Ω.
3. ODT control pin is connected to VDDQ through 3.5kΩ. Therefore it is recommended to connect it to VSS through less than 100Ω to make it low.
4. ODT control pin is connected to VSS through 3.5kΩ. Therefore it is recommended to connect it to VDDQ through less than 100Ω to make it high.

ODT PIN

1) ODT Pin in Option 1

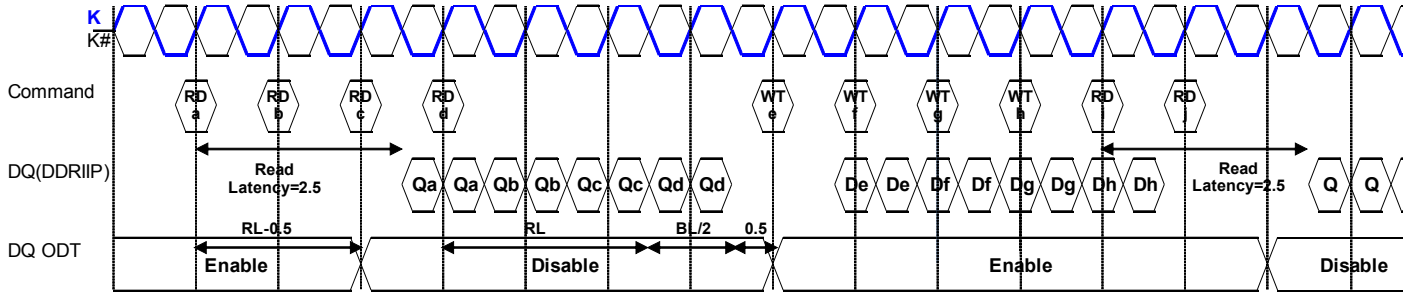
ODT for K, K#, BWx#, and Ds in QUADP products are always ON.

ODT for DQs in common I/O device will be on and off depending on the status. Read commands turn ODT off as follows:

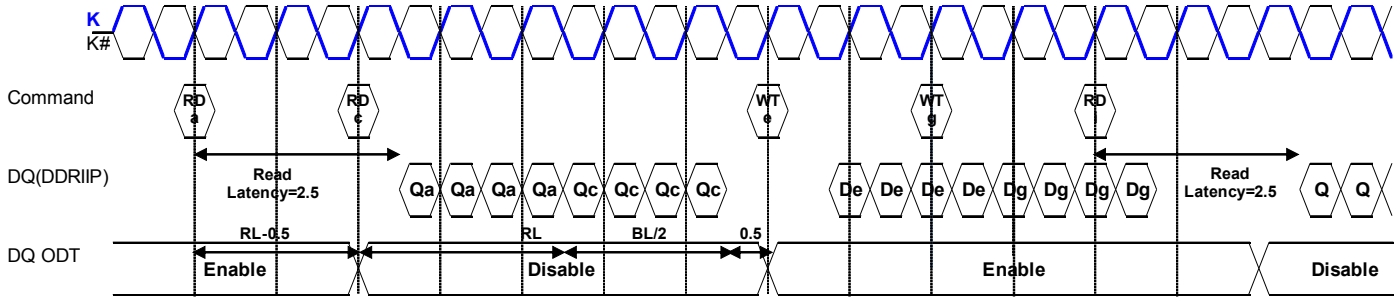
Off: First Read Command + Read Latency - 0.5 cycle

On: Last Read Command + Read Latency + BL/2 cycle + 0.5 cycle (See the timing chart below)

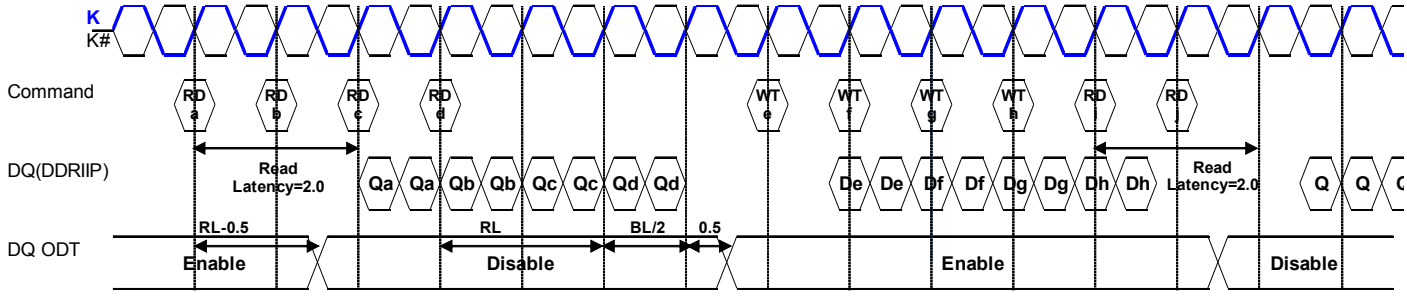
Example1) BL=2, RL(Read Latency=2.5)



Example2) BL=4, RL(Read Latency=2.5)



Example3) BL=2, RL(Read Latency=2.0)



2) ODT Pin in Option 2

The same ODT rules as option1 apply except for K and K# which are always OFF in Option 2.

ISSI QUADP and DDR-IIP ODT Options:

ODT Option	ODT Condition	ISSI Top Mark	Notes
ODT OFF	No ODT resistor	A	
ODT Option1	RQ1x0.3(ODT=L)	A1	1
	RQ2x0.6(ODT=H)	A1	2
	RQ2x0.6(ODT=Floating)	A1	
ODT Option2	Disable(ODT=L)	A2	
	RQ2x0.6(ODT=H)	A2	2
	Disable(ODT=Floating)	A2	

1. RQ1 (Input Strong): ODT is forced to low input voltage and RQ Range is 175Ω<RQ<350Ω
2. RQ2 (Input Weak) : ODT is forced to high input voltage and RQ Range is 175Ω<RQ<250Ω