

## **C-to-FPGA Tools Enabled for the Intel® Front Side Bus Accelerate Xeon® Processor Applications**

*Impulse C™ allows software programmers to quickly develop FPGA-accelerated high performance computing applications*

**Kirkland Washington – September 18, 2007 2:00 PM PST** Impulse Accelerated Technologies Inc. today announced integrated support for new FSB enabled Xeon/FPGA processor development systems.

In related announcements made at the Intel Developers Forum today, hardware platform manufacturers have announced the release of accelerator modules, development boards and complete systems that combine FPGAs with Intel processors using the Intel Front Side Bus. These new systems represent integrated platforms on which processing can be accelerated through increased algorithm parallelism and high throughput from the host Intel processor and the FPGA accelerator. Impulse C enables these systems by allowing C-language applications to be partitioned between hardware and software, with processor-to-FPGA I/O generated automatically by the compiler.

When used to the their fullest potential, FPGA-accelerated systems allow performance-critical sections of an application to be off loaded to the FPGA accelerator, accelerating overall system performance from 2X to 10X. For scalable high performance computing algorithms, processing acceleration of 100X or greater is possible.

The key to fully exploiting these new platforms is a common programming language and a coherent tool flow. The vast majority of FPGA applications are still programmed using low-level hardware design languages such as VHDL and Verilog. While these methods are well established for hardware-oriented applications, C-language is a more natural environment for software application development. Impulse C provides a means for software programmers to more quickly take advantage of FPGA acceleration, while also providing control and visibility over FPGA hardware optimization.

Impulse C provides a C-based programming paradigm that provides:

- C as a design language for FPGA-accelerated applications.
- Iterative optimization of C code to increase parallelism, including pipeline generation and analysis.
- Automation of software-to-hardware interconnects, using platform-portable APIs.
- Integration and compatibility with standard C tools and with common FPGA development tools.

“Software engineers considering FPGAs for acceleration require intelligent tools,” stated Ralph Bodenner, Director of Product Development at Impulse. “Writing low-level hardware drivers to access FPGA memory, for example, or worrying about cycle-by-cycle behaviors in the FPGA hardware is unacceptable. The primary goal with the Impulse C tools is to raise the level of design abstraction and make FPGA programming a software design experience.”

The Impulse C tool flow for Xeon/FPGA co-development includes the use of standard software profiling and debugging tools for C application development. Impulse C then extends these standard tools to include C-to-FPGA compilation, as well as providing a C-compatible library of FPGA-specific functions useful for partitioning and parallelizing C code. The Impulse C compiler interfaces directly to FPGA synthesis tools via generated hardware description language files. Impulse also provides "First Design Optimization" services as well as training to help bring software engineers into the hardware world with minimum frustration.

The Impulse C compiler allows application developers to rapidly experiment with FPGA-accelerated algorithms, using familiar C-language programming techniques. By using the FPGA as a highly parallel coprocessor, applications that include financial modeling, scientific computing, bioinformatics and defense can be quickly developed, optimized and deployed.

### About Impulse

Impulse C allows software and hardware engineers to rapidly and cost-effectively move designs originating in ANSI C to FPGA coprocessors. For more information on Impulse C to FPGA software, visit [www.ImpulseC.com](http://www.ImpulseC.com).

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