Impulse Ready-to-Run Example

Accelerating a Complex FIR Filter on a Xilinx ML501 Board

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Overview

This ready-to-run example demonstrates how to use Impulse C to create an accelerated DSP application using a Xilinx ML501 development board, the Xilinx EDK tools and the embedded MicroBlaze processor. The methods used in this example can be applied to many similar MicroBlaze-based DSP applications.

This example assumes some knowledge of the Xilinx EDK tools. For a detailed description of how to use Impulse C with the Xilinx EDK tools and the MicroBlaze processor, please see the following tutorial:

http://www.impulsec.com/xilinx/MB_Tutorial_FIR/index.html

Example Notes

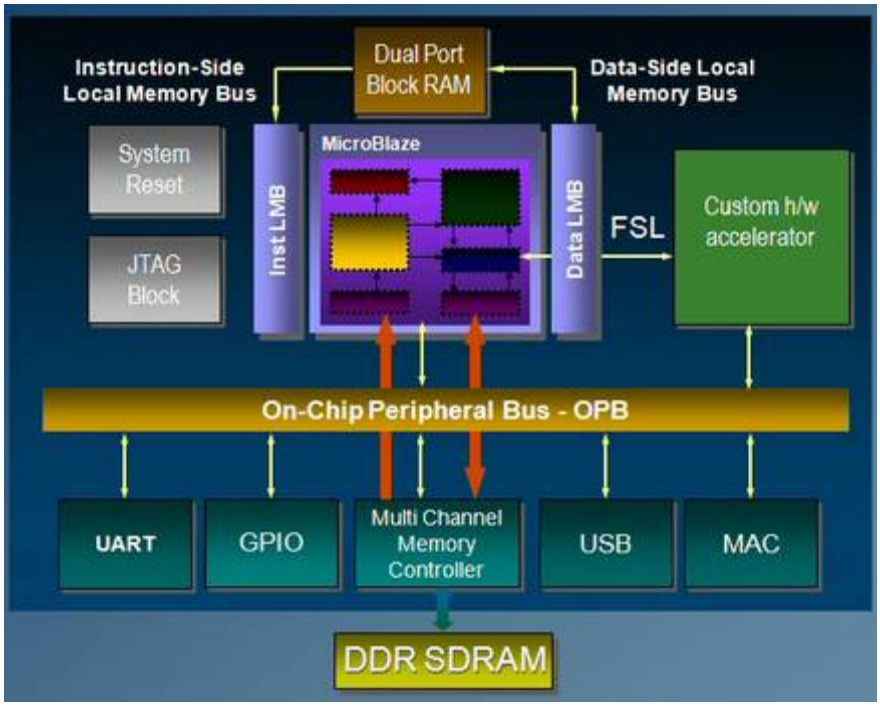
Impulse C can be used to generate hardware modules that are directly connected to an embedded processor (such as the Xilinx MicroBlaze) or to other hardware elements that may have been described using other design tools or techniques. The Impulse C programming model emphasizes the use of data streams, signals, and shared memories for process-to-process communication. These interfaces can be used to connect Impulse C processes to a wide variety of hardware devices and processors.

For embedded processors such as MicroBlaze, there are multiple possible ways to provide communication between a software application running on the processor, and a hardware accelerator running in the FPGA fabric. These include (among others):

- Using the OPB or PLB to create an Impulse C peripheral on a shared bus
- Using the FSL (Fast Simplex Link) to create a high-speed data stream
- Using shared memory

This example demonstrates a streaming application.

See the following simplified block diagram:



In this example, a software application running on the MicroBlaze communicates with the hardware FIR filter using Impulse C API functions/macros, which are implemented by the Impulse C compiler using FSL.

Project Files and EDK Settings

ZIP File Directory Structure

ComplexFIR_ML501.PDF	(This document)
ComplexFIR_ML501_ImpulseC/	(Impulse C project source files)
ComplexFIR_ML501_EDK/	(Pre-built EDK project)

Hardware Platform

Xilinx ML501 development board

Software Versions

Impulse CoDeveloper Version 2.20
Xilinx ISE Version 9.2
Xilinx EDK Version 9.2

Impulse C Platform Support Package

Xilinx MicroBlaze FSL

Xilinx EDK Base System Builder Settings

Board name: ML501
Processor: MicroBlaze
Reference clock frequency: 100 MHz

Processor_Bus clock frequency: 100 MHz
Local memory (BRAM): 8 KB
IO Devices:
    RS232_Uart 9600-8-None
    SRAM
Peripherals:
    XPS TIMER 32 bit one timer
STDIN: RS232_uart
STDOUT: RS232_Uart
Boot Memory: ilmb_cntlr

Note: EDK 9.2i uses a clock generator instead of DCMs. You must therefore add a clock output in the clock generator with a frequency of 50000000 Hz.

Downloading the Bitmap

The *download.bit* file can be downloaded to the FPGA using iMPACT.

XMD Commands For Execution

```
dow ComplexFIR/executable.elf
con 0x84100000
```