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Impulse Adds Support for Virtex 4 FX FPGAs to its CoDeveloper™ C-to-Hardware Tool

Tool allows fast creation of FPGA hardware accelerators from C-language

Kirkland, WA – July 12, 2005 – Impulse Accelerated Technologies™ today announced support for Xilinx Virtex-4 FX FPGAs in the latest release of its CoDeveloper C-to-hardware tools. The CoDeveloper Version 2 update adds significant new capabilities that specifically target Xilinx Virtex-4 platforms, including the automatic generation of PowerPC hardware interfaces.

With the Virtex-4 FX family of devices, Xilinx has provided a unique and powerful Auxiliary Processor Unit (APU) controller that provides direct access to hardware accelerators from instructions executing in software on the embedded IBM™ PowerPC™ 405 CPU. Impulse CoDeveloper enhances this programming of this platform by providing C-to-hardware tools that generate APU peripherals directly accessible from the PowerPC. Using this approach to hardware/software partitioning, speedups of up to 146X have been demonstrated for computationally-intensive PowerPC applications.

“The Xilinx Virtex-4 provides an ideal platform for hardware acceleration of embedded applications,” stated David Pellerin, co-founder and CTO of Impulse. “Adding support for the Virtex-4 in CoDeveloper has made it much easier for FPGA users to create hardware-accelerated functions from C-language descriptions.”

CoDeveloper gives software programmers access to FPGAs by allowing hardware accelerators to be compiled directly from C software descriptions. These accelerators are automatically compiled into efficient, high-performance hardware that can be mapped directly into FPGA gates. In the case of the Virtex-4, Impulse C is also capable of generating the required software/hardware interfaces using the Auxiliary Processing Unit (APU). The generated interfaces and other support files may be exported directly from CoDeveloper into the Xilinx Platform Studio™ tools for mapping into the selected Virtex-4 device.

Impulse C allows FPGA algorithms to be developed and debugged using popular C and C++ development environments including Microsoft Visual Studio™ and gcc-based tools. The CoDeveloper software-to-hardware compiler translates specific C-language subroutines to low-level FPGA-hardware while optimizing the generated logic and identifying opportunities for parallelism. The compiler is also capable of unrolling loops and generating loop pipelines to exploit the extreme levels of parallelism possible in an FPGA. Instrumentation and monitoring functions generate debugging visualizations for highly-parallel, multi-process applications, helping system designers identify dataflow bottlenecks and other areas for acceleration.

About Impulse

Founded in 2002, Impulse provides design tools that enable true software programming of FPGA devices using the C language. The Impulse CoDeveloper tools allow FPGA algorithms to be developed and debugged using popular C/C++ development environments, including Microsoft Visual Studio™ and GCC-based tools. The CoDeveloper software-to-hardware compiler translates C-language processes to low-level FPGA-hardware, while optimizing the generated logic and identifying opportunities for parallelism. The compiler analyzes untimed C code and collapses multiple C statements and operations into single-clock instruction stages. CoDeveloper unrolls loops and generates loop pipelines to exploit the extreme levels of parallelism possible in an FPGA. CoDeveloper's Application Monitor™ generates debugging visualizations for highly-parallel, multi-process applications, helping system designers identify dataflow bottlenecks and other areas for acceleration.

Pricing and Availability

Impulse CoDeveloper for Xilinx Virtex-4 is available now, with prices starting at from \$4,995 for a perpetual, single-user license. Annual and floating licenses are also available. 30-day evaluations are free to qualified organizations and individuals. Visit www.ImpulseC.com for more information or contact info@ImpulseC.com.

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Available Graphics

Impulse Logo

CoDeveloper Virtex-4 Design Flow Diagram

CoDeveloper Version 2 Screen Image