Impulse CoValidator™ Test Bench Generator

Accelerate FPGA verification time by generating HDL test benches from C

Impulse CoValidator™ provides a fast path from C-language to hardware-accurate and bit-accurate RTL simulation. Use CoValidator with the Impulse CoDeveloper™ C-to-FPGA compiler to design FPGA hardware and hardware test bench elements using standard C. Verify the generated HDL with automatically generated HDL test benches, before synthesizing the HDL to a target FPGA device.

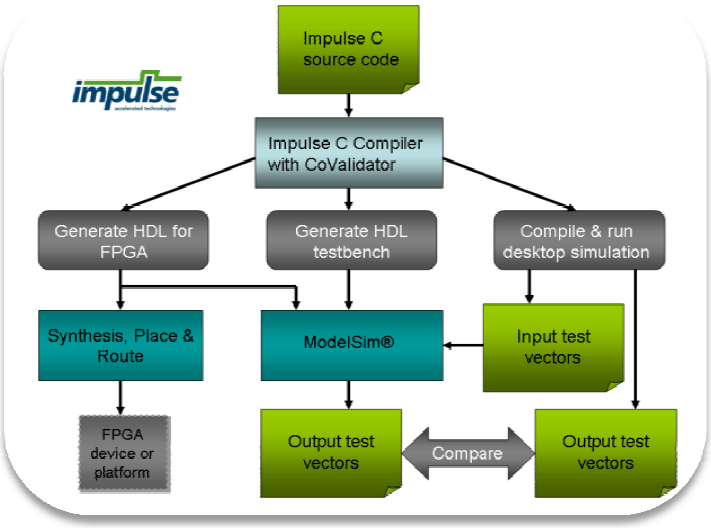
CoValidator lets you use standard C debuggers such as Visual Studio® to validate your application, then compare the results with hardware-accurate HDL simulation. Use C-language for HDL test bench generation to accelerate the FPGA development and debugging process. Use third-party and open source libraries to generate streams of input data, for example using standard-format audio, image or video files. CoValidator generates HDL compatible with all IEEE-compliant VHDL simulators, and also generates scripts for ModelSim® letting you generate HDL test benches and launch simulation with just a few keystrokes. Catch errors before going through FPGA synthesis and place-and-route, and save hours, days or even weeks off of your development time.

Key product benefits

- Generate portable HDL test bench code ready for use with any IEEE standard simulator.
- Generate simulation test files from C-language software, for software and RTL equivalency checking.
- Generate ModelSim compatible simulator scripts, to run HDL simulation with a single command.
- Iteratively verify your design, from unit tests to a complete system test suite.
- Verify bit-accurate and cycle-accurate behavior or your Impulse C hardware modules.
- Trace activity on inputs and outputs, using Impulse C-language APIs to describe streaming I/O.
- Generate and monitor an unlimited number of I/O streams, of any data width.
- Improve your design productivity by leveraging pre-optimized functions and open-source software.
- Reduce your project risk by reusing known-good C-language code for validation.
- Extend your CoValidator testing environment with customized, application specific producer and consumer functions – ask us for details.

Design Flow

1. Design hardware algorithms using C-language design methods.
2. Validate correct untimed algorithm behavior with standard C compilers and debuggers such as Visual Studio, Eclipse, or GCC.
3. Generate an HDL test bench, data and simulator scripts for hardware validation and hardware/software equivalency checking.
4. Analyze, parallelize and optimize your algorithmic C code with CoDeveloper, and generate synthesis-ready HDL.
5. Use an industry-standard HDL simulator to validate the generated hardware, using automatically generated test benches.
6. Export verified VHDL or Verilog to synthesis.



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Using Test Bench Generation with other FPGA tool flows

CoValidator is perfect for validating your C-to-FPGA design flow using RTL simulation techniques. Use it for unit testing of individual hardware modules, or to validate entire DSP or video pipelines. CoValidator greatly speeds the path to HDL simulation by automatically generating test benches, using familiar Impulse C™ APIs and programming methods. Because the test bench and test vectors are generated during desktop simulation, creating new testing scenarios for complex applications is as easy as changing a few lines of C code.

Impulse C-to-FPGA and test bench generation tools generate HDL code that is fully compatible with a wide array of FPGA tools for synthesis and simulation. Test benches are easily generated for IEEE-compliant HDL simulators.

For ModelSim users, CoValidator also generates scripts for semi-automated simulation and equivalency checking. Contact us for information about integration with other simulation tools.

Tools, training and design services

Impulse expert staff members are here to help, providing product support, design consultation and custom development. Impulse tools are intuitive and fit into existing design flows.

Contact us to discuss your design requirements.

About Impulse C™ and CoDeveloper™

Impulse C allows you to accelerate your image, signal and data processing algorithms by taking advantage of FPGA parallelism, without writing low-level HDL. Impulse C is industry-proven for applications in defense, aerospace, medical, industrial and other performance-critical applications. Impulse products and services allow more rapid development of high-performance embedded and streaming video systems using familiar software programming methods.

Impulse CoDeveloper includes the Impulse C software-to-hardware compiler, interactive parallel optimizer, and Platform Support Packages for a wide range of FPGA-based systems. Impulse tools are compatible with all popular FPGA platforms and tools.

Hardware IP blocks from C code

Support for module generation allows hardware IP blocks to be generated from C-language, using named ports and streaming API functions to integrate these blocks with the overall design. Impulse C IP blocks can be mixed with Verilog or VHDL, or with IP created using FPGA manufacturers tools. For video applications, the Impulse C API functions can be used to combine multiple streaming C-language processes to create highly pipelined, high-throughput systems.

Rapid prototyping

By working at a higher level of abstraction, you can more quickly generate working prototypes for system testing. This allows you to try dramatically different algorithmic approaches with only minimal changes to the C source code. Experiments that can take hours to accomplish in HDL can take just minutes using Impulse C.

About Impulse

Impulse is the market leader in software-to-FPGA solutions for embedded and high performance computing. Impulse C is used by 8 of the top 10 US government contractors, half the worldwide automakers and dozens of communications, instrumentation and medical imaging companies.

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