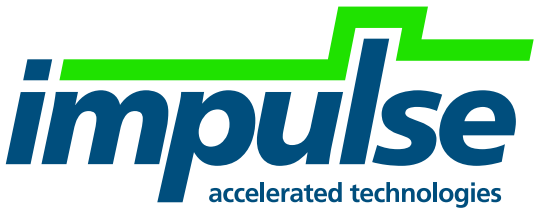

FOR IMMEDIATE RELEASE

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Impulse Releases Version 2 of its CoDeveloper™ C-to-FPGA Tool

New features include Verilog output, redesigned IDE and improved code optimizer

Kirkland, WA – July 21, 2005 – Impulse Accelerated Technologies™ today announced the second major release of its CoDeveloper™ C-to-FPGA design tool. The new release adds significant new capabilities and improved quality-of-results for the latest FPGA devices. New features include:

- Redesigned Application Manager™ and Application Monitor™ interfaces
- VHDL and Verilog compiler output options
- Enhanced instruction scheduling and loop pipelining
- Improved support for fixed-width integers and fixed-point math operations
- Support for module generation through the use of named ports
- Improved optimizer reports, including pipeline effective rate estimates
- Many new examples and tutorials

Support for embedded processor interfaces has also improved in Version 2, including support for the latest processors from Altera and Xilinx. The Impulse C™ libraries included with CoDeveloper Version 2 support multiple programming models including streams, signals and shared memories, allowing a software programmer to make use of available FPGA resources for hardware coprocessing without the need to write low-level hardware descriptions.

The compiler tools included with CoDeveloper Version 2 provide the necessary C-to-hardware compilation path, as well as providing automated generation of software/hardware interfaces that are specifically optimized for FPGA-based processor platforms. This capability makes it possible for an application developer to create a complete hardware/software application with no need to write VHDL or Verilog code. Instead, the CoDeveloper tools create the necessary low-level hardware and software descriptions (in the form of HDL outputs and automatically-generated software libraries) which can then be imported directly into existing FPGA tools (including tools from Xilinx, Altera and Synplicity) for hardware synthesis and implementation.

By allowing software application developers to create FPGA-based prototypes and end-products, CoDeveloper Version 2 promises to dramatically improve development productivity and design

innovation. CoDeveloper gives developers the freedom to try new and different ways of implementing mixed software/hardware applications, without the hardware design lead-times that would otherwise be required.

“One of the key benefits we offer embedded systems programmers and FPGA designers is the ability to experiment,” states David Pellerin, Chief Technology Officer of Impulse. “Our target customers include software developers who may not be familiar with low-level FPGA design techniques and tools, and who are unwilling to invest the amount of time needed to craft hardware solutions using existing methods. With CoDeveloper Version 2, we have extended the capabilities of our tools to serve the growing need for powerful yet accessible software-to-hardware solutions.”

About Impulse

Founded in 2002, Impulse provides design tools that enable true software programming of FPGA devices using the C language. The Impulse CoDeveloper tools allow FPGA algorithms to be developed and debugged using popular C/C++ development environments, including Microsoft Visual Studio™ and GCC-based tools. The CoDeveloper software-to-hardware compiler translates C-language processes to low-level FPGA-hardware, while optimizing the generated logic and identifying opportunities for parallelism. The compiler analyzes untimed C code and collapses multiple C statements and operations into single-clock instruction stages. CoDeveloper unrolls loops and generates loop pipelines to exploit the extreme levels of parallelism possible in an FPGA. CoDeveloper’s Application Monitor™ generates debugging visualizations for highly-parallel, multi-process applications, helping system designers identify dataflow bottlenecks and other areas for acceleration.

For applications involving embedded processors, CoDeveloper automates the creation of hardware/software interfaces and generates outputs compatible with popular FPGA synthesis and system-builder tools including Xilinx Platform Studio™ and Altera SOPC Builder™. This makes it possible to create high performance, mixed hardware/software applications for FPGA-based platforms without the need to write low-level VHDL or Verilog.

Pricing and Availability

Impulse CoDeveloper Version 2 is available now, with prices starting at from $4,995 for a perpetual, single-user license. Annual and floating licenses are also available. 30-day evaluations are free to qualified organizations and individuals. Visit www.ImpulseC.com for more information or contact info@ImpulseC.com.