For Immediate Release

Impulse C-to-FPGA Tools to be Featured at 2008 Embedded Systems Conference Silicon Valley

Impulse Founder and CTO David Pellerin to co-present FPGA workshop at ESC Silicon Valley, April 17 at 10:30 AM

What: Embedded Linux FPGA workshop
Where: Embedded Systems Conference in San Jose, CA
When: April 15 - 17, 2008

Kirkland, WA – March 20, 2008 – Impulse Accelerated Technologies will join LynuxWorks (of San José, California) and Xilinx (also of San José, California) to present a workshop titled "Optimizing Embedded Linux using HW/SW Co-Design" at this year's Embedded Systems Conference Silicon Valley, April 15-17.

The workshop, which will be presented in Marriot Salon 5/6 on Thursday, April 17 at 10:30 AM, will focus on the use of the Xilinx MicroBlaze™ processor, the LynuxWorks BlueCat® Linux operating system and the Impulse CoDeveloper™ C-to-FPGA tools for the fast creation, optimization and deployment of FPGA-accelerated embedded systems for DSP, image processing and other domains.

The workshop, presented jointly by Sonia Leal (LynuxWorks), Navanee Sundaramoorthy (Xilinx), and David Pellerin (Impulse) will include an overview of FPGA-embedded processors, the embedded Linux operating system and the use of C-language FPGA programming methods for algorithm acceleration. Examples of C-language code optimization and cycle-accurate debugging, as well as platform-specific hardware generation, will be presented.

Single-chip, dual PowerPC embedded video system to be showcased

Impulse will also conduct live demonstrations of its C-to-FPGA solutions in the Xilinx booth at ESC (booth #1138). The live demonstrations will include an accelerated dual-processor video application implemented on a Xilinx ML410 development board, equipped with a Xilinx Virtex™-4 FX60 FPGA device.

In the dual-PowerPC demonstration application, the embedded PowerPC processors are accelerated using closely-coupled FPGA accelerators, written in C, that perform image processing functions including inverse discrete cosine transform (IDCT), YUV to RGB color conversion, and run-time configurable video image filters. One of the PowerPCs runs an embedded operating system including an embedded web server and display driver, while the second PowerPC is dedicated to video decoding and real-time image filtering. High-speed serial interfaces are used to communicate video data directly between the two processors and the configurable filters, demonstrating the high performance and scalability of FPGA-based embedded computing.

For more information about this event and to register for the conference, visit www.cmp-egevents.com/web/esv/home. For more information about Impulse C-to-FPGA solutions for accelerated embedded systems, visit www.ImpulseC.com.