Impulse Ready-to-Run Example

Accelerating a Complex FIR Filter on an Avnet Virtex-5 FXT Board

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Overview

This ready-to-run example demonstrates how to use Impulse C to create an accelerated DSP application using an Avnet Virtex-5 FXT Evaluation Kit, the Xilinx EDK tools and the embedded PowerPC440 processor. The methods used in this example can be applied to many similar embedded PowerPC applications.

This example assumes some knowledge of the Xilinx EDK tools. For a detailed description of how to use Impulse C with the Xilinx EDK tools and the PowerPC processor, please see the tutorials installed with your Impulse CoDeveloper tools.

See also the following Xilinx application note:

> http://www.xilinx.com/support/documentation/application_notes/xapp901.pdf

Example Notes

Impulse C can be used to generate hardware modules that are directly connected to an embedded processor (such as the Xilinx PowerPC) or to other hardware elements that may have been described using other design tools or techniques. The Impulse C programming model emphasizes the use of data streams, signals, and shared memories for process-to-process communication. These interfaces can be used to connect Impulse C processes to a wide variety of hardware devices and processors.

For the PowerPC embedded processor, there are multiple possible ways to provide communication between a software application running on the processor, and a hardware accelerator running in the FPGA fabric. These include (among others):

- Using the PLB to create an Impulse C peripheral on a shared bus
- Using the APU interface to create a high-speed data stream
- Using shared memory

This example demonstrates a streaming application using the APU.

In this example, a software application running on the PowerPC communicates with the hardware FIR filter using Impulse C API functions/macros, which are implemented by the Impulse C compiler using the APU.

Project Files and EDK Settings

ZIP File Directory Structure
Avnet_fxt_ComplexFIR.PDF   (This document)
fxtPComplexFIR_edk10_1_02/   (Impulse C project source files)
fxtPComplexFIR_edk10_1_02/EDK   (EDK project)
fxtPComplexFIR_edk10_1_02/ReadyToRun   (download.bit and executable.elf)

Hardware Platform
Avnet Virtex-5 FXT Evaluation Kit

Software Versions
Impulse CoDeveloper Version 3.20
Xilinx ISE Version 10.1 SP2
Xilinx EDK Version 10.1 SP2

Impulse C Platform Support Package
Xilinx Virtex-5 APU

Xilinx EDK Settings
Board name: Avnet Virtex-5 FXT
Processor: PowerPC
Reference clock frequency: 100 MHz
Processor clock frequency: 125 MHz
System bus clock frequency: 125 MHz
Local memory (BRAM): 32 KB
IO Devices:
    RS232_Uart   19200 8-N-1
    LEDs_8bit
    DDR2_SDRAM
Peripherals:
    XPS TIMER   32 bit   one timer
STDIN: RS232_uart
STDOUT: RS232_Uart
Boot Memory: ilmb_cntlr

An FCB (Fabric Co-processor Bus) is needed for connecting the Impulse APU module to the PowerPc.

A clock output with a frequency of 62,500,000 Hz is needed to be added to the clock generator for the Impulse module's co_clk.

PowerPC APU_CONTROL is set to be 0b0000000000000001.

PowerPC ports: CPMINTERCONNECTCLK = ppc440_0_CPMINTERCONNECTCLK
                    CPMINTERCONNECTCLKNTO1 = net_gnd
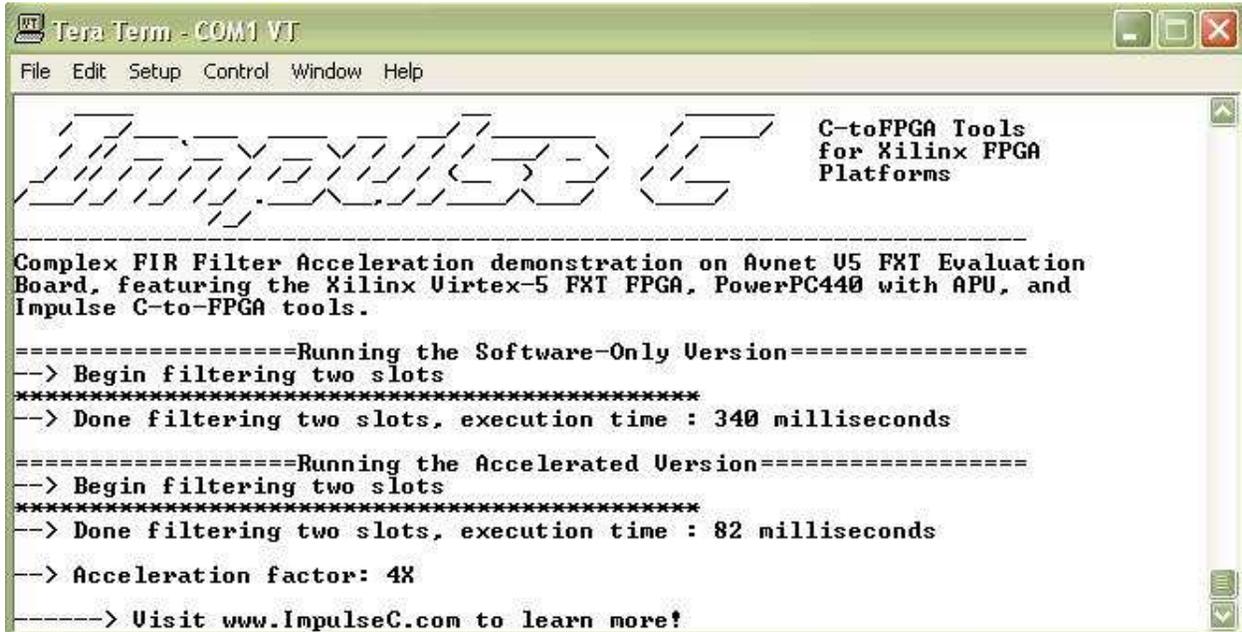
Downloading the Bitmap
The *download.bit* file can be downloaded to the FPGA using iMPACT.

XMD Commands for Execution
  dow filt/executable.elf
  con

Result Display
  Open a HyperTerminal or TeraTerm window, and set the serial port to baud rate 19200, 8-N-1. The output will be as shown below: