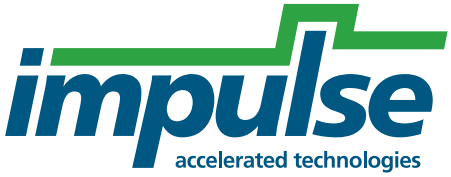

Impulse Ready-to-Run Example

Accelerating MPEG2 Decoding on a Xilinx ML507 Board

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Overview

This ready-to-run example demonstrates how to use Impulse C to create an accelerated MPEG2 deciding application using a Xilinx ML507 development board, the Xilinx EDK tools and the embedded Xilinx PowerPC processor. The methods used in this example can be applied to many similar embedded PowerPC applications.

This example assumes some knowledge of the Xilinx EDK tools. For a detailed description of how to use Impulse C with the Xilinx EDK tools and the PowerPC processor, please see the tutorials installed with your Impulse CoDeveloper tools, in the Help and Support section of the Start Page.

Example Notes

Impulse C can be used to generate hardware modules that are directly connected to an embedded processor (such as the Xilinx PowerPC) or to other hardware elements that may have been described using other design tools or techniques. The Impulse C programming model emphasizes the use of data streams, signals, and shared memories for process-to-process communication. These interfaces can be used to connect Impulse C processes to a wide variety of hardware devices and processors.

For the PowerPC embedded processor, there are multiple possible ways to provide communication between a software application running on the processor, and a hardware accelerator running in the FPGA fabric. These include:

- Using the PLB bus to create an Impulse C peripheral on a shared bus
- Using the APU interface to create a high-speed data stream
- Using shared memory

This example demonstrates a streaming application, using the APU and two distinct accelerated hardware processes. The two hardware processes are:

- YUV Color Conversion
- Discrete Cosine Transform

In this example, a software application running on the PowerPC communicates with the hardware accelerators using Impulse C API functions/macros, which are implemented by the Impulse C compiler using the APU.

Running the Example

On the ML507, connect power, a video display to the DVI connector, and a JTAG programming cable. Assuming Xilinx ISE and EDK tools are in executable paths, on a Windows host running 'run_mpeg_demo.bat' in the 'EDK' directory will:

1) download the .bit file into the ML507's FPGA
2) load the video and executable binary files into CPU memory
3) start execution of the example

On a Linux host this may be done via 'source run_mpeg_demo.bat'.

Project Files and EDK Settings

ZIP File Directory Structure

MPEG2_ML507.PDF	(This document)
MPEG2_ML507.ZIP	(Impulse C project source files and EDK project)

Hardware Platform

Xilinx ML507 development board

Software Versions Used

Impulse CoDeveloper Version 3.10.b.10
Xilinx ISE Version 10.1 SP1
Xilinx EDK Version 10.1 SP1

Impulse C Platform Support Package

Xilinx Virtex-5 PowerPC APU