Impulse CoValidator™ Automatically Generates ModelSim® FPGA Test Benches from C

FPGA developers accelerate verification time using software-to-hardware testing methods

Kirkland, WA – May 9, 2009 – Impulse Accelerated Technologies today announced the release of CoValidator, a tool that automatically generates FPGA test benches from C. CoValidator is an extension of the Impulse CoDeveloper C-to-FPGA tools. The combined CoDeveloper and CoValidator tools allow FPGA system designers to write, refactor, optimize and synthesize FPGA software and hardware with ANSI C, then verify the results of their efforts using industry-standard simulation tools.

As more software developers accelerate processing code in FPGAs, the handoff to hardware engineering can be the critical path. Valuable project time is recovered when simulation test benches are developed concurrently with the algorithms. CoValidator generates hardware test benches from the same C code used to describe and test algorithms in software, reducing test development time and increasing overall system reliability by having test development stay in step with design development.

Impulse software-to-hardware tools enable developers to create complex image, signal and data processing algorithms, with only limited FPGA knowledge. CoValidator adds a fast path from C-language to hardware-accurate and bit-accurate RTL simulation. In the flow, developers design FPGA hardware and hardware test bench elements concurrently using standard C. The C code is refactored, optimized and compiled to create synthesis-ready HDL. With CoValidator, VHDL test benches are created automatically for ModelSim or other IEEE compliant VHDL simulators. Development time is shorter, development costs are lower and results are better.

“CoValidator resulted from our own internal testing requirements” noted Brian Durwood, COO and co-founder of Impulse, “Our engineering staff uses automated, C-based test bench generation internally during development. We knew that many Impulse C users have access to VHDL simulators such as ModelSim, so we extended our C-to-FPGA tools to allow our customers the same benefits. We believe this method of testing helps software and hardware engineers collaborate better.”

Using C-language for HDL test bench generation has many benefits. Third-party and open source libraries can be used to generate streams of input data, for example using standard-format audio, image or video files. Standard C debuggers such as Visual Studio® can be used validate applications. Significant schedule time is saved by applying higher-level, more productive design methods to FPGA design processes.

CoValidator is fully compatible with industry-standard RTL simulators. CoValidator generates HDL compatible with all IEEE-compliant VHDL simulators, and also generates scripts for selected simulators including ModelSim. ModelSim users can generate HDL test benches and launch simulation with just a few keystrokes, catching errors before going through FPGA synthesis and place-and-route.

Ready-to-run reference applications are available for image, vision, signal and data processing. Impulse tools work with Xilinx and Altera devices, embedded processor cores and FPGA development boards.

About Impulse

Impulse provides software-to-FPGA solutions for embedded and high performance computing. Impulse is used by 8 of the top 10 government contractors, half the worldwide automotive manufacturers and by a wide range of medical, industrial and consumer processing designers.

For more information, visit www.ImpulseAccelerated.com or call 425-605-9543, Ext 101.