M200 World's most Advanced Wearable Processor Unit

Efficient Performance

Integrating XBurst, ultra-low power CPU technology, the Ingenic M200 Wearable Processor Unit (WPU) is the industry's most advanced solution for manufacturers wishing to develop wearable devices. M200 is a no compromise design, it has the lowest power requirements of any SoC in its class while delivering performance equivalent to processors used in mass market smartphones and tablets. Above all, battery life will be its longest when Ingenic is at the heart of the solution.

Highlights

- XBurst-HP and XBurst-LP dual-core CPU configuration (1.2GHz/300MHz) based on MIPS
- Low power 3D engine with OpenGL ES2.0 support.
- Voice trigger engine
- H.264 720p video encoder, full-format 720p video decoder
- Super integration, a highly optimized BOM cost
- Complete Android system, regular upgrades and updates
- Turn-key solution for smart watch and smart glass
- Small package size: 7.7 x 8.9 x 0.76 (mm)

Ingenic XBurst technology

XBurst, based on the MIPS Instruction Set Architecture (ISA), is a pure, fast and efficient RISC processor. Using ultra low power pipelining techniques XBurst 1 can deliver 2.0 DMIPs/MHz while consuming only 0.07mW/MHz, the CPU core is capable of operating at speeds above 1.2GHz. In contrast, other industry licensable CPUs consume over twice the power while delivering lower performance. Ingenic has developed a family of SoCs which power products such mobile devices, eReaders, portable media players and now wearable devices.

Ingenic video processing engine

Ingenic's proprietary VPU (Video Processing Engine) uses a combination of custom hardware and a microcode engine to provide a low power, yet flexible and upgradeable solution to video encoding and decoding. This approach allows H.264 720P@30fps streams to be decoded consuming less than 30mW, all industry standard video CODECs are supported.

Key benefits of M200

Ultra low power with mobile performance

User experience for wearable devices is measured by two factors: the richness of the applications that can be used and the battery life of the device. M200 is the industry's first dedicated SoC for the wearable market. In full operating mode it consumes only 150mW and when in standby the power requirement is dropped to only 200uA. Ingenic's engineers were able to achieve this groundbreaking performance by redesigning of all the key modules inside the SoC to target ultra-low power operation, M200 is unique and cannot be replicated by other suppliers that rely on licensed IP.

Ultra Low-power technology

Not only did Ingenic's engineers redesign every module inside the M200, the fabric of the SoC is designed with multiple low power modes and power islands. Essentially the complete SoC can be placed in standby or sleep mode and then woken up by a voice trigger.

Super Integration

M200 sets the integration standard for the wearable market. Included in the device are functions such as MIPI-CSI, MIPI-DSI, USB 2.0, MMC/SD interface. With a package size of only 7.7x8.9x0.76 (mm) the PCB footprint of Ingenic based solutions will be the smallest and most competitive in the market. With its low height, products can be developed that are stylish and fashionable rather than large and unattractive.

Comprehensive turn-key design

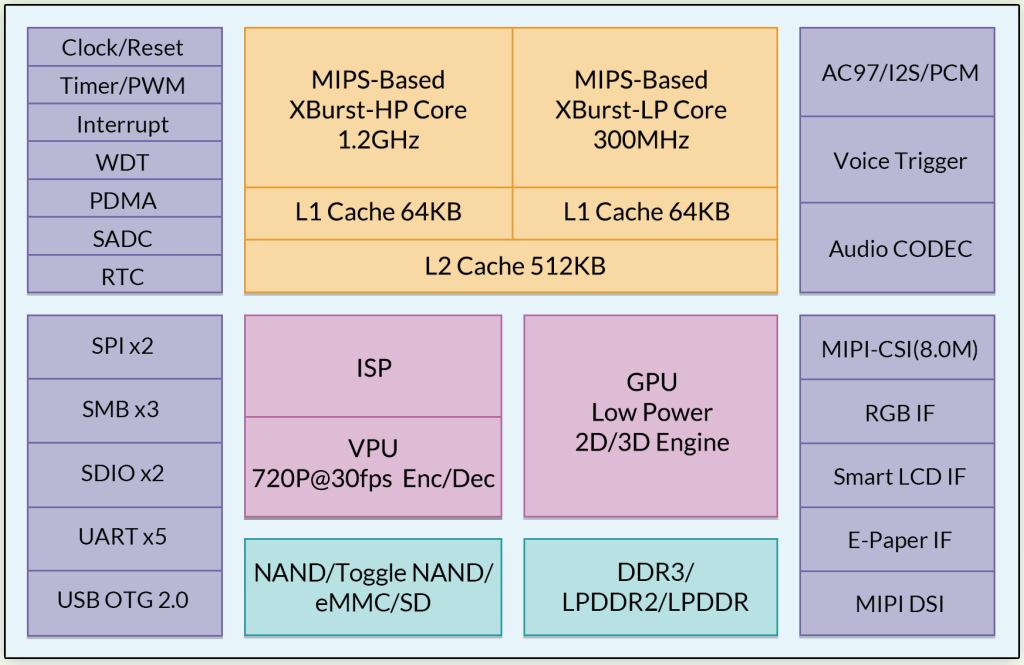
Ingenic, with its partners, has developed complete turn-key platforms for smart watch and smart glass. This package including schematics, bill of materials and PCB layout is available to our customers and will significantly reduce product development time and development risk. Ingenic provides the latest version of Android to run on these platforms.

Board Support Package

Ingenic supplies a complete board support package (BSP) for the M200. The BSP includes OS kernel, device drivers, middleware and sample applications from third parties. Source code is provided and the release is typically timed to coincide with SoC availability. Both Linux and Android BSP's are available.

M200 Mobile Performance with Wearable Power

M200 Block Diagram



Product Feactures

CPU Core
- XBurst-HP core, up to 1.2GHz
- XBurst-LP core, up to 300MHz
- 64KB L1 cache for each core and 512KB unified L2 cache

GPU Core
- Low-power 2D/3D core, OpenGL ES2.0/1.1 compliance; OpenVG 1.1

VPU Core
- Dedicated video processor with upgradeable microcode engine.
- Encoding and decoding support for up to 720P30 video streams.
- Camera interface: DVP, MIPI-CSI2(2-lanes); internal ISP function.
- Highest level 1 security boot.

ISP Core
- Wide Dynamic Range (EDR), dual-stream processing.
- Video and still image stabilization.
- Image cropping and rescaling.
- Auto exposure and gain control.
- Auto white balancing and auto focus control.
- Edge sharpening and advanced noise reduction.
- Color correction and management.

Memory Sub-systems
- Support DDR2, DDR3, LPDDR, LPDDR2, up to 667Mbps
- Support x16 and x32 external DDR data width
- 64-bit ECC NAND flash support, 512B/2KB/4KB/8KB/16KB page size
- Support Toggle1.0/ONFI2.0 NAND
- 2 channels high performance PDMA, and 30 channels general purpose DMA

System Devices
- Clock generation and power management with 2 PLLs
- Interrupt controller, total 64 sources
- OS timer, general timer and counter unit, watchdog timer lock

Audio/Display/UI Interfaces
- Support panel interface: TFT, SLCD, MIPI-DSI, up to 800x480@60Hz(BPP24)
- E-Ink panel interface support
- Support camera interface: DVP, MIPI-CSI; internal ISP function support
- Internal audio codec: 24-bit ADC/DAC, stereo line-in, MIC in, headphone interface
- DMIC controller
- AC97/I2S/SPDIF interface for external audio codec
- One PCM interface
- 3 channels SAR A/D controller

Voice trigger function
- Low-power DMIC controller with special sleep mode
- System wakeup by specific voice

On-chip Peripherals
- USB 2.0 OTG interface
- 2 MMC/SD/SDIO controllers, support MMC version 4.2, SD 3.0
- 5 full-duplex UART ports
- 2 synchronous serial interface controllers
- 4 two-wire serial interface controllers

Security
- Total 4K bits OTP memory
- Support the highest lever 1 security boot

Process Technology and Package
- 40nm CMOS LP, BGA270 7.7mm x 8.9mm x 0.76mm, 0.4mm pitch