JZ4780

Mobile Application Processor

Data Sheet

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北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

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1 Overview

JZ4780 is a mobile application processor targeting for multimedia rich and mobile devices like tablet computer, smart phone, mobile digital TV, and GPS. This SOC introduces a kind of innovative architecture to fulfill both high performance mobile computing and high quality video decoding requirements addressed by mobile multimedia devices. JZ4780 provides high-speed CPU computing power, good 3D experience and fluent 1080p video replay.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data level 1 cache, and 512kB level 2 cache, operating at 1.2GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is powered with another XBurst® processor engine. The SIMD instruction set implemented by XBurst® engine, in together with the on chip video accelerating engine and post processing unit, delivers high video performance. The maximum resolution of 1080p in the formats of H.264, VC-1, MPEG-2, MPEC-4, RealVideo and VP8 are supported in decoding, the maximum resolution of 1080p in the format of H.264 are supported in encoding.

The GPU (Graph Processing Unit) core supports numerous 2D/3D graphics applications. It delivers hardware acceleration for 2D and 3D graphics displays, and supports screen sizes range from the smallest cell phones to full HD 1080p displays. It supports the standard APIs such as OpenGL ES2.0 and 1.1, and Open VG. The OS of Android, Linux and Windows are supported. The GPU provides high performance, high quality graphics and low power consumption.

The memory interface supports a variety of memory types that allow flexible design requirements, including glueless connection to SLC NAND flash memory or up to 64-bit ECC MLC/TLC NAND flash memory and toggle NAND flash for cost sensitive applications. It provides the interface to DDR2, DDR3, LPDDR and LPDDR2 memory chips with lower power consumption.

On-chip modules such as audio CODEC, multi-channel SAR-ADC, AC97/I2S controller and camera interface offer designers a rich suite of peripherals for multimedia application. GPS baseband is embedded. The LCD controller support regular RGB, LVDS and HDMI transmitter, up to 2-channel 1920x1080 output(One channel must be LVDS or HDMI), WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. The TS (Transport stream) interface provides enough bandwidth to connect to an external mobile digital TV demodulator. Other peripherals such as USB OTG and USB 2.0 host, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

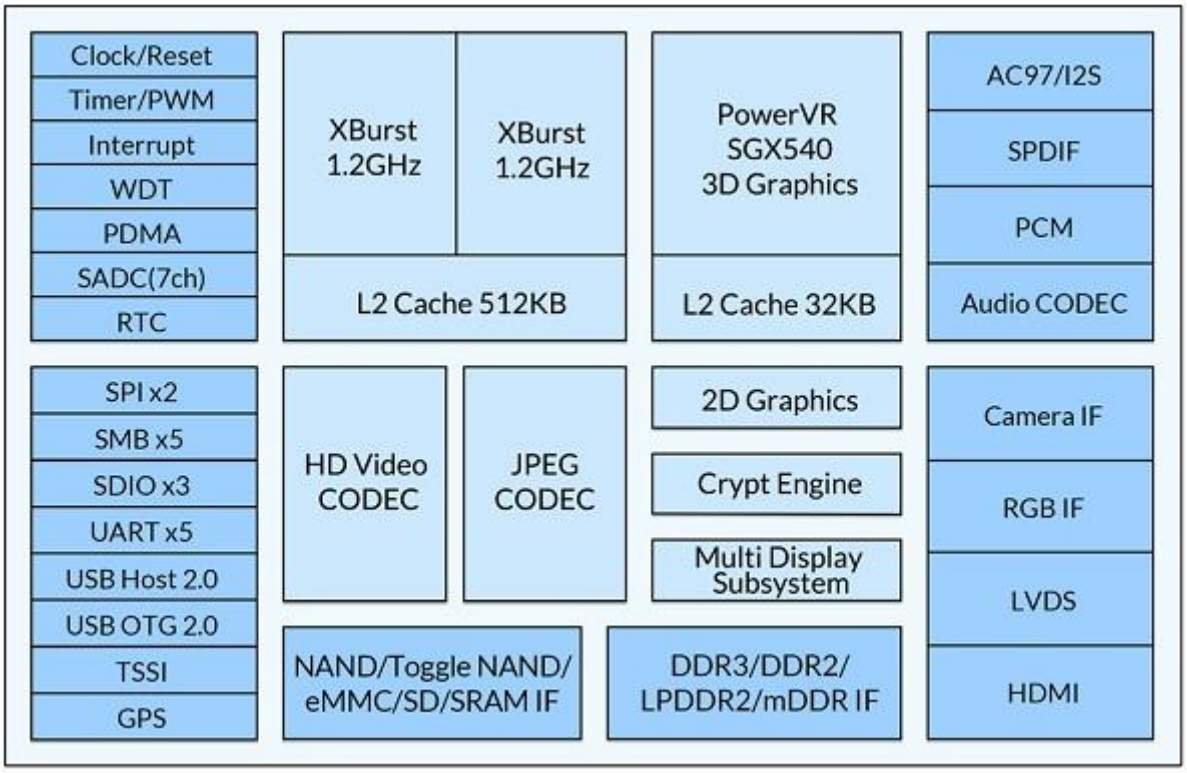


Figure 1-1 JZ4780 Diagram

1.2 Features

1.2.1 CPU

A symmetric XBurst®-1 dual-core implementation, with IRQ dispatching for each core and MSI protocol for cache coherence.

- XBurst®-1 core
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.2G.
  - MMU
    - 32-entry joint-TLB
    - 8 entry Instruction TLB
    - 8 entry data TLB
  - L1 Cache
    - 32kB instruction cache

        - 32kB data cache
    - Hardware debug support
    - 16kB tight coupled memory
- L2 Cache
    - 512kB unify cache
- CoreScheduler
    - Dedicated IRQ dispatcher managing IRQs to each core
- GDIR
    - Global directory aiding MSI protocol for cache coherence

1.2.2 VPU

Include Video Codec and JEPG Codec,

- MPEG-2 decoding up to 1080P 60fps
- VC-1 decoding up to 1080P 60fps
- H.264 decoding up to 1080P 60fps
- VP8 decoding up to 1080P 60fps
- MPEG-4 decoding up to 1080P 30fps
- RV9 decoding up to 1080P 30fps
- H.264 encoding up to 1080P 30fps
- JPEG compressing up to 100Mega-pixels per second (baseline)

1.2.3 GPU

- 3D graphics (PowerVR SGX540)
    - Deferred Pixel Shading
    - 32bit floating point depth accuracy with on chip depth buffer
    - 8-bit Stencil with on chip tile stencil buffer
    - 8 parallel depth/stencil tests per clock
    - Scissor test
    - Texture support
        - Cube Map
        - Projected Textures
        - Non square Textures
    - Texture Formats
        - RGBA 8888,565,1555,1565
        - Mono chromatic 8, 16, 16f, 32f, 32int
        - Dual channel, 8:8, 16:16, 16f:16f
        - Compressed Textures PVR-TC1, PVR-TC2, ETC1
        - Programmable support for YUV formats
    - Resolution Support
        - Frame buffer max size = 2048 x 2048
        - Texture max size = 2048 x 2048

- Texture Filtering
  - Bilinear, Trilinear, Anisotropic
  - Independent min and mag control
- Anti-aliasing
  - 4x Multisampling
  - up to 16x Full scene anti-aliasing
  - Programmable sample positions
- Indexed Primitive List support
  - Bus mastered
- Programmable vertex DMA
- Render to texture
  - Including twiddled formats
  - Auto MipMap generation

- 2D Graphics (X2D)
  - Location: AHB bus
  - Input format
    - Separate frame: YUV /YCbCr (4:2:0)
    - Packaged data: RGB888, RGB565, RGB555, NV12, NV21,TileYUV
  - Output data format
    - ARGB888，XRGB888, RGB555, RGB565
  - Color convention coefficient: configurable (CSC enable)
  - Minimum input image size (pixel): 4x4
  - Maximum input image size (pixel): 12288x12288 (12k x 12k)
  - Maximum output image size (pixel)
    - Width : up to 12288
    - Height: up to 12288
  - Image resizing
    - bi-cube zooming mode
  - Image Clockwise 90, 180, 270 rotation
  - Image horizontal and vertical mirror , same time with rotation
  - 5 layers OSD

1.2.4 Display/Camera/Audio

Include Multi-display subsystem and multiple display interface.

- LCD controller
  - Dual controller
    - Support dual panel(HDMI & TFT, or HDMI & LVDS, or TFT & LVDS, or HDMI & SLCD, or SLCD & LVDS)
    - Display size up to 4kx2k@30Hz(BPP24) for single panel, 1920x1080@60Hz(BPP24) for dual panel
  - Colors Supports
    - Encoded pixel data of 16, 18 or 24 BPP in TFT mode

- Support up to 16,777,216 (16M) colors in TFT mode
- Support 24/16 BPP compressed data
- Support 24 BPP packed data

– Panel Supports
- Support 16-bit parallel TFT panel
- Support 18-bit parallel TFT panel
- Support 24-bit serial TFT panel with 8 data output pins
- Support 24-bit parallel TFT panel
- Support Delta RGB panel
- Support SLCD panel
- Support HDMI 1.4a Interface
- Support LVDS Interface

– OSD Supports
- Supports one single color background
- Supports two foregrounds, and every size can be set for each foreground
- Supports one transparency for the whole graphic
- Supports one transparency for each pixel in one graphic
- Supports color key and mask color key
- Supports porter-duff blending

– Image Enhancement
- Color space conversion: RGB to YCbCr, YCbCr to RGB
- Support Contrast, Brightness, Hue, Saturation control
- Support Visibility Enhance
- Support Dither
- Support Gamma Correction

● Image post processor(IPU)

– Input format
- Separate frame: YUV /YCbCr (4:2:0, 4:2:2, 4:4:4, 4:1:1), RGB888
- Packaged data: YUV422, RGB888, RGB565, RGB555, YUV444
- Separate frame in block format: YUV/YCbCr 420

– Output data format
- RGB (565, 555, 888, AAA)
- Packaged data YUV422

– Color convention coefficient: configurable (CSC enable)
– Minimum input image size (pixel): 4x4
– Maximum input image size (pixel): 8096x8096
– Maximum output image size (pixel)
- Width: up to 4095 (without vertical resizing)
- up to 2048 (with vertical resizing)
- Height: up to 4095

– Image resizing
- Support bilinear
- 0 and bi-cube zooming mode

- Up scaling ratios up to 1:31 in fractional steps with 1/32 accuracy
- Down scaling ratios up to 31:1 in fractional steps with 1/32 accuracy

- Camera interface module
  - Input image size up to 4096x4096 pixels
  - Max. VGA for image preview
  - Max. VGA for video record
  - Integrated DMA
  - Supported data format: YCbCr 4:4:4, YCbCr 4:2:2 and other formats
  - Output format: csc mode is YCbCr 4:2:2 or YCbCr 4:2:0, bypass mode is the input data format
  - Output frame format
    - Packaged : for all data format
    - Separated: for YCbCr 4:4:4, YCbCr 4:2:2 and YCbCr 4:2:0
  - Supports ITU656 (YCbCr 4:2:2) input
  - Configurable CIM_VSYNC and CIM_HSYNC signals: active high/low
  - Configurable CIM_PCLK: active edge rising/falling
  - 256x33 image data receive FIFO (RXFIFO)
  - PCLK max. 80MHz
  - Configurable output order
- AC97/I2S/SPDIF controller
  - AC-link (AC97) features
    - Up to 20 bit audio sample data sizes supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Support variable sample rate in AC-link format
    - Multiple channel output and double rated supported for AC-link format
    - Power Down Mode and two Wake-Up modes Supported for AC-link format
  - I2S features
    - 8, 16, 18, 20 and 24 bit audio sample data sizes supported, 16 bits packed sample data is supported
    - Up to 8 channels sample data supported
    - DMA transfer mode supported
    - Stop serial clock supported
    - Programmable Interrupt function supported
    - Support share clock mode and split clock mode.
    - Support mono PCM data to stereo PCM data expansion on audio play back
    - Support endian switch on 16-bits normal audio samples play back
    - Internal programmable or external serial clock and optional system clock supported for I2S or MSB-Justified format
    - Internal I2S CODEC supported

  - Two FIFOs for transmit and receive respectively
- SPDIF features
  - 8, 16, 18, 20 and 24 bit audio sample data sizes supported
  - DMA transfer mode supported
  - Stop serial clock supported
  - Programmable Interrupt function supported
  - Support IEC60958 two-channel PCM audio
  - Support IEC61937 multi-channel compressed audio
  - Support consumer mode and only support transmitter mode
  - Profession mode is not supported
  - The User data bit is '0'as it is not supported in the chip
  - Support sampling frequency from 32kHz to 192kHz

- PCM interface
  - Data starts with the frame PCMSYN or one PCMCLK later
  - Support three modes of operation for PCM
    - Short frame sync mode
    - Long frame sync mode
    - Multi-slot mode
  - Data is transferred and received with the MSB first
  - Support master mode and slave mode
  - The PCM serial output data, PCMDOUT, is clocked out using the rising edge of the PCMSCLK
  - The PCM serial input data, PCMDIN, is clocked in on the falling edge of the PCMSCLK
  - 8/16 bit sample data sizes supported
  - DMA transfer mode supported
  - Two FIFOs for transmit and receive respectively with 16 samples capacity in every direction
- Internal CODEC Interface
  - 24 bits ADC and DAC
  - Headphone load up to 16 Ohm
  - Sample frequency supported: 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, and 96k
  - Stereo line input
  - DAC to HP path: Power consumption: 17.6mW, THD: -65dB @17.6mW /16Ohm
  - DAC to stereo line output path @10kOhm: SNR: 100dB A-Weighted, THD: -80dB @FS-1dB
  - Line input to ADC path: SNR: 90dB A-Weighted, THD: -80dB @FS-1dB
  - Separate power-down modes for ADC and DAC path with several shutdown modes
  - Reduction of audible glitches systems: Pop Reduction system, Soft Mute mode
  - Output short circuit protection
  - Embedded low noise Linear Regulator
  - 4 MIC in path or 4 line in path Maximum (Total 4 analog input)
  - Support Digital MIC

1.2.5 Memory Interface

- DDR Controller
  - Support DDR2, DDR3, DDR3L, DDR3U, mobile DDR (LPDDR), LPDDR2 memory，up to 800Mbps
  - Support x16 and x32 external DDR data width
  - Asynchronize to system bus and each port.
  - Support clock-stop mode
  - Support auto-refresh and self-refresh
  - Support power-down mode and deep-power-down mode
  - Programmable DDR timing parameters
  - Programmable DDR row and column address width and order
- Static memory interface
  - Support 6 external chip selection CS6~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank
- NAND flash interface
  - Support on CS6~CS1, sharing with static memory bank6~bank1
  - Support both of conventional NAND flash memory and Toggle NAND flash memory
  - Support most types of NAND flashes, 8-bit data access, 512B/2K/4K/8KB/16KB page size. For 512B page size, 3 and 4 address cycles are supported. For 2K/4K/8KB/16KB page size, 4 and 5 address cycles are supported
  - Support read/erase/program NAND flash memory
  - Support boot from NAND flash
- BCH Controller
  - Support up to 64-bit ECC encoding and decoding for NAND

1.2.6 System Functions

- Clock generation and power management
  - On-chip 12/24/48MHZ oscillator circuit
  - External 32.768KHZ input
  - One four-chip phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
  - SSI clock supports 50M clock

- MSC clock supports 100M clock
- Functional-unit clock gating
- Shut down power supply for P0, VPU, GPU, GPS, P1

- Timer and counter unit with PWM output and/or input edge counter
  - Provide eight separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
    - PCLK, EXTAL and RTCCLK can be used as the clock for counter
    - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SOC
  - A simple Xburst-1 CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: $1 \sim 2^{24} - 1$
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - A dedicated bus interface - BIF interconnects with on-chip BCH
  - A dedicated bus interface - NIF interconnects with on-chip NEMC or off-chip NEMC.
  - An extra INTC IRQ can be bound to one programmable DMA channel
  - Dedicated Security ROM and Security RAM supporting enhanced security requirements.
- SAR A/D Controller
  - 7 Channels

- Resolution: 12-bit
- Integral nonlinearity: ±1 LSB
- Differential nonlinearity: ±0.5 LSB
- Resolution/speed: up to 2Msps
- Max Frequency: 200k
- Low power dissipation: 1.5mW(worst)
- Support 4-wire and 5-wire touch panel measurement (Through pin XP, XN, YP, YN and AUX2)
- Support multi-touch detect
- Support write control command by software
- Support voltage measurement (Through pin VBAT)
- Support two auxiliary input (Through pin AUX1, AUX2)
- Single-end and Differential Conversion Mode
- Auto X/Y, X/Y/Z1/Z2 and X/Y/Z1/Z2/X2/Y2 position measurement
- Support external touch screen controller
- Pin Description

- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32k clock generation
  - RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter
- OTP Slave Interface
  - Total 8K bits. Lower 192bits are read only, other higher bits are read-able and write-able
  - Support Security boot.

1.2.7 Peripherals

- Transport stream slave interface
  - Support both parallel mode and serial mode for TS data transfer
  - TSDI0 or TSDI7 can be used to transfer data in serial mode
  - The order of data in one byte supports LSB at first or MSB at first
  - The order of data in one word supports LSB at first or MSB at first
  - Input control signals and data can be either active high or active low
  - Support using either positive or negative edge of TSCLK
  - Support PID filtering function
  - Up to 33 PID filters can be used when PID filtering function is enabled
  - Support adding data 0 before or after transport stream

- Support master DMA transmission

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 6 interrupts, 1 for every group, to INTC
- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 5 independent SMB channels (SMB0, SMB1, SMB2, SMB3, SMB4)
- Two Synchronous serial interfaces (SSI0, SSI1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI_CE_ / SSI_CE2_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing
- Five UARTs (UART0, UART1, UART2, UART3, UART4)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode

- Supports modem flow control by software or hardware
- Slow infrared asynchronous interface that conforms to IrDA specification

- Three MMC/SD/SDIO controllers (MSC0, MSC1, MSC2)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit ,4bit and 8bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
  - 128 x 32 built-in data FIFO
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes
- USB 2.0 host interface
  - Open Host Controller Interface (OHCI/EHCI)-compatible and USB Revision 1.1/2.0-compatible
  - High speed, Full speed and low speed
  - Embedded USB 2.0 PHY
- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints:
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer

1.2.8 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	40nm CMOS low power
Power supply voltage	General purpose I/O: 1.6~3.6V DDR I/O for DDR2: 1.8V± 0.1V DDR I/O for DDR3: 1.5V± 0.075V DDR I/O for DDR3L: 1.35V± 0.1V DDR I/O for DDR3U: 1.25V± 0.06V DDR I/O for LPDDR: 1.8V± 0.15V DDR I/O for LPDDR2: 1.2V± 0.1V RTC I/O: 1.8V~3.6V EFUSE programming: 2.5V± 10% Analog power supply 1: 2.5V± 10% Analog power supply 2: 3.3V± 10% Core: 1.1 -0.1/+0.2 V
Package	BGA390 17mm x 17mm x 1.1mm, 0.8mm pitch
Operating frequency	1.2GHz

2 Packaging and Pinout Information

2.1 Overview

JZ4780 processor is offered in 390-pin LFBGA package, which is 17mm x 17mm x 1.1mm outline, 21 x 21 matrix ball grid array and 0.8mm ball pitch, show in Figure 2-1. The JZ4780 pin to ball assignment is show in Figure **2-2**.

The detailed pin description is listed in Table 2-1~Table 2-28.

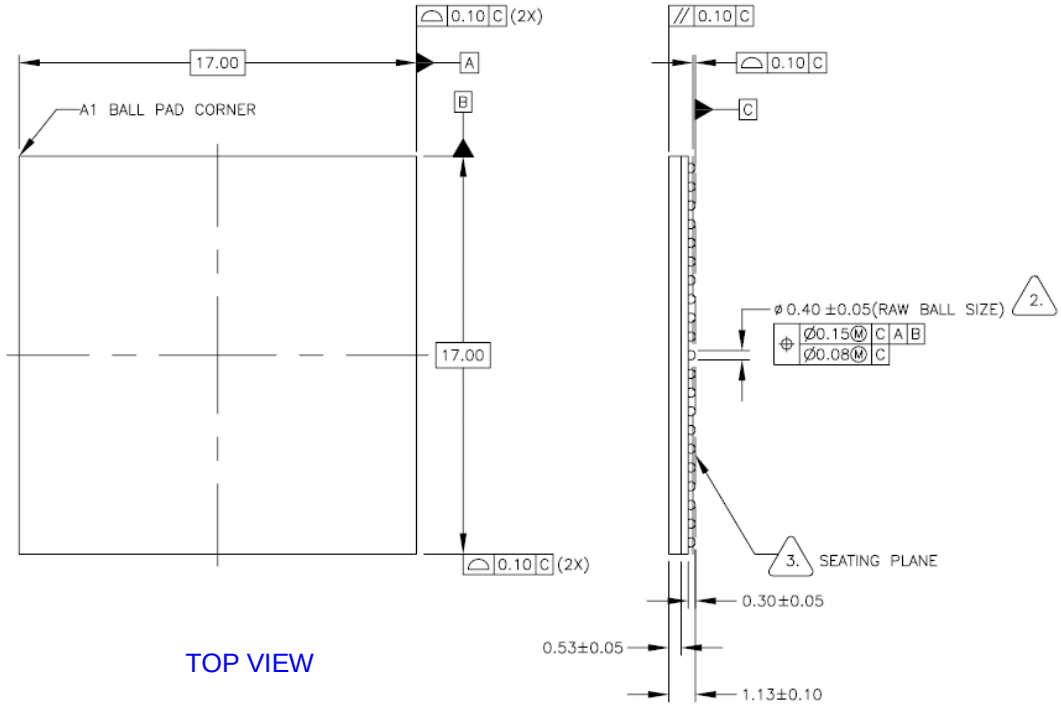
2.2 Solder Process

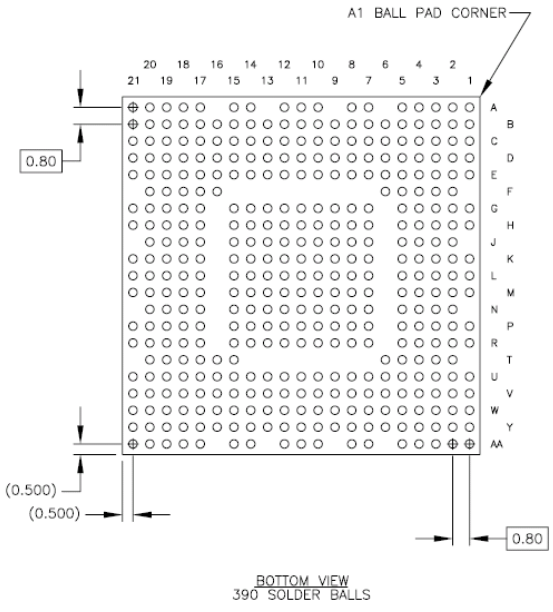
JZ4780 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

JZ4780 package moisture sensitivity is level 3.

2.4 JZ4780 Package





BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALL
4. REFERENCE SPECIFICATIONS:
   - A. AWW SPEC #001-0531-2234: PACKING OPERATION PROCEDURE
   - B. AWW SPEC #001-0519-2062: MARKING

Figure 2-1 JZ4780 package outline drawing

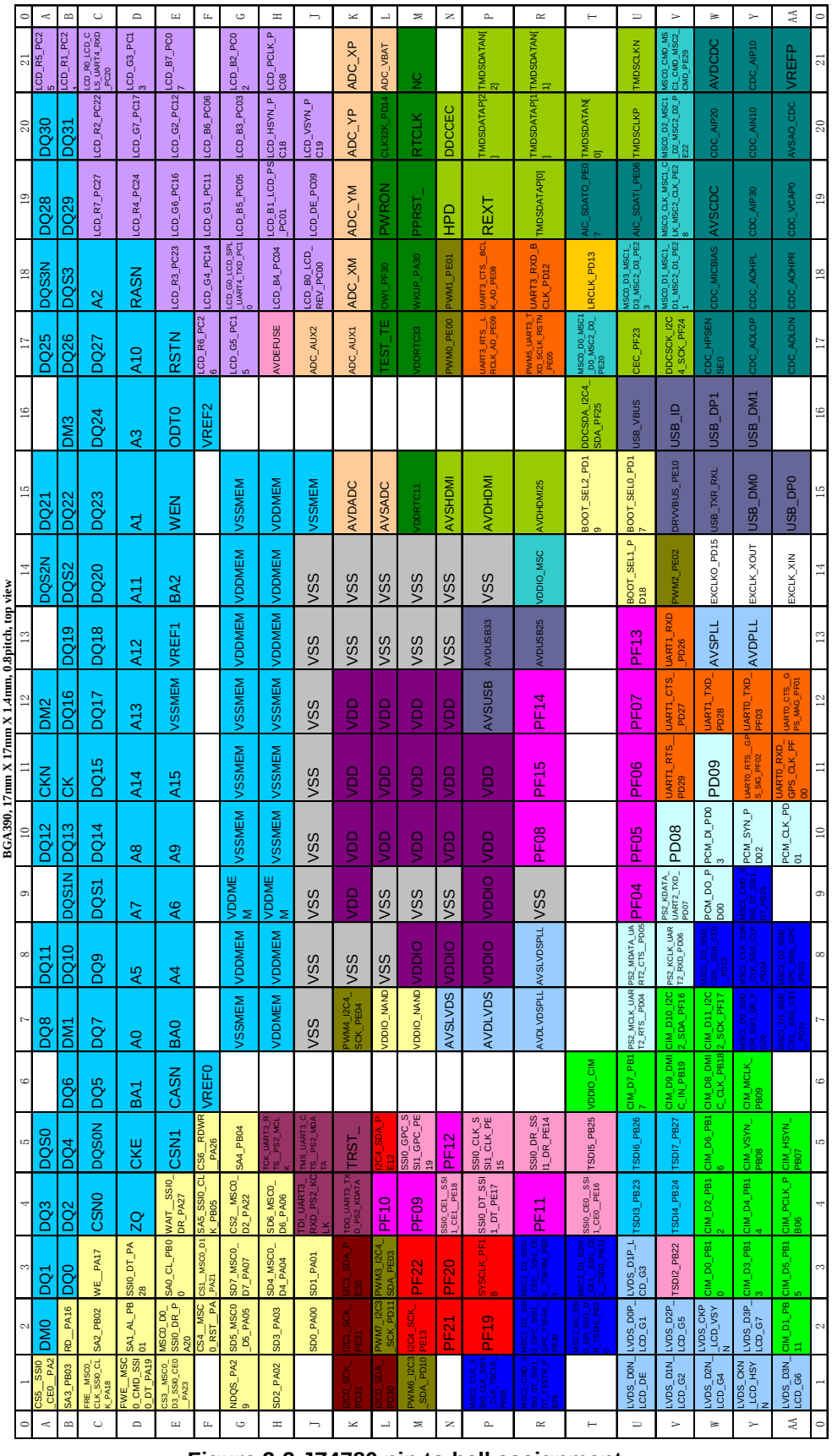


Figure 2-2 JZ4780 pin to ball assignment

2.5 Pin Description [1][2]

2.5.1 DDR

Table 2-1 DDR(mDDR, DDR2, LPDDR2, DDR3) Pins (77)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DQ0	IO	B3	Bi-dir, Single-end	DQ0: DDR data bus bit 0	VDD_{MEM}
DQ1	IO	A3	Bi-dir, Single-end	DQ1: DDR data bus bit 1	VDD_{MEM}
DQ2	IO	B4	Bi-dir, Single-end	DQ2: DDR data bus bit 2	VDD_{MEM}
DQ3	IO	A4	Bi-dir, Single-end	DQ3: DDR data bus bit 3	VDD_{MEM}
DQ4	IO	B5	Bi-dir, Single-end	DQ4: DDR data bus bit 4	VDD_{MEM}
DQ5	IO	C6	Bi-dir, Single-end	DQ5: DDR data bus bit 5	VDD_{MEM}
DQ6	IO	B6	Bi-dir, Single-end	DQ6: DDR data bus bit 6	VDD_{MEM}
DQ7	IO	C7	Bi-dir, Single-end	DQ7: DDR data bus bit 7	VDD_{MEM}
DQ8	IO	A7	Bi-dir, Single-end	DQ8: DDR data bus bit 8	VDD_{MEM}
DQ9	IO	C8	Bi-dir, Single-end	DQ9: DDR data bus bit 9	VDD_{MEM}
DQ10	IO	B8	Bi-dir, Single-end	DQ10: DDR data bus bit 10	VDD_{MEM}
DQ11	IO	A8	Bi-dir, Single-end	DQ11: DDR data bus bit 11	VDD_{MEM}
DQ12	IO	A10	Bi-dir, Single-end	DQ12: DDR data bus bit 12	VDD_{MEM}
DQ13	IO	B10	Bi-dir, Single-end	DQ13: DDR data bus bit 13	VDD_{MEM}
DQ14	IO	C10	Bi-dir, Single-end	DQ14: DDR data bus bit 14	VDD_{MEM}
DQ15	IO	C11	Bi-dir, Single-end	DQ15: DDR data bus bit 15	VDD_{MEM}
DQ16	IO	B12	Bi-dir, Single-end	DQ16: DDR data bus bit 16	VDD_{MEM}
DQ17	IO	C12	Bi-dir, Single-end	DQ17: DDR data bus bit 17	VDD_{MEM}
DQ18	IO	C13	Bi-dir, Single-end	DQ18: DDR data bus bit 18	VDD_{MEM}
DQ19	IO	B13	Bi-dir, Single-end	DQ19: DDR data bus bit 19	VDD_{MEM}
DQ20	IO	C14	Bi-dir, Single-end	DQ20: DDR data bus bit 20	VDD_{MEM}
DQ21	IO	A15	Bi-dir, Single-end	DQ21: DDR data bus bit 21	VDD_{MEM}
DQ22	IO	B15	Bi-dir, Single-end	DQ22: DDR data bus bit 22	VDD_{MEM}
DQ23	IO	C15	Bi-dir, Single-end	DQ23: DDR data bus bit 23	VDD_{MEM}
DQ24	IO	C16	Bi-dir, Single-end	DQ24: DDR data bus bit 24	VDD_{MEM}
DQ25	IO	A17	Bi-dir, Single-end	DQ25: DDR data bus bit 25	VDD_{MEM}
DQ26	IO	B17	Bi-dir, Single-end	DQ26: DDR data bus bit 26	VDD_{MEM}
DQ27	IO	C17	Bi-dir, Single-end	DQ27: DDR data bus bit 27	VDD_{MEM}
DQ28	IO	A19	Bi-dir, Single-end	DQ28: DDR data bus bit 28	VDD_{MEM}
DQ29	IO	B19	Bi-dir, Single-end	DQ29: DDR data bus bit 29	VDD_{MEM}
DQ30	IO	A20	Bi-dir, Single-end	DQ30: DDR data bus bit 30	VDD_{MEM}
DQ31	IO	B20	Bi-dir, Single-end	DQ31: DDR data bus bit 31	VDD_{MEM}
A0	O	D7	Output, Single-end	A0: DDR address bus bit 0	VDD_{MEM}
A1	O	D15	Output, Single-end	A1: DDR address bus bit 1	VDD_{MEM}
A2	O	C18	Output, Single-end	A2: DDR address bus bit 2	VDD_{MEM}
A3	O	D16	Output, Single-end	A3: DDR address bus bit 3	VDD_{MEM}
A4	O	E8	Output, Single-end	A4: DDR address bus bit 4	VDD_{MEM}
A5	O	D8	Output, Single-end	A5: DDR address bus bit 5	VDD_{MEM}
A6	O	E9	Output, Single-end	A6: DDR address bus bit 6	VDD_{MEM}
A7	O	D9	Output, Single-end	A7: DDR address bus bit 7	VDD_{MEM}
A8	O	D10	Output, Single-end	A8: DDR address bus bit 8	VDD_{MEM}
A9	O	E10	Output, Single-end	A9: DDR address bus bit 9	VDD_{MEM}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
A10	O	D17	Output, Single-end	A10: DDR address bus bit 10	VDD_{MEM}
A11	O	D14	Output, Single-end	A11: DDR address bus bit 11	VDD_{MEM}
A12	O	D13	Output, Single-end	A12: DDR address bus bit 12	VDD_{MEM}
A13	O	D12	Output, Single-end	A13: DDR address bus bit 13	VDD_{MEM}
A14	O	D11	Output, Single-end	A14: DDR address bus bit 14	VDD_{MEM}
A15	O	E11	Output, Single-end	A15: DDR address bus bit 15	VDD_{MEM}
CSN0	O	C4	Output, Single-end	CSN0: DDR chip select 0	VDD_{MEM}
CSN1	O	E5	Output, Single-end	CSN1: DDR chip select 1	VDD_{MEM}
RASN	O	D18	Output, Single-end	RASN: DDR row address strobe	VDD_{MEM}
CASN	O	E6	Output, Single-end	CASN: DDR column address strobe	VDD_{MEM}
WEN	O	E15	Output, Single-end	WEN: DDR write enable	VDD_{MEM}
DQS0	IO	A5	Bi-dir, Differential	DQS0: DDR data byte 0 strobe positive	VDD_{MEM}
DQS0N	IO	C5	Bi-dir, Differential	DQS0N: DDR data byte 0 strobe negative for differential. Use this pin for differential DQS signal.	VDD_{MEM}
DQS1	IO	C9	Bi-dir, Differential	DQS1: DDR data byte 1 strobe positive	VDD_{MEM}
DQS1N	IO	B9	Bi-dir, Differential	DQS1N: DDR data byte 1 strobe negative for differential.	VDD_{MEM}
DQS2	IO	B14	Bi-dir, Differential	DQS2: DDR data byte 2 strobe positive	VDD_{MEM}
DQS2N	IO	A14	Bi-dir, Differential	DQS2N: DDR data byte 2 strobe negative for differential.	VDD_{MEM}
DQS3	IO	B18	Bi-dir, Differential	DQS3: DDR data byte 3 strobe positive	VDD_{MEM}
DQS3N	IO	A18	Bi-dir, Differential	DQS3N: DDR data byte 3 strobe negative for differential.	VDD_{MEM}
DM0	O	A2	Output, Single-end	DM0: DDR data byte 0 mask	VDD_{MEM}
DM1	O	B7	Output, Single-end	DM1: DDR data byte 1 mask	VDD_{MEM}
DM2	O	A12	Output, Single-end	DM2: DDR data byte 2 mask	VDD_{MEM}
DM3	O	B16	Output, Single-end	DM3: DDR data byte 3 mask	VDD_{MEM}
BA0	O	E7	Output, Single-end	BA0: DDR address bus bank 0	VDD_{MEM}
BA1	O	D6	Output, Single-end	BA1: DDR address bus bank 1	VDD_{MEM}
BA2	O	E14	Output, Single-end	BA2: DDR address bus bank 2	VDD_{MEM}
CK	O	B11	Output, Differential	CK: DDR clock	VDD_{MEM}
CKN	O	A11	Output, Differential	CKN: DDR inverse clock	VDD_{MEM}
CKE	O	D5	Output, Single-end	CKE: DDR clock enable	VDD_{MEM}
ODT0	O	E16	Output, Single-end	ODT0: DDR rank 0 On-die termination (for CSN0)	VDD_{MEM}
RSTN	O	E17	Output, Single-end	RSTN: DDR3 reset pin	VDD_{MEM}
VREF0	AI	F6		VREF0: DDR/DDR2/DDR3 input reference voltage	$VDD_{MEM}/2$
VREF1	AI	E13		VREF1: DDR/DDR2/DDR3 input reference voltage	$VDD_{MEM}/2$
VREF2	AI	F16		VREF2: DDR/DDR2/DDR3 input reference voltage	$VDD_{MEM}/2$
ZQ	AIO	D4		ZQ: DDR3 External reference which is connected to a 240ohm resister to VSSIOm	

2.5.2 BOOT and storage

Table2-2 Static-Memory/MSC0/SPI0/DMA/1WIRE Pins (28; all GPIO shared: PA0~7, PA16~29, PB0~5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 PA0	IO IO	J2	8mA, pullup-pe	SD0: Static memory data bus bit 0 PA0: GPIO group A bit 0	VDDIOn

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD1 PA1	IO IO	J3	8mA, pullup-pe	SD1: Static memory data bus bit 1 PA1: GPIO group A bit 1	VDDIOn
SD2 PA2	IO IO	H1	8mA, pullup-pe	SD2: Static memory data bus bit 2 PA2: GPIO group A bit 2	VDDIOn
SD3 PA3	IO IO	H2	8mA, pullup-pe	SD3: Static memory data bus bit 3 PA3: GPIO group A bit 3	VDDIOn
SD4 MSC0_D4 PA4	IO IO IO	H3	8mA, pullup-pe	SD4: Static memory data bus bit 4 MSC0_D4: MSC (MMC/SD) 0 data bit 4 PA4: GPIO group A bit 4	VDDIOn
SD5 MSC0_D5 PA5	IO IO IO	G2	8mA, pullup-pe	SD5: Static memory data bus bit 5 MSC0_D5: MSC (MMC/SD) 0 data bit 5 PA5: GPIO group A bit 5	VDDIOn
SD6 MSC0_D6 PA6	IO IO IO	H4	8mA, pullup-pe	SD6: Static memory data bus bit 6 MSC0_D6: MSC (MMC/SD) 0 data bit 6 PA6: GPIO group A bit 6	VDDIOn
SD7 MSC0_D7 PA7	IO IO IO	G3	8mA, pullup-pe	SD7: Static memory data bus bit 7 MSC0_D7: MSC (MMC/SD) 0 data bit 7 PA7: GPIO group A bit 7	VDDIOn
SA0 (CL) PB0	O IO	E3	8mA, pulldown-pe, rst-pe	SA1: Static memory address bus bit 0 If NAND flash is used, this pin is used as NAND CL (command latch) pin PB0: GPIO group B bit 0	VDDIOn
SA1 (AL) PB1	O IO	D2	8mA, pulldown-pe, rst-pe	SA1: Static memory address bus bit 1 If NAND flash is used, this pin is used as NAND AL (address latch) pin PB1: GPIO group B bit 1	VDDIOn
SA2 PB2	O IO	C2	8mA, pullup-pe	SA2: Static memory address bus bit 2 PB2: GPIO group B bit 2	VDDIO
SA3 PB3	O IO	B1	8mA, pullup-pe	SA3: Static memory address bus bit 3 PB3: GPIO group B bit 3	VDDIO
SA4 PB4	O IO	G5	8mA, pullup-pe	SA4: Static memory address bus bit 4 PB4: GPIO group B bit 4	VDDIO
SA5 SSI0_CLK PB5(FRB1)	O O IO	F4	8mA, pullup-pe	SA5: Static memory address bus bit 5 SSI0_CLK: SSI 0 clock output PB5: GPIO group B bit 5. NAND flash FRB input 1 candidate	VDDIO
RD_ PA16	O IO	B2	8mA, pullup-pe, rst-pe	RD_: Static memory read strobe PA16: GPIO group A bit 16	VDDIO
WE_ PA17	O IO	C3	8mA, pullup-pe, rst-pe	WE_: Static memory write strobe PA17: GPIO group A bit 17	VDDIO
FRE_ MSC0_CLK SSI0_CLK PA18	O O O IO	C1	8mA, pullup-pe, rst-pe	FRE_: NAND read enable MSC0_CLK: MSC (MMC/SD) 0 clock output SSI0_CLK: SSI 0 clock output PA18: GPIO group A bit 18	VDDIOn
FWE_ MSC0_CMD SSI0_DT PA19	O O O IO	D1	8mA, pullup-pe, rst-pe	FWE_: NAND write enable MSC0_CMD: MSC (MMC/SD) 0 command SSI0_DT: SSI 0 data output PA19: GPIO group A bit 19	VDDIOn
MSC0_D0 SSI0_DR PA20(FRB0)	IO I IO	E2	8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SSI0_DR: SSI 0 data input PA20: GPIO group A bit 20. NAND flash FRB (ready/busy) input 0	VDDIOn
CS1_ MSC0_D1 SSI0_DT PA21	O IO IO	F3	8mA, pullup-pe, rst-pe	CS1_: NAND/NOR/SRAM chip select 1 MSC0_D1: MSC (MMC/SD) 0 data bit 1 SSI0_DT: SSI 0 data output PA21: GPIO group A bit 21	VDDIOn
CS2_ MSC0_D2 PA22	O IO IO	G4	8mA, pullup-pe, rst-pe	CS2_: NAND/NOR/SRAM chip select 2 MSC0_D2: MSC (MMC/SD) 0 data bit 2 PA22: GPIO group A bit 22	VDDIOn

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CS3_ MSC0_D3 SSI0_CE0_ PA23(FRB1)	O IO O IO	E1	8mA, pullup-pe, rst-pe	CS3_: NAND/NOR/SRAM chip select 3 MSC0_D3: MSC (MMC/SD) 0 data bit 3 SSI0_CE0_: SSI0 chip enable 0 PA23: GPIO group A bit 23. NAND flash FRB input 1 candidate	VDDIOn
CS4_ MSC0_RST_ PA24	O O IO	F2	8mA, pullup-pe, rst-pe	CS4_: NAND/NOR/SRAM chip select 4 MSC0_RST_: MSC0 Reset output PA24: GPIO group A bit 24	VDDIOn
CS5_ SSI0_CE0_ PA25	O O IO	A1	8mA, pullup-pe, rst-pe	CS5_: NAND/NOR/SRAM chip select 5 SSI0_CE0_: SSI0 chip enable 0 PA25: GPIO group A bit 25	VDDIO
CS6_ RDWR_ PA26(FRB1)	O O IO	F5	8mA, pullup-pe, rst-pe	CS6_: NAND/NOR/SRAM chip select 6 RDWR_: Static memory access indicator, 1 for read and 0 for write PA26: GPIO group A bit 26. NAND flash FRB input 1 candidate	VDDIO
WAIT_ SSI0_DR PA27(FRB1)	I I IO	E4	8mA, pullup-pe	WAIT_: Slow static memory/device wait signal SSI0_DR: SSI 0 data input PA27: GPIO group A bit 27. NAND flash FRB input 1 candidate	VDDIO
SSI0_DT PA28(FRB1)	O IO	D3	8mA, pullup-pe	SSI0_DT: SSI 0 data output PA28: GPIO group A bit 28. NAND flash FRB input 1 candidate	VDDIO
NDQS PA29	IO IO	G1	8mA, pullup-pe	NDQS: NAND DQS signal PA29: GPIO group A bit 29	VDDIOn

2.5.3 LCD

Table 2-3 LCDC Pins (28; all GPIO shared: PC0~27)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_B0 LCD_REV PC0	O O IO	J18	8mA, pullup-pe	LCD_B0: LCD Blue data bit 0 LCD_REV: LCD REV output for special TFT PC0: GPIO group C bit 0	VDDIO
LCD_B1 LCD_PS PC1	O O IO	H19	8mA, pullup-pe	LCD_B1: LCD Blue data bit 1 LCD_PS: LCD PS output for special TFT PC1: GPIO group C bit 1	VDDIO
LCD_B2 PC2	O IO	G21	8mA, pullup-pe	LCD_B2: LCD Blue data bit 2 PC2: GPIO group C bit 2	VDDIO
LCD_B3 PC3	O IO	G20	8mA, pullup-pe	LCD_B3: LCD Blue data bit 3 PC3: GPIO group C bit 3	VDDIO
LCD_B4 PC4	O IO	H18	8mA, pullup-pe	LCD_B4: LCD Blue data bit 4 PC4: GPIO group C bit 4	VDDIO
LCD_B5 PC5	O IO	G19	8mA, pullup-pe	LCD_B5: LCD Blue data bit 5 PC5: GPIO group C bit 5	VDDIO
LCD_B6 PC6	O IO	F20	8mA, pullup-pe	LCD_B6: LCD Blue data bit 6 PC6: GPIO group C bit 6	VDDIO
LCD_B7 PC7	O IO	E21	8mA, pullup-pe	LCD_B7: LCD Blue data bit 7 PC7: GPIO group C bit 7	VDDIO
LCD_PCLK PC8	O IO	H21	8mA, pullup-pe	LCD_PCLK: LCD pixel clock PC8: GPIO group C bit 8	VDDIO
LCD_DE PC9	O IO	J19	8mA, pullup-pe	LCD_DE: STN AC bias drive/non-STN data enable PC9: GPIO group C bit 9	VDDIO
LCD_G0 LCD_SPL UART4_TxD PC10	O O O IO	G18	8mA, pullup-pe, rst-pe	LCD_G0: LCD Green data bit 0 LCD_SPL: LCD SPL output UART4_TxD: UART 4 transmitting data PC10: GPIO group C bit 10	VDDIO
LCD_G1 PC11	O IO	F19	8mA, pullup-pe	LCD_G1: LCD Green data bit 1 PC11: GPIO group C bit 11	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LCD_G2 PC12	O IO	E20	8mA, pullup-pe	LCD_G2: LCD Green data bit 2 PC12: GPIO group C bit 12	VDDIO
LCD_G3 PC13	O IO	D21	8mA, pullup-pe	LCD_G3: LCD Green data bit 3 PC13: GPIO group C bit 13	VDDIO
LCD_G4 PC14	O IO	F18	8mA, pullup-pe	LCD_G4: LCD Green data bit 4 PC14: GPIO group C bit 14	VDDIO
LCD_G5 PC15	O IO	G17	8mA, pullup-pe	LCD_G5: LCD Green data bit 5 PC15: GPIO group C bit 15	VDDIO
LCD_G6 PC16	O IO	E19	8mA, pullup-pe	LCD_G6: LCD Green data bit 6 PC16: GPIO group C bit 16	VDDIO
LCD_G7 PC17	O IO	D20	8mA, pullup-pe	LCD_G7: LCD Green data bit 7 PC17: GPIO group C bit 17	VDDIO
LCD_HSYN PC18	IO IO	H20	8mA, pullup-pe	LCD_HSYN: LCD line clock/horizonal sync PC18: GPIO group C bit 18	VDDIO
LCD_VSYN PC19	IO IO	J20	8mA, pullup-pe	LCD_VSYN: LCD frame clock/vertical sync PC19: GPIO group C bit 19	VDDIO
LCD_R0 LCD_CLS UART4_RxD PC20	O O I IO	C21	8mA, pullup-pe	LCD_R0: LCD Red data bit 0 LCD_CLS: LCD CLS output UART4_RxD: UART 4 Receiving data PC20: GPIO group C bit 20	VDDIO
LCD_R1 PC21	O IO	B21	8mA, pullup-pe	LCD_R1: LCD Red data bit 1 PC21: GPIO group C bit 21	VDDIO
LCD_R2 PC22	O IO	C20	8mA, pullup-pe	LCD_R2: LCD Red data bit 2 PC22: GPIO group C bit 22	VDDIO
LCD_R3 PC23	O IO	E18	8mA, pullup-pe	LCD_R3: LCD Red data bit 3 PC23: GPIO group C bit 23	VDDIO
LCD_R4 PC24	O IO	D19	8mA, pullup-pe	LCD_R4: LCD Red data bit 4 PC24: GPIO group C bit 24	VDDIO
LCD_R5 PC25	O IO	A21	8mA, pullup-pe	LCD_R5: LCD Red data bit 5 PC25: GPIO group C bit 25	VDDIO
LCD_R6 PC26	O IO	F17	8mA, pullup-pe	LCD_R6: LCD Red data bit 6 PC26: GPIO group C bit 26	VDDIO
LCD_R7 PC27	O IO	C19	8mA, pullup-pe	LCD_R7: LCD Red data bit 7 PC27: GPIO group C bit 27	VDDIO

2.5.4 GPIO

Table 2-4 GPIO Pins (12; all GPIO shared: PF4~15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PF4	IO	U9	8mA, pulldown-pe	PF4: GPIO group F bit 4. Pull-down not enabled at and after reset	VDDIO
PF5	IO	U10	8mA, pulldown-pe	PF5: GPIO group F bit 5. Pull-down not enabled at and after reset	VDDIO
PF6	IO	U11	8mA, pulldown-pe	PF6: GPIO group F bit 6. Pull-down not enabled at and after reset	VDDIO
PF7	IO	U12	8mA, pulldown-pe	PF7: GPIO group F bit 7. Pull-down not enabled at and after reset	VDDIO
PF8	IO	R10	8mA, pulldown-pe	PF8: GPIO group F bit 8. Pull-down not enabled at and after reset	VDDIO
PF9	IO	M4	8mA, pulldown-pe	PF9: GPIO group F bit 9. Pull-down not enabled at and after reset	VDDIO
PF10	IO	L4	8mA, pulldown-pe	PF10: GPIO group F bit 10. Pull-down not enabled at and after reset	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PF11	IO	R4	8mA, pulldown-pe	PF11: GPIO group F bit 11. Pull-down not enabled at and after reset	VDDIO
PF12	IO	N5	8mA, pullup-pe	PF12: GPIO group F bit 12	VDDIO
PF13	IO	U13	8mA, pullup-pe	PF13: GPIO group F bit 13	VDDIO
PF14	IO	R12	8mA, pullup-pe	PF14: GPIO group F bit 14	VDDIO
PF15	IO	R11	8mA, pullup-pe	PF15: GPIO group F bit 15	VDDIO

2.5.5 CIM

Table 2-5 CIM/SMB2/DMIC/TSSI1 Pins (16; all GPIO shared: PB6~19, PF16~17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CIM_PCLK PB6	I IO	AA4	8mA, pullup-pe	CIM_PCLK: CIM pixel clock input PB6: GPIO group B bit 6	VDDIOc
CIM_HSYN PB7	I O	AA5	8mA, pullup-pe	CIM_HSYN: CIM horizonal sync input PB7: GPIO group B bit 7	VDDIOc
CIM_VSYN PB8	I IO	Y5	8mA, pullup-pe	CIM_VSYN: CIM vertical sync input PB8: GPIO group B bit 8	VDDIOc
CIM_MCLK PB9	O IO	Y6	8mA, pullup-pe	CIM_MCLK: CIM master clock output PB9: GPIO group B bit 9	VDDIOc
CIM_D0 PB10	I IO	W3	8mA, pulldown-pe	CIM_D0: CIM data input bit 0. When use 8-bit data, use CIM_D0~D7 PB10: GPIO group B bit 10	VDDIOc
CIM_D1 PB11	I IO	AA2	8mA, pulldown-pe	CIM_D1: CIM data input bit 1 PB11: GPIO group B bit 11	VDDIOc
CIM_D2 PB12	I IO	W4	8mA, pullup-pe	CIM_D2: CIM data input bit 2 PB12: GPIO group B bit 12	VDDIOc
CIM_D3 PB13	I IO	Y3	8mA, pullup-pe	CIM_D3: CIM data input bit 3 PB13: GPIO group B bit 13	VDDIOc
CIM_D4 PB14	I IO	Y4	8mA, pullup-pe	CIM_D4: CIM data input bit 4 PB14: GPIO group B bit 14	VDDIOc
CIM_D5 PB15	I IO	AA3	8mA, pullup-pe	CIM_D5: CIM data input bit 5 PB15: GPIO group B bit 15	VDDIOc
CIM_D6 PB16	I IO	W5	8mA, pulldown-pe	CIM_D6: CIM data input bit 6 PB16: GPIO group B bit 16	VDDIOc
CIM_D7 PB17	I IO	U6	8mA, pulldown-pe	CIM_D7: CIM data input bit 7 PB17: GPIO group B bit 17	VDDIOc
DMIC_CLK PB18	O IO	W6	8mA, pulldown-pe	DMIC_CLK: Digital MIC clock output PB18: GPIO group B bit 18	VDDIOc
DMIC_IN PB19	I IO	V6	8mA, p pulldown-pe	DMIC_IN: Digital MIC input PB19: GPIO group B bit 19	VDDIOc
SMB2_SDA PF16	IO IO	V7	8mA, pullup-pe	SMB2_SDA: SMB 2 serial data PF16: GPIO group F bit 16	VDDIOc
SMB2_SCK PF17	O IO	W7	8mA, pullup-pe	SMB2_SCK: SMB 2 serial clock PF17: GPIO group F bit 17	VDDIOc

2.5.6 3G/M-DTV

Table 2-6 TSSI/MSC2/SSI Pins (12; all GPIO shared: PB20~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC2_D0 SSI0_DR SSI1_DR TSDI0 PB20	IO I I I IO	T2	8mA, pullup-pe	MSC2_D0: MSC (MMC/SD) 2 data bit 0 SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input TSDI0: TS slave interface input data bus bit 0 PB20: GPIO group B bit 20	VDDIO
MSC2_D1 SSI0_CE1_ SSI1_CE1_ TSDI1 PB21	IO O O I IO	T3	8mA, pullup-pe	MSC2_D1: MSC (MMC/SD) 2 data bit 1 SSI0_CE1_: SSI 0 chip select 1 SSI1_CE1_: SSI 1 chip select 1 TSDI1: TS interface input data bus bit 1 PB21: GPIO group B bit 21	VDDIO
TSDI2 PB22	I IO	V3	8mA, pullup-pe	TSDI2: TS interface input data bus bit 2 PB22: GPIO group B bit 22	VDDIO
TSDI3 PB23	I IO	U4	8mA, pullup-pe	TSDI3: TS interface input data bus bit 3 PB23: GPIO group B bit 23	VDDIO
TSDI4 PB24	I IO	V4	8mA, pullup-pe	TSDI4: TS interface input data bus bit 4 PB24: GPIO group B bit 24	VDDIO
TSDI5 PB25	I IO	T5	8mA, pullup-pe	TSDI5: TS interface input data bus bit 5 PB25: GPIO group B bit 25	VDDIO
TSDI6 PB26	I IO	U5	8mA, pullup-pe	TSDI6: TS interface input data bus bit 6 PB26: GPIO group B bit 26	VDDIO
TSDI7 PB27	I IO	V5	8mA, pullup-pe	TSDI7: TS interface input data bus bit 7 PB27: GPIO group B bit 27	VDDIO
MSC2_CLK SSI0_CLK SSI1_CLK TSCLK PB28	O O O I IO	P1	8mA, pullup-pe	MSC2_CLK: MSC (MMC/SD) 2 clock output SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output TSCLK: TS interface clock input PB28: GPIO group B bit 28	VDDIO
MSC2_CMD SSI0_DT SSI1_DT TSSTR PB29	IO O O I IO	R1	8mA, pullup-pe, rst-pe	MSC2_CMD: MSC (MMC/SD) 2 command SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output TSSTR: TS interface frame start input PB29: GPIO group B bit 29	VDDIO
MSC2_D2 SSI0_GPC SSI1_GPC TSFAIL PB30	IO O O I IO	R2	8mA, pullup-pe	MSC2_D2: MSC (MMC/SD) 2 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal TSFAIL: TS interface error package indicator input PB30: GPIO group B bit 30	VDDIO
MSC2_D3 SSI0_CE0_ SSI1_CE0_ TSFRM PB31	IO O O I IO	R3	8mA, pullup-pe, rst-pe	MSC2_D3: MSC (MMC/SD) 2 data bit 3 SSI0_CE1_: SSI 0 chip enable 0 SSI1_CE1_: SSI 1 chip enable 0 TSFRM: TS interface frame valid input PB31: GPIO group B bit 31	VDDIO

2.5.7 GPS

Table 2-7 UART0/GPSBB Pins (4; all GPIO shared: PF0~3)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RxD GPS_CLK PF0	I I IO	AA11	8mA, pullup-pe	UART0_RxD: UART 0 Receiving data GPS_CLK: GPS baseband clock input from RF PF0: GPIO group F bit 0	VDDIO
UART0_CTS_ GPS_MAG PF1	I I IO	AA12	8mA, pullup-pe, rst-pe	UART0_CTS_: UART 0 CTS_ input GPS_MAG: GPS baseband MAG input from RF PF1: GPIO group F bit 1	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART0_RTS_ GPS_SIG PF2	O I IO	Y11	8mA, pullup-pe, rst-pe	UART0_RTS_: UART 0 RTS_ output GPS_SIG: GPS baseband SIG input from RF PF2: GPIO group F bit 2	VDDIO
UART0_TxD PF3	O IO	Y12	8mA, pullup-pe, rst-pe	UART0_TxD: UART 0 transmitting data PF3: GPIO group F bit 3	VDDIO

2.5.8 WIFI

Table 2-8 MSC1/SSI0/SSI1, Pins (6; all GPIO shared: PD20~25)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_D0 SSI0_DR SSI1_DR PD20	IO I I IO	Y7	8mA, pullup-pe	MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input PD20: GPIO group D bit 20	VDDIO
MSC1_D1 SSI0_CE1_ SSI1_CE1_ PD21	IO O O IO	AA7	8mA, pullup-pe	MSC1_D1: MSC (MMC/SD) 1 data bit 1 SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 PD21: GPIO group D bit 21	VDDIO
MSC1_D2 SSI0_GPC SSI1_GPC PD22	IO O O IO	AA8	8mA, pullup-pe	MSC1_D2: MSC (MMC/SD) 1 data bit 2 SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal PD22: GPIO group D bit 22	VDDIO
MSC1_D3 SSI0_CE0_ SSI1_CE0_ PD23	IO O O IO	W8	8mA, pullup-pe, rst-pe	MSC1_D3: MSC (MMC/SD) 1 data bit 3 SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 PD23: GPIO group D bit 23	VDDIO
MSC1_CLK SSI0_CLK SSI1_CLK PD24	O O O IO	Y8	8mA, pullup-pe	MSC1_CLK: MSC (MMC/SD) 1 clock output SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output PD24: GPIO group D bit 24	VDDIO
MSC1_CMD SSI0_DT SSI1_DT PD25	IO O O IO	Y9	8mA, pullup-pe, rst-pe	MSC1_CMD: MSC (MMC/SD) 1 command SSI0_DT: SSI 0 data output SSI1_DT: SSI 0 data output PD25: GPIO group D bit 25	VDDIO

2.5.9 Phone baseband

Table 2-9 UART1 Pins (4; all GPIO shared: PD26~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
UART1_RxD PD26	I IO	V13	8mA, pullup-pe	UART1_RxD: UART 1 Receiving data PD26: GPIO group D bit 26	VDDIO
UART1_CTS_ PD27	I IO	V12	8mA, pullup-pe	UART1_CTS_: UART 1 CTS_ input PD27: GPIO group D bit 27	VDDIO
UART1_TxD PD28	O IO	W12	8mA, pullup-pe, rst-pe	UART1_TxD: UART 1 transmitting data PD28: GPIO group D bit 28	VDDIO
UART1_RTS_ PD29	O IO	V11	8mA, pullup-pe, rst-pe	UART1_RTS_: UART 1 RTS_ output PD29: GPIO group D bit 29	VDDIO

2.5.10 SMB

Table 2-10 SMB0/SMB1 Pins (4; all GPIO shared: PD30~31, PE30~31)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SMB0_SDA PD30	IO IO	L1	8mA, pullup-pe	SMB0_SDA: SMB 0 serial data PD30: GPIO group D bit 30	VDDIO
SMB0_SCK PD31	IO IO	K1	8mA, pullup-pe	SMB0_SCK: SMB 0 serial clock PD31: GPIO group D bit 31	VDDIO
SMB1_SDA PE30	IO IO	K3	8mA, pullup-pe	SMB1_SDA: SMB 1 serial data PE30: GPIO group E bit 30	VDDIO
SMB1_SCK PE31	IO IO	K2	8mA, pullup-pe	SMB1_SCK: SMB 1 serial clock PE31: GPIO group E bit 31	VDDIO

2.5.11 MSCx

Table 2-11 MSCx (6; all GPIO shared: PE20~23, PE28~29)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_CLK MSC1_CLK MSC2_CLK PE28	O O O IO	V19	8mA, pullup-pe	MSC0_CLK: MSC (MMC/SD) 0 clock output MSC1_CLK: MSC (MMC/SD) 1 clock output MSC2_CLK: MSC (MMC/SD) 2 clock output PE28: GPIO group E bit 28	VDDIOs
MSC0_CMD MSC1_CMD MSC2_CMD PE29	IO IO IO IO	V21	8mA, pullup-pe	MSC0_CMD: MSC (MMC/SD) 0 command MSC1_CMD: MSC (MMC/SD) 1 command MSC2_CMD: MSC (MMC/SD) 2 command PE29: GPIO group E bit 29	VDDIOs
MSC0_D0 MSC1_D0 MSC2_D0 PE20	IO IO IO IO	T17	8mA, pullup-pe	MSC0_D0: MSC (MMC/SD) 0 data bit 0 MSC1_D0: MSC (MMC/SD) 1 data bit 0 MSC2_D0: MSC (MMC/SD) 2 data bit 0 PE20: GPIO group E bit 20	VDDIOs
MSC0_D1 MSC1_D1 MSC2_D1 PE21	IO IO IO IO	V18	8mA, pullup-pe	MSC0_D1: MSC (MMC/SD) 0 data bit 1 MSC1_D1: MSC (MMC/SD) 1 data bit 1 MSC2_D1: MSC (MMC/SD) 2 data bit 1 PE21: GPIO group E bit 21	VDDIOs
MSC0_D2 MSC1_D2 MSC2_D2 PE22	IO IO IO IO	V20	8mA, pullup-pe	MSC0_D2: MSC (MMC/SD) 0 data bit 2 MSC1_D2: MSC (MMC/SD) 1 data bit 2 MSC2_D2: MSC (MMC/SD) 2 data bit 2 PE22: GPIO group E bit 22	VDDIOs
MSC0_D3 MSC1_D3 MSC2_D3 PE23	IO IO IO IO	U18	8mA, pullup-pe	MSC0_D3: MSC (MMC/SD) 0 data bit 3 MSC1_D3: MSC (MMC/SD) 1 data bit 3 MSC2_D3: MSC (MMC/SD) 2 data bit 3 PE23: GPIO group E bit 23	VDDIOs

2.5.12 SPIx

Table 2-12 SSI0/SSI1 Pins (6/0; all GPIO shared: PE14~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_DR SSI1_DR PE14	I I IO	R5	8mA, pullup-pe	SSI0_DR: SSI 0 data input SSI1_DR: SSI 1 data input PE14: GPIO group E bit 14	VDDIO
SSI0_CLK SSI1_CLK PE15	O O IO	P5	8mA, pullup-pe	SSI0_CLK: SSI 0 clock output SSI1_CLK: SSI 1 clock output PE15: GPIO group E bit 15	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SSI0_CE0_ SSI1_CE0_ PE16	O O IO	T4	8mA, pullup-pe, rst-pe	SSI0_CE0_: SSI 0 chip enable 0 SSI1_CE0_: SSI 1 chip enable 0 PE16: GPIO group E bit 16	VDDIO
SSI0_DT SSI1_DT PE17	O O IO	P4	8mA, pullup-pe	SSI0_DT: SSI 0 data output SSI1_DT: SSI 1 data output PE17: GPIO group E bit 17	VDDIO
SSI0_CE1_ SSI1_CE1_ PE18	O O IO	N4	8mA, pullup-pe, rst-pe	SSI0_CE1_: SSI 0 chip enable 1 SSI1_CE1_: SSI 1 chip enable 1 PE18: GPIO group E bit 18	VDDIO
SSI0_GPC SSI1_GPC PE19	O O IO	M5	8mA, pullup-pe	SSI0_GPC: SSI 0 general-purpose control signal SSI1_GPC: SSI 1 general-purpose control signal PE19: GPIO group E bit 19	VDDIO

2.5.13 BlueTooth/PCM0/PS2

Table 2-13 BlueTooth/PCM0/PS2 Pins (10; all GPIO shared: PD0~9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PCM0_DO PD0	O IO	W9	8mA, pullup-pe	PCM0_DO: PCM 0 data out PD0: GPIO group D bit 0	VDDIO
PCM0_CLK PD1	IO IO	AA10	8mA, pullup-pe	PCM0_CLK: PCM 0 clock PD1: GPIO group D bit 1	VDDIO
PCM0_SYN PD2	IO IO	Y10	8mA, pullup-pe	PCM0_SYN: PCM 0 sync PD2: GPIO group D bit 2	VDDIO
PCM0_DI PD3	I IO	W10	8mA, pullup-pe	PCM0_DI: PCM 0 data in PD3: GPIO group D bit 3	VDDIO
UART2_RTS_ PS2_MCLK PD4	O IO IO	U7	8mA, pullup-pe	UART2_RTS_: UART 2 RTS_ output PS2_MCLK: PS/2 mouse clock PD4: GPIO group D bit 4	VDDIO
UART2_CTS_ PS2_MDATA PD5	I IO IO	U8	8mA, pullup-pe	UART2_CTS_: UART 2 CTS_ input PS2_MDATA: PS/2 mouse data PD5: GPIO group D bit 5	VDDIO
UART2_RxD PS2_KCLK PD6	I IO IO	V8	8mA, pullup-pe	UART2_RxD: UART 2 Receiving data PS2_KCLK: PS/2 keyboard clock PD6: GPIO group D bit 6	VDDIO
UART2_TxD PS2_KDATA PD7	O IO IO	V9	8mA, pullup-pe	UART2_TxD: UART 2 transmitting data PS2_KDATA: PS/2 keyboard data PD7: GPIO group D bit 7	VDDIO
PD8	IO	V10	8mA, pullup-pe	PD8: GPIO group D bit 8	VDDIO
PD9	IO	W11	8mA, pullup-pe	PD9: GPIO group D bit 9	VDDIO

2.5.14 PWM/AIC/UART3

Table 2-14 PWM/AIC/UART3 Pins (16; all GPIO shared: PE0~9, PE12~13, PD10~13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM0 PE0	IO IO	N17	8mA, pulldown-pe	PWM0: PWM output or pulse input 0 PE0: GPIO group E bit 0. Pull-down not enabled at and after reset	VDDIO
PWM1 PE1	O IO	N18	8mA, pulldown-pe	PWM1: PWM 1 output. This PWM can run in sleep mode in RTCLK clock PE1: GPIO group E bit 1. Pull-down not enabled at and after reset	VDDIO

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PWM2 PE2	O IO	V14	8mA, pullup-pe	PWM2: PWM 2 output. This PWM can run in sleep mode in RTCLK clock PE2: GPIO group E bit 2. Pull-up not enabled at and after reset	VDDIO
PWM3 SMB4_SDA PE3	IO IO IO	L3	8mA, pullup-pe	PWM3: PWM output or pulse input 3 SMB4_SDA: SMB 4 serial data PE3: GPIO group E bit 3. Pull-up not enabled at and after reset	VDDIO
PWM4 SMB4_SCK PE4	IO IO IO	K7	8mA, pullup-pe	PWM4: PWM output or pulse input 4 SMB4_SCK: SMB 4 serial clock PE4: GPIO group E bit 4	VDDIO
PWM5 UART3_TxD SCLK_RSTN PE5	IO O O IO	R17	8mA, pullup-pe, rst-pe	PWM5: PWM output or pulse input 5 UART3_TxD: UART 3 transmitting data SCLK_RSTN: AIC0 I2S system clock output or AC97 reset output PE5: GPIO group E bit 5	VDDIO
PWM6 SMB3_SDA PD10	IO IO IO	M1	8mA, pullup-pe	PWM6: PWM output or pulse input 6 SMB3_SDA: SMB 3 serial data PD10: GPIO group D bit 10	VDDIO
PWM7 SMB3_SCK PD11	IO IO IO	L2	8mA, pullup-pe	PWM7: PWM output or pulse input 7 SMB3_SCK: SMB 3 serial clock PD11: GPIO group D bit 11	VDDIO
UART3_RxD BCLK0 PD12	I IO IO	R18	8mA, pulldown-pe	UART3_RxD: UART 3 Receiving data BCLK0: AIC AC97 bit clock/I2S unified or DAC bit clock PD12: GPIO group D bit 12	VDDIO
LRCLK0 PD13	IO IO	T18	8mA, pulldown-pe	LRCLK0: AIC AC97 frame SYNC/I2S unified or DAC Left/Right clock PD13: GPIO group D bit 13	VDDIO
AIC_SDATI PE6	I IO	U19	8mA, pullup-pe	AIC_SDATI: AIC AC97/I2S serial data input PE6: GPIO group E bit 6	VDDIO
AIC0_SDATO PE7	O IO	T19	8mA, pulldown-pe	AIC0_SDATO: AIC AC97/I2S serial data output or SPDIF output PE7: GPIO group E bit 7	VDDIO
UART3_CTS_ BCLK_AD PE8	I IO IO	P18	8mA, pullup-pe	UART3_CTS_: UART 3 CTS_ input BCLK_AD: AIC I2S ADC bit clock PE8: GPIO group E bit 8	VDDIO
UART3_RTS_ LRCLK_AD PE9	O IO O	P17	8mA, pullup-pe, rst-pe	UART3_RTS_: UART 3 RTS_ output LRCLK_AD: AIC I2S ADC Left/Right clock PE9: GPIO group E bit 9	VDDIO
SMB4_SDA PE12	IO IO	L5	8mA, pullup-pe	SMB4_SDA: SMB 4 serial data PE12: GPIO group E bit 12	VDDIO
SMB4_SCK PE13	IO IO	M2	8mA, pullup-pe	SMB4_SCK: SMB 4 serial clock PE13: GPIO group E bit 13	VDDIO

Table 2-15 GPIO Pins (5: PF18~22)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PF18	IO	P3	8mA, pullup-pe	PF18: GPIO group F bit 18	VDDIO
PF19	IO	P2	8mA, pulldown-pe	PF19: GPIO group F bit 19	VDDIO
PF20	IO	N3	8mA, pulldown-pe	PF20: GPIO group F bit 20	VDDIO
PF21	IO	N2	8mA, pullup-pe	PF21: GPIO group F bit 21	VDDIO
PF22	IO	M3	8mA, pulldown-pe	PF22: GPIO group F bit 22	VDDIO

2.5.15 System/JTAG/UART3(DEBUG Used)

Table 2-16 JTAG/UART3/PS2 Pins (5, GPIO PA30~31 are used to control)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST_	I	K5	Schmitt, pull-down	TRST_: JTAG reset	VDDIO
TCK UART3_RTS_ PS2_MCLK	I O IO	H5	8mA, Schmitt, pulldown-pe, rst-pe	TCK: JTAG clock UART3_RTS_: UART 3 RTS_ output PS2_MCLK: PS/2 mouse clock PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO
TMS UART3_CTS_ PS2_MDATA	I I IO	J5	8mA, Schmitt, pullup-pe, rst-pe	TMS: JTAG mode select UART3_CTS_: UART 3 CTS_ input PS2_MDATA: PS/2 mouse data PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO
TDI UART3_RxD PS2_KCLK	I I IO	J4	8mA, Schmitt, pullup-pe, rst-pe	TDI: JTAG serial data input UART3_RxD: UART 3 Receiving data PS2_KCLK: PS/2 keyboard clock PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO
TDO UART3_TxD PS2_KDATA	O O IO	K4	8mA, Schmitt, pullup-pe, rst-pe	TDO: JTAG serial data output UART3_TxD: UART 3 transmitting data PS2_KDATA: PS/2 keyboard data PA30 is used to select between JTAG and PS2, PA31 is used to select between JTAG and UART and control the pull-down enable	VDDIO

Table 2-17 System Pins (3, all GPIO shared: PD17~19)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PD17 (BOOT_SEL0)	IO I	U15	8mA, pullup-pe	PD17: GPIO group D bit 17 It is taken as BOOT select bit 0 by Boot ROM code	VDDIO
PD18 (BOOT_SEL1)	IO I	U14	8mA, pullup-pe	PD18: GPIO group D bit 18 It is taken as BOOT select bit 1 by Boot ROM code	VDDIO
PD19 (BOOT_SEL2)	IO I	T15	8mA, pullup-pe	PD19: GPIO group D bit 19 It is taken as BOOT select bit 2 by Boot ROM code	VDDIO

Table 2-18 USB OTG Digital Pins (1, all GPIO shared: PE10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DRVVBUS PE10	O IO	V15	8mA, pulldown-pe, rst-pe	DRVVBUS: USB OTG VBUS driver control signal PE10: GPIO group E bit 10	VDDIO

Table 2-19 EXCLK output Pins (1, all GPIO shared: PD15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLKO PD15	O IO	W14	8mA, pulldown-pe, rst-pe	EXCLKO: output external clock PD15: GPIO group D bit 15	VDDIO

2.5.16 Digital power/ground

Table 2-20 IO/Core power supplies for FBGAs (66)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDMEM	P	G8 G9 G13 G14 H7 H8 H9 H13 H14 H15		VDDMEM: IO digital power for DRAM, 1.2V~1.8V	-
VSSMEM	P	E12 G7 G10 G11 G12 G15 H10 H11 H12 J15		VSSMEM: IO digital ground for DRAM, 0V	-
VDDIO_NAND	P	L7 M7		VDDIO_NAND: IO digital power for NAND power domain, 1.8V~3.3V	-
VDDIO_CIM	P	T6		VDDIO_CIM: IO digital power for CIM power domain, 1.8V~3.3V	-
VDDIO_MSC	P	R14		VDDIO_MSC: IO digital power for SDcard power domain, 1.8V~3.3V	-
VDDIO	P	M8 N8 P8 P9		VDDIO: IO digital power for none DRAM/NAND, 3.3V	-
VSS	P	J7 J8 J9 J10 J11 J12 J13 J14 K8 K13 K14 L8 L9 L13 L14 M9 M13 M14 N9 N13 N14 P14 R9		VSS: IO digital gound for none DRAM and CORE digital ground, 0V	-
VDD	P	K9 K10 K11 K12 L10 L11 L12 M10 M11 M12 N10 N11 N12 P10 P11		VDD: CORE digital power, 1.1V	-

2.5.17 Analog

Table 2-21 Audio CODEC Pins (15)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CDC_AOHPL	AO	Y18		CDC_AOHPL: Left headphone out	AVD_{CDC}
CDC_AOHPR	AO	AA18		CDC_AOHPR: Right headphone out	AVD_{CDC}
CDC_AOLOP	AO	Y17		CDC_AOLOP: Line out positive	AVD_{CDC}
CDC_AOLON	AO	AA17		CDC_AOLON: Line out negative	AVD_{CDC}
CDC_MICBIAS	AO	W18		CDC_MICBIAS: Microphone bias	AVD_{CDC}
CDC_AIP10	AI	Y21		CDC_AIP10: Single-ended or differential analog input. positive 1	AVD_{CDC}
CDC_AIN10	AI	Y20		CDC_AIN10: Single-ended or differential analog input. negative 1	AVD_{CDC}
CDC_AIP20	AI	W20		CDC_AIP20: Single-ended analog left channel input.	AVD_{CDC}
CDC_AIP30	AI	Y19		CDC_AIP30: Single-ended analog right channel input.	AVD_{CDC}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CDC_VCAP0	AO	AA19		CDC_VCAP0: Voltage Reference Output. An 10μF ceramic or tantalum capacitor in parallel with a 0.1μF ceramic capacitor attached from this pin to AVSCDC eliminates the effects of high frequency noise.	AVD_{CDC}
CDC_HPSENSE0	AI	W17		CDC_HPSENSE0: Sense of headphone jack insertion	AVD_{CDC}
VREFP	P	AA21		VREFP: Internal nLR output	-
AVDCDC	P	W21		AVDCDC: CODEC analog power, 3.3V, internal nLR input.	-
AVSCDC	P	W19		AVSCDC: CODEC analog ground	-
AVSAO_CDC	P	AA20		AVSAO_CDC: CODEC analog ground	

Table 2-22 USB 2.0 OTG, USB 2.0 host (10)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB_DP0	AIO	AA15		USB_DP0: USB OTG data plus	AVD_{USB33}
USB_DM0	AIO	Y15		USB_DM0: USB OTG data minus	AVD_{USB33}
USB_VBUS	AIO	U16		USB_VBUS: USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin	5V
USB_ID	AI	V16		USB_ID: USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDOTG25.	AVD_{USB25}
USB_TXR_RKL	AIO	W15		USB_TXR_RKL: Transmitter resister tune. It connects to an external resistor of 44.2Ω with 1% tolerance to analog ground AVSUSB, that adjusts the USB 2.0 high-speed source impedance	AVD_{USB25}
USB_DP1	AIO	W16		USB_DP1: USB 2.0 host data plus	AVD_{USB33}
USB_DM1	AIO	Y16		USB_DM1: USB 2.0 host data minus	AVD_{USB33}
AVDUSB33	P	P13		AVDUSB33: USB 2.0 host & USB OTG analog power, 3.3V	-
AVDUSB25	P	R13		AVDUSB25: USB OTG analog power, 2.5V	-
AVSUSB	P	P12		AVSUSB: USB analog ground	

Table 2-23 SAR ADC Pins (9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_XP	AIO	K21		ADC_XP: Touch screen input, X+ for 4-wire, bottom-right for 5-wire, or ADC general purpose input	AVD_{AD}
ADC_XM	AIO	K18		ADC_XM: Touch screen input, X- for 4-wire, top-left for 5-wire, or ADC general purpose input	AVD_{AD}
ADC_YP	AIO	K20		ADC_YP: Touch screen input Y+ for 4-wire, top-right for 5-wire, or ADC general purpose input	AVD_{AD}
ADC_YM	AIO	K19		ADC_YM: Touch screen input Y- for 4-wire, bottom-left for 5-wire, or ADC general purpose input	AVD_{AD}
ADC_AUX1	AI	K17		ADC_AUX1: ADC general purpose input	AVD_{AD}
ADC_AUX2	AI	J17		ADC_AUX2: ADC general purpose input or top sheet connection for 5-wire touch screen	AVD_{AD}
ADC_VBAT	AI	L21		ADC_VBAT: Battery voltage input with external resistance divider or ADC general purpose input	1.2V
AVDADC	P	K15		AVDADC: ADC analog power, 3.3 V	-

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVSADC	P	L15		AVSADC: ADC analog ground	-

Table 2-24 EFUSE Pins for Two EFUSE (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
AVDEFUSE	P	H17		AVDEFUSE: EFUSE programming power, 0V/2.5V	AVD_{AD}

Table 2-25 LVDS Pins (14)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
LVDS_CKP LCD_HSYN	AO O	W2		LVDS_CKP: LVDS CLK output positive for LCD LCD_HSYN: LCD line clock/horizonal sync	AVD_{LVDS}
LVDS_CKN LCD_VSYN	AO O	Y1		LVDS_CKN: LVDS CLK output negative for LCD LCD_VSYN: LCD frame clock/vertical sync	AVD_{LVDS}
LVDS_D0N LCD_DE	AO O	U1		LVDS_D0N: LVDS date channel 0 output negative for LCD LCD_DE: STN AC bias drive/non-STN data enable	AVD_{LVDS}
LVDS_D0P LCD_G1	AO O	U2		LVDS_D0P: LVDS date channel 0 output positive for LCD LCD_G1: LCD Green data bit 1	AVD_{LVDS}
LVDS_D1N LCD_G2	AO O	V1		LVDS_D1N: LVDS date channel 1 output negative for LCD LCD_G2: LCD Green data bit 2	AVD_{LVDS}
LVDS_D1P LCD_G3	AO O	U3		LVDS_D1P: LVDS date channel 1 output positive for LCD LCD_G3: LCD Green data bit 3	AVD_{LVDS}
LVDS_D2N LCD_G4	AO O	W1		LVDS_D2N: LVDS date channel 2 output negative for LCD LCD_G4: LCD Green data bit 4	AVD_{LVDS}
LVDS_D2P LCD_G5	AO O	V2		LVDS_D2P: LVDS date channel 2 output positive for LCD LCD_G5: LCD Green data bit 5	AVD_{LVDS}
LVDS_D3N LCD_G6	AO O	AA1		LVDS_D3N: LVDS date channel 3 output negative for LCD LCD_G6: LCD Green data bit 6	AVD_{LVDS}
LVDS_D3P LCD_G7	AO O	Y2		LVDS_D3P: LVDS date channel 3 output positive for LCD LCD_G7: LCD Green data bit 7	AVD_{LVDS}
AVDLVDSPLL	P	R7		AVDLVDSPLL: Power supply for LVDS PLL, 3.3 V	-
AVSLVDSPLL	P	R8		AVSLVDSPLL: Ground for LVDS PLL 3.3V power	-
AVDLVDS	P	P7		AVDLVDS: Power supply for LVDS output, 3.3 V	-
AVSLVDS	P	N7		AVSLVDS: Ground for LVDS output	-

Table 2-26 HDMI Pins (17)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TMDSDATAP[0]	AO	R19		Positive TMDS differential output for data channels 0	AVD_{HDMI}
TMDSDATAN[0]	AO	T20		Negative TMDS differential output for data channels 0	AVD_{HDMI}
TMDSDATAP[1]	AO	R20		Positive TMDS differential output for data channels 1	AVD_{HDMI}
TMDSDATAN[1]	AO	R21		Negative TMDS differential output for data channels 1	AVD_{HDMI}
TMDSDATAP[2]	AO	P20		Positive TMDS differential output for data channels 2	AVD_{HDMI}
TMDSDATAN[2]	AO	P21		Negative TMDS differential output for data channels 2	AVD_{HDMI}
TMDSCLKP	AO	U20		Positive TMDS differential clock output	AVD_{HDMI}

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TMDSCLKN	AO	U21		Negative TMDS differential clock output	AVD_{HDMI}
CEC PF23	O IO	U17		CEC data on CEC bus, 5V tolerance PF23: GPIO group F bit 23	VDDIO
DDCSCK SMB4_SCK PF24	IO IO IO	V17		HDMI SMB clock output, 5V tolerance SMB4_SCK: SMB 4 serial clock PF24: GPIO group F bit 24	VDDIO
DDCSDA SMB4_SDA PF25	IO IO IO	T16		HDMI SMB data inout, 5V tolerance SMB4_SDA: SMB 4 serial data PF25: GPIO group F bit 25	VDDIO
HPD	I	N19		Hot plug detect signal 0-5V	VDDIO
DDCCEC	IO	N20		Ground reference for the Hot plug detect signal, 5V tolerance	VDDIO
REXT	P	P19		Reference resistor 1.6Kohm connection	AVD_{HDMI}
AVDHDMI25	P	R15		Analog power supply 2.5V	
AVDHDMI	P	P15		Analog power supply 1.1V	
AVSHDMI	P	N15		Analog ground	

Table 2-27 CPM Pins (4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XIN	AI	AA14	2~30 MHz Oscillator, OSC on/off	EXCLK_XIN: OSC input or 12MHz clock input	VDD33
EXCLK_XOUT	AO	Y14		EXCLK_XOUT: OSC output	VDD33
AVDPLL	P	Y13		AVDPLL: PLL0~3 analog power, 1.1V	-
AVSPLL	P	W13		AVSPLL: PLL0~3 analog ground	-

Table 2-28 RTC Pins (10, 3 with GPIO input: PA30, PD14, PF30)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
RTCLK	AI	M20	32768Hz Oscillator	RTCLK:32768Hz clock input	VDDRTC
NC	AO	M21		NC: Not Connect	-
PWRON	O	L19	8mA	PWRON: Power on/off control of main power	VDDRTC
CLK32K PD14	O IO	L20	8mA, pullup-pe	CLK32K: 32768Hz clock output PD14: GPIO group D bit 14. When main power down, this pin is controlled by RTC register: CLK32K or PD14, pull-up enable/disable, input/output if it is PD14, 0/1 if it is PD14 output	VDDRTC
WKUP PA30	I I	M18	Schmitt	WKUP: Wakeup signal after main power down PA30: GPIO group A bit 30, input/interrupt only	VDDRTC
PF30	IO	L18	8mA, pullup-pe	PF30: GPIO group F bit 30	VDDRTC
PPRST_	I	M19	Schmitt	PPRST_: RTC power on reset and RESET-KEY reset input	VDDRTC
TEST_TE	I	L17	Schmitt, pull-down	TEST_TE: Manufacture test enable, program readable	VDDRTC
VDDRTC	P	M17		VDDRTC: 1.8V power for RTC and hibernating mode controlling that never power down	-
VDDRTC11	P	M15		VDDRTC11: 1.1V power for RTC core that never power down	

NOTES:

1 The meaning of phases in IO cell characteristics are:

a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.
b Output, Single-end: output and single-ended DDR IO are used.
c Output, Differential: output and differential signal DDR IO are used.
d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.
e 8/16mA out: The IO cell's output driving strength is about 8/16mA.
f Pull-up: The IO cell contains a pull-up resistor.
g Pull-down: The IO cell contains a pull-down resistor.
h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.
i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.
j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled
k Schmitt: The IO cell is Schmitt trig input.

2 All GPIO shared pins are reset to GPIO input.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIOn power supplies voltage	-0.5	3.6	V
VDDcore power supplies voltage	-0.2	1.21	V
AVDPLL power supplies voltage	-0.2	1.21	V
AVDEFUSE power supplies voltage	-0.5	2.75	V
VDDRTC11 power supplies voltage	-0.5	1.3	V
VDDRTC power supplies voltage	-0.5	3.63	V
AVDUSB25 power supplies voltage	-0.5	2.75	V
AVDUSB33 power supplies voltage	-0.5	3.63	V
AVDAD power supplies voltage	-0.5	3.63	V
AVDCDC power supplies voltage	-0.5	3.63	V
AVDLVDSPLL power supplies voltage	-0.2	3.63	V
AVDLVDS power supplies voltage	-0.5	3.63	V
AVDHDMI25 power supplies voltage	0	2.75	V
AVDHDMI power supplies voltage	0	5.0	V
Input voltage to VDDmem supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO supplied non-supply pins with 5V tolerance	-0.5	6.0	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDIOn supplied non-supply pins	-0.5	3.6	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	3.6	V
Input voltage to AVDCDC supplied non-supply pins	-0.5	3.5	V
Input voltage to AVDUSB25 supplied non-supply pins	-0.5	2.75	V
Input voltage to AVDUSB33 supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDAD supplied non-supply pins	-0.5	3.63	V
Input voltage to AVDHDMI supplied non-supply pins	0	5.0	V
Output voltage from VDDmem supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDIO supplied non-supply pins	-0.5	3.6	V

Output voltage from VDDIOn supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC11 supplied non-supply pins	-0.5	1.3	V
Output voltage from AVDUSB25 supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDUSB33 supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDAD supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDHDMI supplied non-supply pins	0	5.0	V
Output voltage from AVDCDC supplied non-supply pins	-0.5	4.6	V
Output voltage from AVDLVDS supplied non-supply pins	-0.5	3.6	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDMEM voltage for LPDDR	1.65	1.8	1.95	V
	VDDMEM voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
	VDDMEM voltage for DDR3	1.425	1.5	1.575	V
	VDDMEM voltage for DDR3L	1.28	1.35	1.45	V
	VDDMEM voltage for DDR3U	1.19	1.25	1.31	V
	VDDMEM voltage for LPDDR2	1.14	1.2	1.3	V
VIO	VDDIO voltage	3	3.3	3.6	V
VION	VDDIOn voltage	3	3.3	3.6	V
VCORE	VDDcore voltage	0.99	1.1	1.21	V
VPLL	AVDPLL analog voltage	1.08	1.1	1.21	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTC11	VDDRTC11 voltage	0.99	1.1	1.21	V
VRTC	VDDRTC voltage	1.8	1.8	3.6	V
VUSB25	AVDUSB25 voltage	2.25	2.5	2.75	V
VUSB33	AVDUSB33 voltage	3.0	3.3	3.6	V
VADC	AVDAD voltage	3.0	3.3	3.6	V
VCDC	AVDCDC voltage	2.97	3.3	3.63	V
VLVDSPLL	AVDLVDSPLL voltage	3.0	3.3	3.6	V
VLVDS	AVDLVDS voltage	3.0	3.3	3.6	V
VHDMI	AVDHDMI voltage	0.99	1.1	1.21	V
VHDMI25	AVDHDMI25 voltage	2.25	2.5	2.75	V

Table 3-3 Recommended operating conditions for VDDmem supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VI18	Input voltage for DDR2/LPDDR applications	0		1.9	V
VO18	Output voltage for DDR2/LPDDR applications	0		1.9	V
VI15	Input voltage for DDR3 application	0		1.575	V
VO15	Output voltage for DDR3 application	0		1.575	V
VI135	Input voltage for DDR3L application	0		1.45	V
VO135	Output voltage for DDR3L application	0		1.45	V
VI125	Input voltage for DDR3U application	0		1.31	V
VO125	Output voltage for DDR3U application	0		1.31	V
VI12	Input voltage for LPDDR2 application	0		1.3	V
VO12	Output voltage for LPDDR2 application	0		1.3	V

Table 3-4 Recommended operating conditions for VDDIO/VDDIOn/VDDRTC supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	1.17		3.6	V
V_{IL18}	Input low voltage for 1.8V I/O application	–0.3		0.63	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7		3.6	V
V_{IL25}	Input low voltage for 2.5V I/O application	–0.3		0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2		3.6	V
V_{IL33}	Input low voltage for 3.3V I/O application	–0.3		0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	–20		85	°C

Table 3-6 Recommended operating conditions for ADC pins

Symbol	Description	Min	Typical	Max	Unit
Vbat	VBAT input voltage range	0		1.15	V
V_{IADC}	ADC_XP/ADC_XM/ADC_YP/ADC_YM/ADC_AUX1/ADC_AUX2 input voltage range	0		AVD_{AD}	V

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-7 DC characteristics for V_{REFMEM} and V_{TT}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM
VTT	Terminal Voltage	VREFM – 0.4	VREFM	VREFM + 0.4	V

Table 3-8 DC characteristics for VDDmem supplied pins in DDR3 application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREFMEM + 0.1		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VMEM -0.1	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic LOW			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	Ω
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=120		5.07	5.48	mA
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=60		8.45	9.28	mA
IOHL(DC)	PAD pin, 34Ω Output source/sink DC current, RTT=40		10.80	11.97	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=120		4.53	5.13	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=60		6.97	8.24	mA
IOHL(DC)	PAD pin, 50Ω Output source/sink DC current, RTT=40		8.42	10.21	mA
IMEM	VMEM standby current; ODT OFF		0.02	14.47	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		9.49	10.68	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.74	1.31	mA
IMEM	Input Low ODT/Drv=60/34,		6.51	7.65	mA

	IMEM DC current				
IMEM	Input High ODT/Drv=60/34, IMEM DC current		12.45	15.31	mA
ILS	Input leakage current, SSTL mode, unterminated		0.02	5.06	uA

Table 3-9 DC characteristics for VDDmem supplied pins in DDR3L application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREF + 0.09		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.09	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic Low			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	ohm
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.55	4.99	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.58	8.36	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.66	10.70	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=120		4.17	4.65	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.50	7.37	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.93	9.05	mA
IMEM	VMEM standby current; ODT OFF		0.02	13.48	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		8.25	9.40	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.48	1.02	mA
IMEM	Input Low ODT/Drv=60/34,		5.41	6.35	mA

	IMEM DC current				
IMEM	Input High ODT/Drv=60/34, IMEM DC current		11.29	13.28	mA
ILS	Input leakage current, SSTL mode, unterminated		0.01	4.80	uA

Table 3-10 DC characteristics for VDDmem supplied pins in DDR3U application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	VREF + 0.09		VMEM	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.09	V
VOH	DC output logic High	0.8 * VMEM			V
VOL	DC output logic Low			0.2 * VMEM	V
RTT	Input termination resistance (ODT) to VMEM/2	100 54 36	120 60 40	140 66 44	ohm
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.24	4.56	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.07	7.74	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.04	9.98	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=120		3.89	4.23	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.09	6.74	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.44	8.3	mA
IMEM	VMEM standby current; ODT OFF		0.02	12.39	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		7.6	8.42	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.34	0.78	mA
IMEM	Input Low ODT/Drv=60/34,		4.34	5.03	mA

	IMEM DC current				
IMEM	Input High ODT/Drv=60/34, IMEM DC current		9.38	10.76	mA
ILS	Input leakage current, SSTL mode, unterminated		0.005	4.53	uA

Table 3-11 DC characteristics for VDDmem supplied pins in DDR2 application

Symbol	Parameter	Min	Typical	Max	Unit
VIH(DC)	DC input voltage High	V_{REF} + 0.125		VMEM+0.3	V
VIL(DC)	DC input voltage Low	-0.3		VREF -0.125	V
VOH	DC output logic High	VMEM-0.28			V
VOL	DC output logic Low			+0.28	V
RTT	Input termination resistance (ODT) to VMEM/2	120 60 40	150 75 50	180 90 60	Ω
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=120		4.24	4.56	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=60		7.07	7.74	mA
IOHL(DC)	PAD pin, 34-ohm Output source/sink DC current, RTT=40		9.04	9.98	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=120		3.89	4.23	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=60		6.09	6.74	mA
IOHL(DC)	PAD pin, 50-ohm Output source/sink DC current, RTT=40		7.44	8.3	mA
IMEM	VMEM standby current; ODT OFF		0.02	12.39	uA
IMEM	Output Low Drv/RTT=34/60, IMEM DC current		7.6	8.42	mA
IMEM	Output High Drv/RTT=34/60, IMEM DC current		0.34	0.78	mA
IMEM	Input Low ODT/Drv=60/34,		4.34	5.03	mA

	IMEM DC current				
IMEM	Input High ODT/Drv=60/34, IMEM DC current		9.38	10.76	mA
ILS	Input leakage current, SSTL mode, unterminated		0.005	4.53	uA

Table 3-12 DC characteristics for VDDmem supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	Input logic threshold High	0.7* VMEM		VMEM+0.3	V
$V_{IL(DC)}$	Input logic threshold Low	VMEM-0.3		0.3* VMEM	V
VIH(AC)	AC Input logic High	0.8* VMEM		VMEM+0.3	V
VIL(AC)	AC Input logic Low	VMEM-0.3		0.2* VMEM	V
VOH	DC output logic High (IOH=-0.1mA)	0.9*VMEM			V
VOL	DC output logic Low (IOL=0.1mA)			0.1 *VMEM	V
ILL	Input leakage current		0.01	6.45	uA
IMEM	VMEM quiescent current		0.02	15.03	uA

Table 3-13 DC characteristics for VDDmem supplied pins in LPDDR2 application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	DC input voltage High	VREF + 0.13		VMEM	V
$V_{IL(DC)}$	DC input voltage Low	-0.3		VREF- 0.13	V
V_{OH}	DC output logic High	0.9 * VMEM			V
V_{OL}	DC output logic Low			0.1 * VMEM	V
IMEM	VMEM standby current		0.02	12.31	uA
IMEM	Output Low IMEM DC current		0.30	0.79	mA
IMEM	Output High IMEM DC current		0.28	0.76	mA
IMEM	Input Low IMEM DC current		0.30	0.79	mA
IMEM	Input High IMEM DC current		0.28	0.76	mA
ILL	Input leakage current		0.01	4.51	uA

Table 3-14 DC characteristics for VDDIO/VDDIOn/VDDRTC supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.77	0.84	0.92	V
V_{T+}	Schmitt trig low to high threshold point	0.99	1.1	1.19	V

V_{T-}	Schmitt trig high to low threshold point		0.62	0.73	0.82	V
V_{TPU}	Threshold point with pull-up resistor enabled		0.77	0.84	0.91	V
V_{TPD}	Threshold point with pull-down resistor enabled		0.77	0.85	0.92	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		0.99	1.1	1.19	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		0.62	0.73	0.81	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		0.99	1.1	1.2	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		0.62	0.73	0.82	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		79	129	218	kΩ
R_{PD}	Pull-down Resistor		73	127	233	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	6.9	12.5	20.1	mA
		16mA	11.5	20.8	33.5	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	4.9	11.6	22.6	mA
		16mA	8.4	19.9	38.8	mA

Table 3-15 DC characteristics for VDDIO/VDDIOn/VDDRTC supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.03	1.13	1.23	V
V_{T+}	Schmitt trig low to high threshold point	1.32	1.45	1.56	V
V_{T-}	Schmitt trig high to low threshold point	0.92	1.01	1.12	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.03	1.13	1.23	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.05	1.14	1.23	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.32	1.45	1.55	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.91	1	1.12	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.33	1.46	1.56	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.92	1.01	1.13	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA
R_{PU}	Pull-up Resistor	53	82	132	kΩ

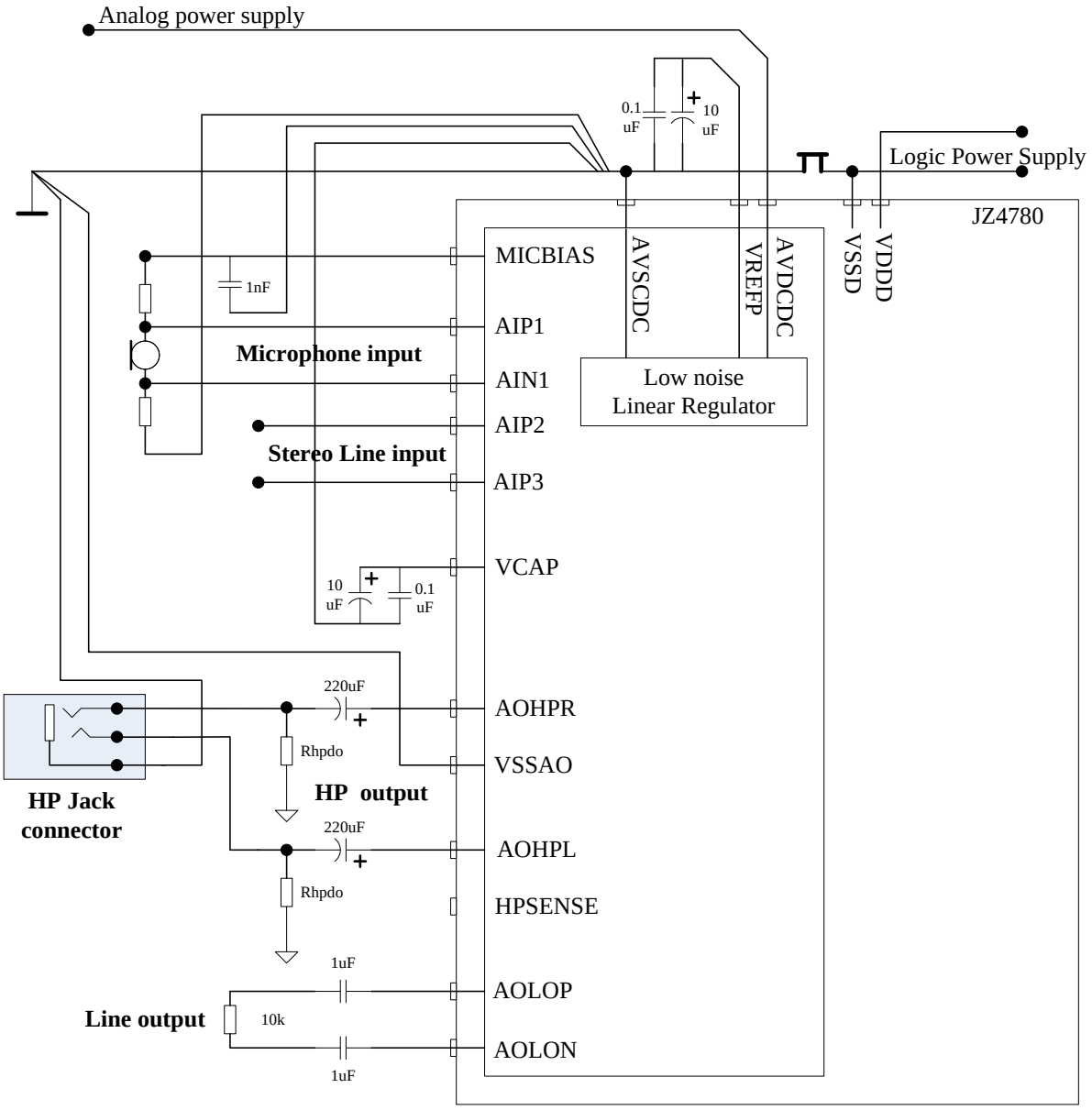
R_{PD}	Pull-down Resistor		51	82	143	kΩ
V_{OL}	Output low voltage				0.7	V
V_{OH}	Output high voltage		1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	15.1	25.3	37.3	mA
		16mA	25.1	42.2	62.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.3	26.6	46.4	mA
		16mA	22.8	45.7	79.6	mA

Table 3-16 DC characteristics for VDDIO/VDDIOn/VDDRTC supplied pins for 3.3V application

Symbol	Parameter		Min	Typical	Max	Unit
V_T	Threshold point		1.34	1.46	1.6	V
V_{T+}	Schmitt trig low to high threshold point		1.69	1.83	1.96	V
V_{T-}	Schmitt trig high to low threshold point		1.21	1.32	1.46	V
V_{TPU}	Threshold point with pull-up resistor enabled		1.33	1.44	1.59	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.36	1.47	1.6	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.69	1.82	1.94	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.2	1.31	1.45	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.71	1.84	1.97	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.23	1.33	1.46	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		41	60	92	kΩ
R_{PD}	Pull-down Resistor		43	64	104	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	13.1	20.2	27.4	mA
		16mA	21.9	33.8	45.7	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	19.3	38.2	64.5	mA
		16mA	33.1	65.4	110.5	mA

3.4 Audio codec

3.4.1 Application schematic



Note: 1. The Rhpdo value is 470 Ohm, it use to prevent pop-up noise.

2. The single-ended/differential input port AIP1/AIN1 and single-ended input port AIP2/AIP3 can be configure to microphone input or line input by software.

3. VREFP/VCAP/VREFP each of them requires connecting decoupling capacitors (0.1uF) between the pads VREFP/VCAP/VREFP and AVSCDC. This ceramic capacitor has to be kept as close as possible to IC package (closer than 0.2 inch)

3.4.2 Line input to audio ADC path

Measurement conditions: T = 25°C, AVDCDC = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale, Gain GIDL, GIDR = 0dB (note 1)	1.89	2.12	2.39	Vpp
	Full Scale, Gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB	0.189	0.212	0.239	
SNR	A-weighted, 1 kHz sine wave @ Full Scale and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 0 dB	85	90		dB
	A-weighted, 1 kHz sine wave @ Full Scale and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB	75	80		dB
THD	1 kHz sine wave @ Full Scale -1 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 0 dB		-80	-70	dB
	1 kHz sine wave @ Full Scale -1 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB		-70	-60	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale -60 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 0 dB (note 1)	85	90		dB
	A-weighted, 1 kHz sine wave @ Full Scale -60 dB and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB (note 1)	75	80		dB
PSRR	100 mVpp 1 kHz sinewave is applied to AVD, input data is 0 and gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB		90		dB
Gain boost accuracy	GIM1, GIM2 @1 kHz	-1		+1	dB
Input resistance	Boost gain GIM1, GIM2 = 0 dB	63	80	96	kOhm
	Boost gain GIM1, GIM2 = 20 dB	10	12.5	15	
Input capacitance	Includes 10pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Input capacitance		1		uF

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR.

Note 2: The Full Scale input voltage scales with LDO output: VREFP.

3.4.3 Audio DAC to headphone output path

Measurement conditions: T = 25°C, AVDCDC = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level (3)	Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load	1.89	2.12	2.39	Vpp
	Full Scale, Gain GOL, GOR = -3 dB, GODL, GODR = 0 dB, 16 Ohm load	1.33	1.5	1.69	Vpp
Maximum output power	Rl = 16 Ohm		17.6		mW
SNR	A-weighted, 1 kHz sine wave @ Full Scale, Gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load	95	100		dB
Idle Noise	A-weighted with no signal and gain GOL, GOR= -10 dB, GODL, GODR = 0 dB, 16 Ohm load		-103	-98	dBV
THD, THD+N	1 kHz sine wave @ Full Scale -1 dB, GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load		-85	-75	dB
	1 kHz sine wave @ Full Scale -1 dB and gain GOL, GOR = -3 dB, GODL, GODR = 0 dB, 16 Ohm load		-70	-65	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale -60 dB, Gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load (note 1)	95	100		dB
Wide Band Noise	1 kHz sine wave @ Full Scale and gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load, measurement bandwidth 20 kHz – 100 kHz		65		dB
PSRR	100 mVpp 1 kHz sinewave is applied to AVD, input data is 0 and gain GOL, GOR = 0 dB, GODL, GODR = 0 dB, 10 kOhm load		90		dB
	100 mVpp 1 kHz sinewave is applied to AVD, input data is 0 and gain GOL, GOR		90		dB

	= -25 dB, GODL, GODR = 0 dB, 16 Ohm load				
PuN	Active <-> inactive, 10 kOhm load		-60		dBVp
	Active <-> inactive, 16 Ohm load		-60		dBVp
Output resistance	Rl	16			Ohm
Output bypass capacitor	Cl (Rl = 10 kOhm)			1	uF
	Cl (Rl = 16 Ohm)			220	uF

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR with a FS-60 dB input signal.
Note 2: Output may oscillate above specified load capacitances. The capacitance is equivalent to a 2-meter cable.
Note 3: The Full Scale input voltage scales with the nLR output: VREFP.

3.4.4 Audio DAC to mono line output path

Measurement conditions: T = 25°C, AVD = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Output level (2)	Full Scale, Gain GODL, GODR = 0 dB	3.78	4.25	4.78	Vpp
SNR	A-weighted, 1 kHz sine wave @ Full Scale, Gain GODL, GODR = 0 dB	90	95		dB
THD+N	1 kHz sine wave @ Full Scale -1 dB, Gain GODL, GODR = 0 dB		-85	-75	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale – 60 dB, Gain GODL, GODR = 0 dB (note 1)	90	95		dB
PSRR	100 mVpp 1 kHz sinewave is applied to AVD, Gain GODL, GODR = 0 dB, input data is 0		90		dB
Output resistance	Rl	10			kOhm
Output capacitance	Cp			100	pF

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR.
Note 2: The Full Scale input voltage scales with the nLR output: VREFP.

3.4.5 Line input to headphone output path (analog bypass)

Measurement conditions: T = 25°C, AVDCDC = 3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96

kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Input level	Full Scale	1.89	2.12	2.39	Vpp
	Full Scale, Gain GIDL, GIDR = 0 dB, boost gain GIM1, GIM2 = 20 dB	0.189	0.212	0.239	
Input resistance		10k			Ohm
Output level (2)	Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load (note 1)	1.89	2.12	2.39	Vpp
	Full Scale, Gain GOL, GOR = -3 dB, GIL, GIR = 0 dB, 16 Ohm load	1.33	1.5	1.69	Vpp
SNR	A-weighted, 1 kHz sine wave @ Full Scale, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB	95	100		dB
THD, THD+N	1 kHz sine wave @ Full Scale -1 dB, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load		-85	-75	dB
	1 kHz sine wave @ Full Scale -1 dB and gain GOL, GOR = -3 dB, GIL, GIR = 0 dB, 16 Ohm load		-70	-65	dB
Dynamic range	A-weighted, 1 kHz sine wave @ Full Scale -60 dB, Gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load (note 1)	95	100		dB
PSRR	100 mVpp 1 kHz sinewave is applied to AVD, input data is 0 and gain GOL, GOR = 0 dB, GIL, GIR = 0 dB, 10 kOhm load		90		dB
	100 mVpp 1 kHz sinewave is applied to AVD, input data is 0 and gain GOL, GOR = -25 dB, GIL, GIR = 0 dB, 16 Ohm load		90		dB
PuN	Active <-> inactive, 10 kOhm load		-60		dBVp
	Active <-> inactive, 16 Ohm load		-60		dBVp
Output resistance	Rl	16			Ohm
Gain accuracy	GIL, GIR @1 kHz	-0.5		+0.5	dB
Input capacitance	Includes 10 pF for ESD, bonding and package pins capacitances			25	pF
Input bypass capacitor	Cbyline		1		uF
Polarity	AIL,R to AOL,R		+1		

Note 1: The specified value is extrapolated by adding 60 dB to the measured SNR.

Note 2: The Full Scale input voltage scales with the nLR output: VREFP.

3.4.6 Micbias and reference

Measurement conditions: T = 25°C, AVDCDC=3.3 V, input sine wave with a frequency of 1 kHz, Fmclk = 12 MHz, Fs = 8 to 96 kHz, measurement bandwidth 20 Hz – 20 kHz, unless otherwise specified.					
Parameter	Test conditions	Min.	Typ	Max.	Unit
Micbias output level		2.35	2.5	2.65	V
Micbias output current				4	mA
Micbias output noise	A-weighted		30	40	uVrms
Micbias decoupling capacitor	Cmic	0.75	1	1.25	nF
VCAP voltage			2		V
VREFP		2.35	2.5	2.65	V

3.5 Power On, Reset and BOOT

3.5.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the JZ4780 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1 shows this sequence and Table 3-17 gives the timing parameters. Following are the name of the power.

- VDDRTC
- AVDAUD: AVDCDC
- VDD11: all 1.1V power supplies, include VDDCORE, AVDPLL
- VDD: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIOn
- AVD: all other analog power supplies: AVDAD, AVDOTG25, AVDUSB, AVDLVDS, AVDLVDSPLL, AVDHDMI, AVDHDMI25
- AVDEFUSE

Table 3-17 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD33 arriving 50% (or 90%)	0	–	ms
t_{R_VDD11}	VDD11 rise time[1]	0	5	ms
t_{D_VDD11}	Delay between VDD arriving 50% (or 90%) to VDD11 arriving 50% (or 90%)	–1	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms
t_{D_AVDAUD}	Delay between VDD11 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms

t_{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]
$t_{D\_VPEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

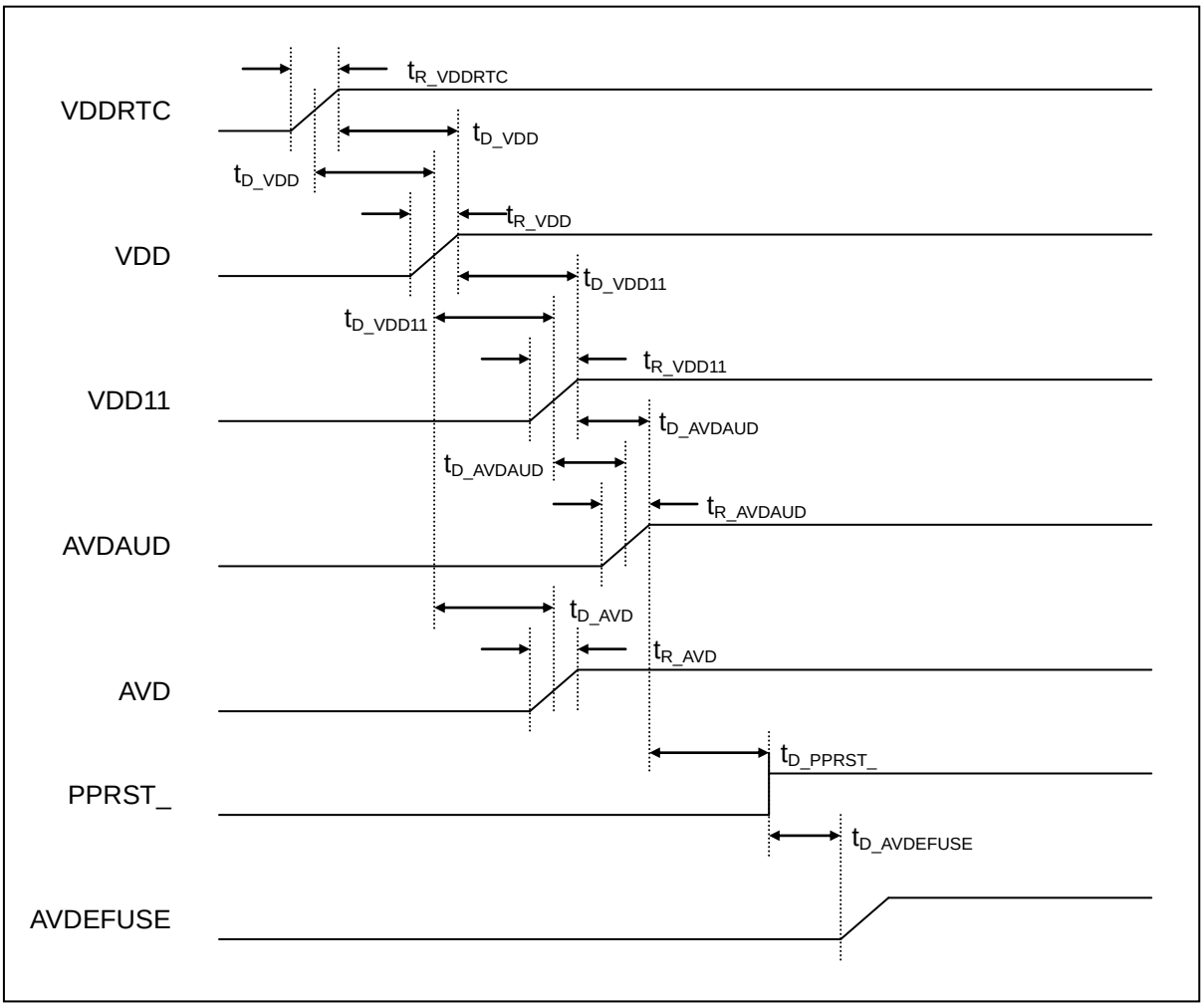


Figure 3-1 Power-On Timing Diagram

3.5.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see "2.5Pin Description [1][2]" for details. The PWRON is output 1. The oscillators are on. The USB 2.0 OTG PHY and USB 1.1 PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.5.3 BOOT

JZ4780 supports 7 different boot sources depending on BOOT_SEL0, BOOT_SEL1 and BOOT_SEL2 pins values. Table 3-18 lists them.

Table 3-18 Boot from 3 boot sources

BOOT_SEL2	BOOT_SEL1	BOOT_SEL0	Boot From
1	1	1	usb boot
1	0	0	msc1 boot
1	0	1	msc0 boot
0	1	1	emmc boot
1	1	0	nand boot
0	0	0	spi boot
0	0	1	Reserves
0	1	0	nor boot (CS2)

The boot procedure is showed in the following flow chart:

- In case of NAND/SDcard/iNAND/SPI boot, if it fails, enter MSC1 and USB boot.
- In case of USB boot, if it cannot connect to USB host within 10 seconds, restart the boot procedure.
- In case of NOR boot, if it fails, restart the boot procedure.
- If the boot procedure has been repeated more than 3 times, enter hibernating mode.